Chain-rule resistance: a new circuit principle for inherently linear ultra-low-power on-chip transconductances or transresistances

W.A. Serdijn, A.C. van der Woerd and H.M. van Roermund

Indexing terms: Analogue circuits, Transconductors

It is shown that, with the aid of five system blocks: namely two differentiators, an integrator, a multiplier and a nonlinear transresistor, it is possible to obtain an inherently linear transresistor. A circuit implementation that comprises only two capacitors and a handful of transistors is proposed. The transresistor can be linearly controlled over a wide range, from a few kilo-ohms up to many giga-ohms.

Introduction: Transconductors and transresistors are important building blocks in electronic systems for the conversion of voltage into current or vice versa. Usually, to implement these functions, resistors are taken and embedded in some kind of feedback structure. However, when going to lower and lower currents, below 1 μA, the resistor values become too large for integration. The only components that remain suitable for the IC designer are capacitors and transistors, and the question arises as to whether it is possible to obtain an inherently linear active transconductor or transresistor with these components.

In the following Section it is shown that, using five mathematical operators, namely two differentiators, an integrator, a multiplier and a nonlinear transresistor, this indeed is possible. The last Section deals with a class-A implementation of the new principle that uses transistors and capacitors only.

Principle of operation: In this Letter we focus on the realisation of a linear transresistor. A linear transconductor is easily realised by connecting a transresistor in the feedback path of a high-gain amplifier.

Let the desired input–output relation be

$$v_2 = i_1 R \tag{1}$$

with v_2, i_1 and R the output voltage, the input current and the (constant) (trans)resistor value, respectively.

Now suppose v_1 is some internal quantity, which is a function of i_1: $v_1 = G(i_1)$. Differentiating eqn. 1 with respect to time, applying the chain rule yields

$$\frac{dv_2}{dt} = R\frac{di_1}{dv_1}\frac{dv_1}{dt} \tag{2}$$

Integrating this expression again over time and neglecting the constant (DC) term results in

$$v_2 = R\int \frac{di_1}{dv_1}\frac{dv_1}{dt}\,dt \tag{3}$$

From this expression it can be deduced that an inherently linear transresistance is feasible if it is possible to implement the two derivatives, the integration and the multiplication. The corresponding block diagram is depicted in Fig. 1.

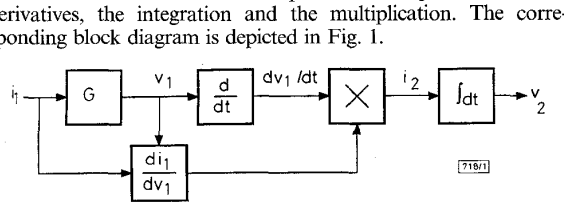

Fig. 1 *General block diagram of chain-rule transresistor*

In practice, on a chip there is only one type of component available that can act as a time integrator or differentiator, namely the capacitor. Hence, as suggested by their names, v_1 must be a voltage and i_2 must be a current. As both the input signals and the output signal of the multiplier are currents, a translinear circuit is the natural choice to implement the multiplier.

G is a current-to-voltage converter, which may be nonlinear. The only demand made on G for correct operation of the chain-rule transresistor is that its derivative with respect to i_1 must exist and that both functions are integratable using transistors only.

A convenient implementation for G may be the logarithmic relation between the collector current and the base-emitter voltage of a single bipolar transistor. MOS transistors, biased in weak inversion and driven at the gate and/or the back-gate (bulk) terminal [1], or even 'compound transistors' [2, 3], are also possible. Assuming a bipolar transistor, it follows that

$$v_1 = G(i_1) = V_T \ln(i_1/I_S) \tag{4}$$

V_T and I_S are two normalising constants. As the derivative of i_1 with respect to v_1 is proportional to the input current, we thus may replace the block di_1/di_1 by a simple connection. The result is shown in Fig. 2.

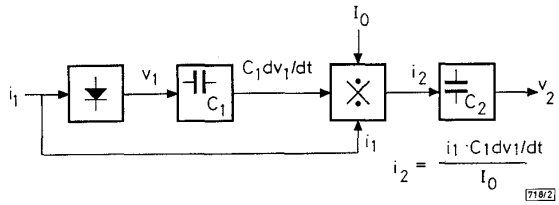

Fig. 2 *Possible embodiment of chain-rule transresistor*

The output voltage v_2 equals

$$v_2 = \frac{1}{C_2}\int i_2\,dt \tag{5}$$

$$= \frac{1}{C_2}\int \frac{i_1 C_1 dv_1/dt}{I_O}\,dt \tag{6}$$

$$= \frac{1}{C_2}\int \frac{i_1 C_1 V_T di_1/dt}{I_O i_1}\,dt \tag{7}$$

$$= \frac{C_1}{C_2}\frac{V_T}{I_O} i_1 \tag{8}$$

I_O being a normalising constant current, which is used in the multiplier to generate a current output (i_2).

Hence, the transresistor R is given by

$$R = \frac{C_1}{C_2}\frac{V_T}{I_O} \tag{9}$$

From this expression it can be seen that, by using capacitors and transistors only, it is possible to obtain an inherently linear transresistor, which can be controlled by means of a current I_O. If I_O is made proportional to the absolute temperature (PTAT), the transresistor becomes independent of the temperature.

Note that, because of the logarithmic diode transfer, the voltage across capacitor C_1, v_1, is compressed. This is beneficial in a low-voltage environment [4]. Also note that, in contrast to the overall transfer function, the internal quantities $C_1 dv_1/dt$ and i_2 are frequency-dependent. This implies that implementing a transresistor, when using this technique, will not be without difficulties if the frequency range is wider than several decades.

Another possible implementation for G (Fig. 1) may be the inverse of a hyperbolic sine function ($\sinh^{-1}$), which results from, for example two diode-connected transistors in antiparallel. The resulting transresistor topology is easily implemented in class AB. For low input signals, this may result in a lower noise production of the complete chain-rule transresistance than its resistor counterpart.

Design example: A possible, very compact embodiment of a class-A chain-rule transresistor was inspired by the current-companding integrator of Seevinck [5] and is depicted in Fig. 3.

Transistors Q_1–Q_4 are connected in a translinear loop and implement both the multiplier/divider function for the generation of i_2 [Note 1] and the nonlinear function $v_1 = G(i_1) = V_T \ln(i_1/I_S)$. To make the discharge of C_1 possible, an additional current source I_O is connected in parallel with C_1. To restore the desired multiplier/divider output signal, the input current i_i is subtracted from the output at node v_2 by transistor Qm_3. Qm_1–Qm_4 together form a current mirror with two outputs. Qm_4 provides the necessary base currents of the output transistors. A voltage-follower, consisting of Qm_1–Qm_3, generates a low-impedance version of v_2 to avoid

Note 1: This circuit is also known as the 'log-antilog' multiplier [6]

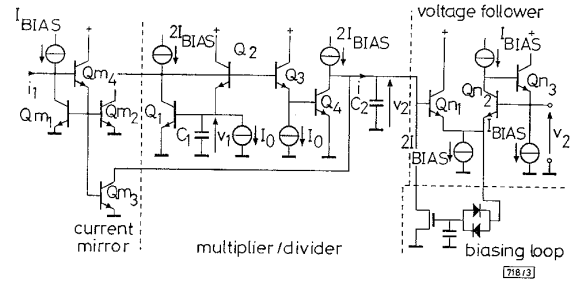

Fig. 3 *Circuit diagram of chain-rule transresistor*

interaction. Note that the output voltage swing of the transresistor is limited by the embodiment of the voltage-follower only. For a wider output swing, e.g. from rail to rail, it is possible to replace C_2 and the follower by an integrating transimpedance amplifier.

The correct biasing of the circuit has been ensured by several DC current sources and a simple lowpass filter consisting of two diodes, a (small) capacitor and an NMOS transistor.

The circuit shown in Fig. 3 was simulated using SPICE and realistic transistor and capacitor models. The results indicate the correct operation of the chain-rule resistance for various temperatures and values of I_O, I_{BIAS}, C_1 and C_2, yielding linear transresistances ranging from several kΩ up to many GΩ. Connecting the collector of Qn_3 to the input (i_1) and a minor adaptation of the biasing circuitry result in a linear (grounded) resistance. Fig. 4 depicts a simulation for C_1 = 200pF, C_2 = 10pF, I_O = I_{BIAS} = 50nA and a sinusoidal input signal of 1kHz, 25nA amplitude. With these values, the resistance = 9.4MΩ and the total harmonic distortion is <1% over 470mV (peak-to-peak).

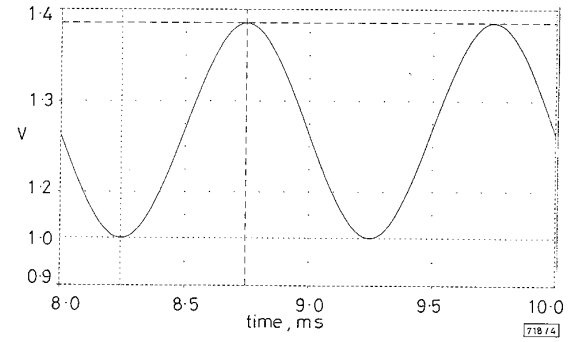

Fig. 4 *Simulation of chain-rule resistance for C_1 = 200pF, C_2 = 10pF, I_O = I_{BIAS} = 50nA and a sinusoidal input signal of 1kHz, 25nA amplitude*

Conclusions: In this Letter it has been shown that, with the aid of five system blocks, two differentiators, an integrator, a multiplier and a nonlinear transresistor, an inherently linear transresistance can be obtained, without the need for resistors. A circuit implementation, operating in class A and consisting of only two capacitors and a handful of transistors, has been proposed. The transresistor value can easily be controlled over a wide range by means of a current. If this current is proportional to the absolute temperature, the transresistor becomes independent of the temperature. Implementing the internal nonlinear transresistor by two diode-connected transistors paves the way for class-AB operation, which, in turn, enables the transresistance to have a wider dynamic range than its resistor counterpart.

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Improvement of SOI MOS current-mirror performances using serial-parallel association of transistors

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Indexing terms: Silicon-on-insulator, MOSFET, Analogue circuits

The serial-parallel association of SOI MOSFETs proves to be useful for increasing the breakdown voltage and the early voltage of transistor structures. This permits one to realise current mirrors with an output-to-input current ratio close to unity in the weak, moderate and strong inversion regimes of the MOSFETs.

SOI MOSFETs may suffer from a low drain breakdown problem which tends to decrease their output impedance and therefore their Early voltage [1]. This effect leads to the degradation of analogue cells fabricated using that technology, and, in particular, the performance of current mirrors. These are an important component of analogue circuits and are supposed to deliver a current which is independent of the voltage applied to the drain of the output transistor. Several solutions have been proposed to improve the breakdown voltage of the transistors and their output impedance, such as the twin-gate SOI MOSFET [2]. Such devices are, however, not standard and the use of master and slave sections having the same width, but different channel lengths was previously recognised to be a suboptimal solution [3]. Recently, it has been proposed to use the serial-parallel combination of MOSFETs to achieve an improvement of the output conductance [4]. In this Letter it is shown that the serial-parallel association of MOSFETs improves the drain breakdown voltage and the Early voltage of SOI MOSFET cells. In particular, it greatly improves the performance of current mirrors, especially in the moderate and weak inversion regimes, which is of importance in increasing the output swing of analogue functions operating at low supply voltages.

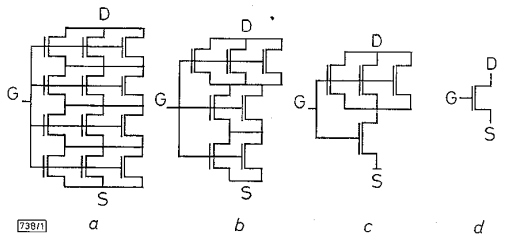

Fig. 1 *Serial-parallel association of 12, seven and four transistors*

a 12 transistors
b Seven transistors
c Four transistors
d Reference transistor