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Simple low-voltage weak inversion MOS 1/*x* circuit

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Indexing terms: MOS integrated circuits, Analogue computer circuits, Current mode circuits

A circuit with a transfer function $I_{out} = c/I_{in}$ (1/*x* circuit) with MOSFETs biased in weak inversion is presented. The circuit operates at a supply voltage that is a few hundred millivolts above one threshold voltage. The accuracy is +4%/−8% with respect to the desired transfer over a 6pA to 2nA input current range.

Introduction: Translinear circuits whose output current is inversely proportional to the input current usually need a supply voltage larger than two base-emitter or gate-source voltages [1]. Therefore, these circuits are not suitable for low-voltage applications. The circuit presented here uses MOSFETs in weak inversion and it can operate at a supply voltage that is only slightly above one threshold voltage.

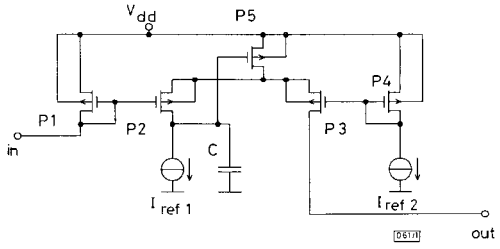

Fig. 1 *1/x circuit*

Operation of 1/x circuit: In Fig. 1 the 1/*x* configuration is shown. When the current through *P*1 increases, its gate-source voltage (V_{GS}) also increases. The drain current of *P*2 is kept constant by the feedback loop *P*5-*P*2. Consequently, the gate-source voltage of *P*2 is almost constant, so the gate-source voltage of *P*3 decreases when the gate-source voltage of *P*1 increases. As a result of the exponential relationship between the gate-source voltage and the drain current (I_D) of MOSFETs biased in weak inversion, the output current is inversely proportional to the input current and equals $I_{out} = I_{ref1}I_{ref2}/I_{in}$ when *P*1 and *P*4 have equal *W*/*L* ratios, and *P*2 and *P*3 have equal *W*/*L* ratios.

The maximal input current is limited by the requirement that *P*1 must operate in the weak inversion region and by the requirement that the output current must always be large compared to the leakage currents. The output current will always be smaller than I_{ref2} multiplied by the scaling factor between *P*4 and *P*3; this implies that the circuit can only function properly when the input current is larger than I_{ref1}, divided by this scaling factor. Of course, the input current should also be large compared to the leakage currents.

A breadboard realisation of the circuit has been made. *P*1 and *P*4 are 108/7.5 transistors, *P*2 and *P*3 are two groups of four 108/7.5 transistors connected in parallel, *P*5 is a group of four 72/3 transistors connected in parallel, I_{ref1} is a 10 pA current obtained by scaling down a 30pA current with a 3:1 current mirror, I_{ref2} = 5 nA and *C* is a 12pF capacitor with a low leakage current (ceramic tube type). $V_{TH_NMOS} \simeq 0.75$V and $V_{TH_PMOS} \simeq -1$V.

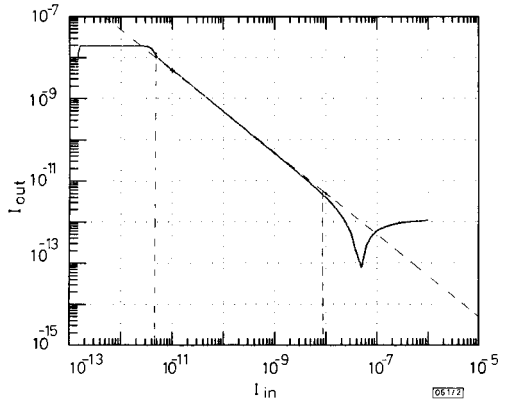

Fig. 2 I_{out} *against* I_{in}

Fig. 2 shows the results at a supply voltage of 1.3V; the output is loaded by a 0.65V voltage source. The circuit is accurate within +4%/−8% with respect to the desired transfer over a 6pA to 2nA input current range (with a supply current smaller than 15nA), and within 20% over a 4.5pA to 9nA range (I_{DD} < 26nA).

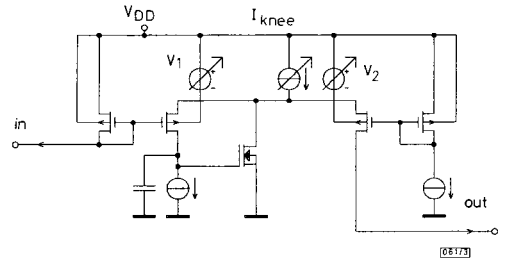

Fig. 3 *Special variant of 1/x circuit*

Special variant of circuit: A bipolar [3] and an MOS hearing aid-IC with on-chip compressor-expander systems are being developed in our laboratory. For an application in the MOS compander system, the reciprocal value (1/*x*) of a control current has to be determined; this control signal has to be multiplied by a factor that depends exponentially on a control voltage, divided by a factor that depends exponentially on another control voltage and it has to be limited to an adjustable maximum value. The control current that has to be processed lies in the 330pA to 165nA range. A high degree of accuracy is not necessary. These functions can all be combined into one circuit, shown in Fig. 3. The current limit can be controlled with I_{knee}. Because the drain current of a MOSFET in weak inversion depends exponentially on the back gate-source (or bulk-source) voltage V_{BS} (Fig. 2), the transfer depends exponentially on the voltages *V*1 and *V*2. According to simulations the error is −43%/+45% when V_1 = 0.3616V and V_2 = 0.2V, which is acceptable for this application.

Conclusions: A simple MOS $1/x$ circuit has been presented. The circuit uses MOSFETs operating in the weak inversion region and a supply voltage a few hundred millivolts above the threshold voltage suffices. A breadboard realisation is accurate within +4%/−8% with respect to the desired transfer over a 6 pA to 2 nA input current range.

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Area-time efficient diminished-1 multiplier for Fermat number transform

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Indexing terms: Digital arithmetic, Number theoretic transforms

A new regular implementation of a diminished-1 multiplier is presented which requires less silicon area and achieves higher speed than existing designs. For a multiplier where the modulus involved is F_4, a 34% increase in the speed of operation is achieved in comparison to that of Sunder *et al.*

Introduction: Several algorithms that perform diminished-1 multiplication based on the work of [1] have been described recently [2, 3]. In this Letter, a regular structure for the implementation of a diminished-1 multiplier which requires less silicon area and at the same time provides higher operation speed than previously published works [2, 3] is presented.

Parallel multiplication: In this Section, a new diminished-1 multiplier is presented. Its architecture is implemented using a parallel diminished-1 multiplication followed by two stages of residue reduction. The realisation consists of a multiplier, carry save-adder, and a diminished-1 CLA adder as shown in Fig. 1 for n = 4, i.e. F_2, where the F_t (tth Fermat number) is represented by $n + 1 = 2^t + 1$ bits as has been shown in [2, 3]. The diminished-1 multiplier described here is for F_2 and can be generalised for any FNT. To illustrate the proposed method, the product of diminished-1 numbers X-1 and Y-1 can be given as [1]

$$XY-1=[(X-1)(Y-1)+(X-1)+(Y-1)+1]-1 \quad (1)$$

As shown in Fig. 1, the multiplier used in implementing this architecture is the carry save array, where an AND gated full-adder is used as its basic building block. In the (i,j)th cell, the ith bit of X is multiplied by the jth bit of Y and the product is added to the carry bit fed from the top and the sum bit which is propagating diagonally from left to right. The reasons for using the carry save array is that it is regular, modular, and very easy to design. Furthermore, at the same time that multiplication of the two numbers in their diminished-1 form is performed by the array, the addition of both the multiplier and the multiplicand can be easily incorporated by feeding them to the sum and the carry inputs at the top edge of the array, while a correction term equal to $2^n(2^n-1)$ (for reasons that will be explained in the following Section), is fed to the free sum inputs at the left hand side boundary of the array. In this way, maximum use of the gated full-adder cells is achieved.

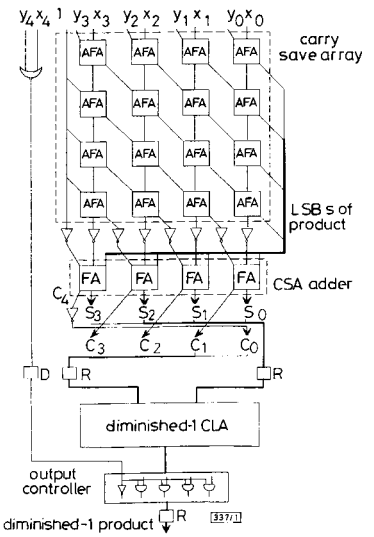

Fig. 1 *Block diagram of 4 × 4 pipelined diminish-1 multiplier using carry save array*

In the new scheme, the use of the separate column of half adders to add 1, as has been implemented in [3], is eliminated. As will be explained later, the addition of 1 in eqn. 1 will be achieved at the CSA-adder stage.

When the MSBs of the multiplicand and the multiplier are zero, the NOR output is one and the above multiplication scheme produces the correct results. If the NOR operation induces a zero, then either or both the MSBs of the multiplicand and the multiplier are 1 (i.e. either (or both) the multiplicand and the multiplier is zero). As a result, the multiplication product should be zero. To take this into consideration, a output controller unit proposed in [3] is used as shown in Fig. 1. When the NOR of the MSBs of the two operands is one, the output of the unit is the correct product. On the other hand, when the NOR operation induces a zero, the output of the unit is zero.

Residue reduction: In [3] a CPA adder is used to compute the most significant bits of the product from the two sets of bits that come out of the lower boundary of the array multiplier. The output of the CPA is then negated and added to the LSBs which exits from the right boundary of the array multiplier to perform residue reduction [1]. In this Letter, these two sets of bits that come out of the lower boundary of the array are termed carry word 1, C_1, and carry word 2, C_2. In the proposed architecture, a CPA adder is not used and instead the two carry words C_1 and C_2 (whose sum represents the MSB bits of the product) are negated and added to the LSBs of the same product. In the following we will explain that the addition of the correction term (2^4-1) to the MSBs of the product (i.e. adding $2^n(2^n-1)$) makes the sum of the two inverted (negated) carry words C_1 and C_2 equal to the inverted MSBs of the product. Let A_1 and A_2 be the two carry words produced at the lower boundary of the array without the addition of 2^4-1, and $C_t = A_1 + A_2$ (represents the MSBs of the product). Then by definition, adding the correction term 2^4-1 to the MSBs will induce the two carry words C_1 and C_2, because $C_1 + C_2 = 2^4-1 + A_1 + A_2 = 2^4-1 + C_t$. In the new scheme the two carry words C_1 and C_2 are inverted before adding them to the LSBs of the product, hence $C'_1 + C'_2 = 2(2^4-1)-(C_1 + C_2) = 2^4-1-C_t = C'_t$, where C'_1, C'_2, and C'_t are the inverted bits of C_1, C_2, and C_t, respectively. Therefore, instead of calculating C_t, negating and adding it to the LSBs of the product as was used in [3], we add $2^n(2^n-1)$, negate the two carry words and add them to the LSBs of the product.

As has been reported in [3], the negation is performed only if the MSB of the 9 bit multiplication product is zero, in which case all the five MSBs of the product except the MSB are complemented. If the MSB is equal to one the negation is inhibited. The only case in which the MSB is one in [3] is where the multiplicand and the multiplier are equal to 15 (16 diminished-1 form), i.e. the