10 NAY, K., and BUDAK, A.: 'A voltage-controlled resistance with wide dynamic range and low distortion', *IEEE Trans.*, 1983, **CAS-30**, pp. 770–772

11 SENANI, R., and BHASKAR, D.R.: 'Simple configuration for realizing voltage-controlled impendances', *IEEE Trans.*, 1992, **CAS-39**, (1), pp. 52–59

12 SENANI, R., and SINGH, V.K.: 'Single-element-controlled sinusoidal oscillator employing a single current conveyor IC', *Electron. Lett.*, 1992, **28**, (14), pp. 414–415

13 WILSON, B.: 'High-performance current conveyor implementation', *Electron. Lett.*, 1984, **20**, (24), pp. 990–991

14 FABRE, A.: 'Wideband translinear current conveyor', *Electron. Lett.*, 1984, **20**, pp. 241–242

√*x* circuit based on a novel, back-gate-using multiplier

M. van der Gevel and J.C. Kuenen

Indexing terms: MOSFETs, Multiplying circuits

A simple low-power low-voltage square-rooting circuit (or √*x* circuit) is presented. This circuit is based on a novel multiplier that uses the back gate of a MOSFET biased in weak inversion. A breadboard implementation has shown an error of less than 20% with respect to the desired transfer over an input current range from 4pA to 80nA.

Introduction: The drain current of a MOSFET biased in weak inversion approximately equals the product of a constant, I_O W/L, a factor that depends on the gate-source voltage V_{GS} and a factor that depends on the back gate-source (or bulk-source) voltage V_{BS}. This property has been used for the realisation of a simple low-power low-voltage one quadrant multiplier. This multiplier has been used as a squarer and has been placed in a negative-feedback path around a high-gain amplifier to obtain a simple low-power low-voltage square-rooting circuit.

Operation of multiplier: According to Pavasović [1] the drain current of a *p*MOSFET in weak inversion is

$$-I_D = I_O \frac{W}{L} e^{-\frac{V_{GS}}{\kappa U_T}} e^{-\frac{V_{BS}}{\eta U_T}}$$

when the MOSFET is biased in the saturation region ($-V_{DS} > 4U_T$, $U_T = kT/q \simeq 26$mV at room temperature). The factor κ is a constant, and although the factor η depends on the gate-source voltage, it can be considered to be approximately constant. In the case of an *n*MOSFET the minus signs have to be removed from the equation.

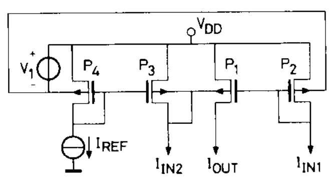

Fig. 1 *Back-gate-using multiplier*

When two of these MOSFETs are connected in a current-mirror configuration, the output current of the mirror is approximately proportional to the input current and depends exponentially on the difference between the back gate-source voltages of the transistors (this is a very useful technique when a controlled amplifier has to be realised). When an extra 'diode'-connected MOSFET is added, whose back gate instead of the normal gate is connected to the drain, the output current becomes proportional to both input currents. Hence, the circuit becomes a one quadrant multiplier. In Fig. 1 this configuration is shown. A fourth MOSFET provides the gate-source biasing voltage of P_3. For optimal accuracy, voltage source V_1 should have a value that roughly equals the average of the limits of the useful V_{BS} range. The current through the forward biased back gate-source junction should be negligible, therefore $-V_{BS}$ should be smaller than ~0.4V. Because the $-V_{BS}$ of P_3 equals its $-V_{DS}$, this voltage should be higher than ~60mV, otherwise P_3 would operate deeply in the triode region. Hence, V_1 = 0.23V is a reasonable value. When a somewhat lower degree of accuracy is acceptable, V_1 can be replaced by a short circuit and the W/L ratios of P_2 and P_4 can be increased. The output current equals $I_{OUT} = I_{IN1}I_{IN2}/I_{REF}$.

Operation of √x circuit: In Fig. 2, P_5 and N_1 – N_4 form a high-gain amplifier with three current outputs. Two of these outputs are connected to the multiplier; the output signal of the multiplier is fed back to the input of the amplifier. As a result of the negative-feedback action, the output current of the multiplier is forced to equal the input current of the entire circuit. This means that the output currents of the high-gain amplifier are forced to equal

$$I_{OUT} = \sqrt{I_{IN,ROOT} I_{REF}}$$

where $I_{IN,\ ROOT}$ is the input current of the entire square-rooting circuit.

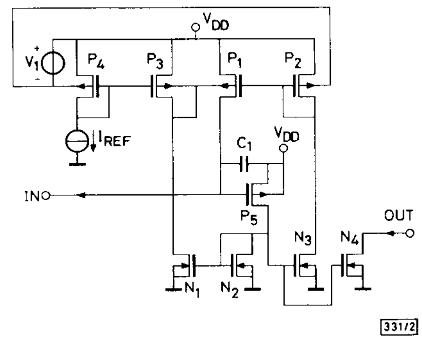

Fig. 2 *Square-root circuit*

Measurements were made of a breadboard circuit. Unfortunately, the *N*-wells of the breadboard ICs are internally connected, so we have replaced all *p*MOSFETs in the circuit by 108/7 *n*MOSFETS and all *n*MOSFETS by 108/7.5 *p*MOSFETs, and we have used the entire substrate of an IC with *n*MOSFETs as the controlled back gate. I_{REF} is 2.5nA, $V_{T,\ nMOS} \simeq 0.75$V, $V_{T,\ pMOS} \simeq -1$V and C_1 is a 6.8pF capacitor with a low leakage current (ceramic tube type). Fig. 3 shows the results at a supply voltage V_{DD} of 1.3V with a 0.65V voltage source connected to the output. The circuit is accurate within 20% with respect to the desired transfer (dashed line in Fig. 3) over an input current range from ~3.4pA to 80nA.

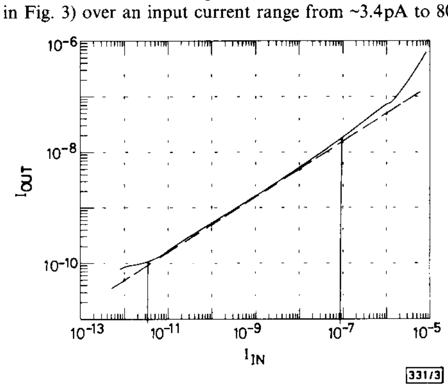

Fig. 3 *Measurement results*

Conclusions: A √*x* circuit based on a novel multiplier that uses the back gates of MOSFETs biased in weak inversion has been presented. The circuit operates at a low voltage (a few hundred millivolts above the threshold voltage), the supply current can be made as low as a few hundred nanoamps and a breadboard realisation operates over a 4 – 80nA input current range. However, the circuit is not suitable for high-accuracy applications.

2 December 1993

Electronics Letters Online No: 19940176

M. van de Gevel and J. C. Kuenen (*Delft University of Technology, Department of Electrical Engineering, Electronics Research Laboratory, Mekelweg 4, 2628 CD Delft, The Netherlands*)

References

1 PAVASOVIĆ A.: 'Subthreshold region MOSFET mismatch analysis and modeling for analog VLSI systems'. PhD Thesis, The John Hopkins University, Baltimore, Maryland, USA, 1991

Coherent detection of MPSK via efficient block estimation

P.Y. Kam and S.Y. Tay

Indexing terms: Detectors, Phase shift keying

A tree approach is proposed for efficient block estimation of MPSK sequences with unknown carrier phase. Its computational load increases with block length at a much lower rate than in previous algorithms. This enables coherent detection performance to be achieved through the use of large block lengths.

The trend in receiver design for coherent detection of M-phase phase shift keyed (MPSK) signals is moving towards completely digital architectures suitable for VLSI implementation. The theory of sequence estimation provides a class of digital signal processing algorithm ideally suited to this purpose. In [1], we applied the theory of maximum likelihood (ML) estimation of digital sequence and unknown carrier phase, and arrived at the quadratic receiver structure for an MPSK sequence. Under suitable conditions, this receiver was shown to attain coherent detection error performance as the sequence length goes to infinity. The only obstacle in its practical implementation is the exponential growth in complexity and computational load as sequence length increases. In [2], the same algorithm was proposed, except that the authors employed differential encoding to resolve ambiguities in sequence decision. This limits the ultimate performance of the receiver to that of coherent detection with differential encoding and decoding, which is worse than that of coherent detection without differential encoding and decoding. It also suffers from the problem of exponential receiver complexity and computational load.

This Letter follows the approach in [1], and employs MPSK with no differential encoding and decoding. A receiver is proposed which performs block-by-block detection of the sequence. Ambiguities in sequence decision are avoided by including the decision on the present block as part of the next block to be detected. A tree approach is developed by which the decision metrics can be computed with a computational load that is much reduced compared to that in [1, 2]. This allows the receiver to process efficiently with large block lengths, and enables error performances close to that of coherent detection to be attained with practical block sizes.

The model for the received signal $r(k)$ over the kth symbol interval $[kT, (k+1)T)$, T being the symbol duration, is [1, 2]

$$r(k) = E_s^{1/2} e^{j(\phi(k)+\theta)} + n(k) \qquad (1)$$

E_S is the energy per symbol, $\phi(k)$ is the data-modulation phase, and θ is the unknown carrier phase. Assume Gray coding of bits onto the phase $\phi(k)$ and the carrier phase θ to be slowly time-varying so that it can be considered constant over a duration longer than K symbol intervals. The term $n(k)$ is due to channel additive white Gaussian noise, and $\{n(k)\}$ is a sequence of independent complex Gaussian random variables with $E[n(k)] = 0$ and $E[n(k)n^*(l)] = N_O\delta_{kl}$ (superscript * denotes conjugate). Assume that the sequence $\mathbf{m} = E_s^{1/2}[e^{j\phi(0)}\ e^{j\phi(1)} \dots e^{j\phi(K-1)}]^T$ of K symbols has been sent (superscript T denotes transposed), and the sequence $\mathbf{r} = [r(0)\ r(1) \dots r(K-1)]^T$ of signals has been received. In [1], we have shown that the receiver which performs ML estimation of the sequence $\mathbf{m}$ and the unknown carrier phase θ decides on the sequence $\hat{\mathbf{m}}$ if

$$|\mathbf{r}\cdot\hat{\mathbf{m}}|^2 = \max_m |\mathbf{r}\cdot\mathbf{m}|^2 \qquad (2)$$

Here,

$$\mathbf{r}\cdot\mathbf{m} = \sum_{k=0}^{K-1} r(k) E_s^{1/2} e^{-j\phi(k)}$$

Thus, $|\mathbf{r}.\mathbf{m}|^2$ is the decision metric of a sequence $\mathbf{m}$

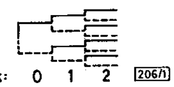

Fig. 1 *Tree for BPSK*

——— $\phi(k) = 0$
– – – – $\phi(k) = \pi$

To make a decision via eqn. 2 means that the receiver has to form the metric $|\mathbf{r}.\mathbf{m}|^2$ for each of the M^K symbol sequences $\mathbf{m}$, and this is the exponential complexity problem faced in [1, 2]. We now show that the computational load can be tremendously reduced by viewing the possible sequences $\mathbf{m}$ as paths through a tree, as in Fig. 1. In Fig. 1, we illustrate the tree for the simple case of M=2 and K=3. Using this point of view, we see that the receiver can compute the running sum

$$\sum_{i=0}^{k} r(i) E_s^{1/2} e^{-j\phi(i)}$$

recursively in time k for each possible sequence $\mathbf{m}$ (or each path through the tree) as the signals $\{r(k)\}_{k=0}^{K-1}$ are being received. Note, however, that at each time k, we only have to compute $r(k)E_s^{1/2}\,e^{-j\phi(k)}$ for the M possible values of $\phi(k)$, which leads to M complex multiplications. At time $k = K$–1, when all the signals have been received, $\mathbf{r}.\mathbf{m}$ is formed for all sequences $\mathbf{m}$, and the receiver then computes $|\mathbf{r}.\mathbf{m}|^2$ and makes a decision.

Using this tree approach, the total number of complex multiplications is KM. The number of complex additions at each time $k > 0$ is M^{k+1}, because there are M possible values of $r(k)E_s^{1/2}\,e^{-j\phi(k)}$ to be added to each of the M^k tree branches existing at the end of time k–1. Thus, the total number of complex additions is

$$\sum_{k=1}^{K-1} M^{k+1} = \frac{M^2}{M-1}(M^{K-1} - 1)$$

Observe that whereas the number of complex additions is exponential in sequence length K, the number of complex multiplications is only linear in K. Because multiplications consume more processing time than additions, this latter result is important.

Without using this tree approach [1, 2], the total number of complex multiplications is KM^K as there are M^K sequences each requiring K multiplications. The number of complex additions per sequence is K–1, resulting in a total of $M^K(K-1)$. This is basically KM^K for large K, while the number of additions in the tree approach is basically M^K (for large K and M). Thus, the tree approach leads to a drastic reduction in both the number of additions and multiplications.

Having developed the tree processing approach, we note that ambiguities can occur in sequence decision, because for any sequence, say $\mathbf{m}_0$, there is another sequence $\mathbf{m}_1$ such that $\mathbf{m}_1 = \mathbf{m}_o e^{j\beta}$, where $\beta = \pi$ rad for BPSK and $\beta = \pi/2$ rad or a multiple of $\pi/2$ rad for QPSK. Obviously, $|\mathbf{r}.\mathbf{m}_0|^2 = |\mathbf{r}.\mathbf{m}_1|^2$. One way to overcome this problem is to constrain all sequences $\mathbf{m}$ to have a common subsequence. Thus, we propose the following block-by-block detection algorithm. Assume that the sequence $\mathbf{m}$ above, transmitted over times $k = 0, 1, \dots, K-1$, is the first sequence, and that the first $K/2$ symbols $\{E_s^{1/2}\,e^{j\phi(k)}\}_{k=0}^{(K/2)-1}$ are known preamble symbols. Let K be even. With the reception of the signals $\{r(k)\}_{k=0}^{K-1}$, the decision on $\mathbf{m}$ is made via eqn. 2 using the tree processing approach. This leads to decisions on the symbols $\{E_s^{1/2}\,e^{j\phi(k)}\}_{k=K/2}^{K-1}$, which we denote as