60 GHz 5-bit digital controlled phase shifter in a digital 40 nm CMOS technology without ultra-thick metals

H. Gao✉, K. Ying, M.K. Matters-Kammerer, P. Harpe, B. Wang, B. Liu, W.A. Serdijn and P.G.M. Baltus

A 5-bit digital controlled switch-type passive phase shifter realised in a 40 nm digital CMOS technology without ultra-thick metals for the 60 GHz Industrial, Scientific and Medical (ISM) band is presented. A patterned shielding with electromagnetic bandgap structure and a stacked metals method to increase the on-chip inductor quality factor are proposed. To reduce the insertion loss from the transistors, the transistor switches are implemented with a body–source connection. For all 32 states, the minimum phase error is 1.5°, and the maximum phase error is 6.8°. The measured insertion loss is −20.9 ± 1 dB including pad loss at 60 GHz and the return loss is >10 dB over 57–64 GHz. The total chip size is 0.24 mm^2 with 0 mW DC power consumption.

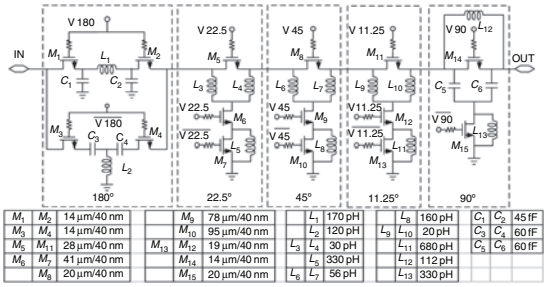
Introduction: Typical applications in the 60 GHz ISM band such as wireless high-definition video streaming require a high signal quality to achieve large data rate transfer. At 60 GHz, it is possible to integrate multiple antennas on chip. Beam steering is enabled electronically by on-chip phase shifters. The phased array architecture with RF phase shifter [1] is a compact solution for achieving on-silicon integration. In this solution, the main challenge is to design and implement a phase shifter with good phase accuracy, low loss and small phase/loss variation.

In the RF path, the phase shifters could be implemented using structures of switch type [2], vector sum [3] or reflection type [4] in CMOS technology. Compared with other structures, the switch-type digital controlled phase shifter is compact, and has the lowest power consumption. However, the switch-type phase shifter suffers from the problem of phase accuracy due to the cascading stages. In this Letter, a hybrid 180° stage is implemented to increase the phase accuracy and achieve broadband performance. Also, the method of body–source connection is applied to decrease the loss from transistor switches.

In a digital 40 nm CMOS technology without ultra-thick metal, we propose a patterned shielding with electromagnetic bandgap (EBG) structure, and a stacked metals method to increase the on-chip inductor quality factor.

5-bit digital controlled passive phase shifter with a hybrid 180° stage: The complete 5-bit phase shifter schematic is shown in Fig. 1. The 180° stage is using a hybrid structure, switching between low-pass and high-pass networks. Therefore, it can compensate the frequency-dependent phase variation between the two networks, and the whole frequency response is much more flat and broadband. Fig. 2 compares the insertion phase flatness of 180° stages using a cascaded two-stage low-pass structure and a hybrid structure. The hybrid structure has a smaller phase variation than the cascaded structure. The following 22.5°, 45° and 11.25° stages are implemented by using low-pass T-type networks. Compared with other stages, the 90° stage is implemented by using a Π-type structure. In the Π-type structure, the shunt inductor to the ground is 330 pH (L_{13}), while it will be only 66 pH if using the T-type structure. Therefore, the Π-type is more robust and less sensitive to the parasitic ground inductance in a single-ended structure for a 90° stage. In the 11.25° and 22.5° stages, the shunt inductors (L_3, L_4, L_9, L_{10}) in the low-pass T-type networks are small, which are sensitive to loading effects. Therefore, they are located in between 180°, 45° and 90° stages which have a higher input impedance to reduce the influence of loading effects.

Body–source connected NMOS switches: The switches inside the phase shifter are implemented by NMOS transistors. In this technology, the NMOS transistor can be fabricated in a deep *n*-well structure. The equivalent circuit of an NMOS transistor with deep *n*-well technology is shown in Fig. 3. R_{bias} is the biasing resistor. The insertion loss arises from the on-resistor R_{ds}, and the coupling of drain or source nodes through junction capacitor C_{db} or C_{sb} to ground. When the source and body are connected, the insertion loss decreases as the ground path through the substrate is removed. On the other hand, when the switch is turned off, the drain and source are connected directly through C_{db} since the source and body are connected together, which degrades the isolation of the switch. The on-state resistance could be reduced by increasing the size of the transistors, which also introduces a larger junction capacitor resulting in more loss and poorer isolation. Fig. 3 illustrates the simulation results of insertion losses for body–ground connected and body–source connected switches and it is clear that the insertion loss has a 0.5 dB improvement at 60 GHz.



M_1	M_2	14 μm/40 nm	M_9	78 μm/40 nm	L_1	170 pH	L_8	160 pH	C_1	C_2	45 fF
M_3	M_4	14 μm/40 nm	M_{10}	95 μm/40 nm	L_2	120 pH	L_9	L_{10}	20 pH	C_3	C_4	60 fF
M_5	M_{11}	28 μm/40 nm	M_{13}	M_{12}	19 μm/40 nm	L_3	L_4	30 pH		L_{11}	680 pH	C_5	C_6	60 fF
M_6	M_7	41 μm/40 nm	M_{14}	14 μm/40 nm	L_5	330 pH		L_{12}	112 pH			
	M_8	20 μm/40 nm	M_{15}	20 μm/40 nm	L_6	L_7	56 pH		L_{13}	330 pH			

Fig. 1 *Schematic of 5-bit switch-type digital controlled phase shifter*

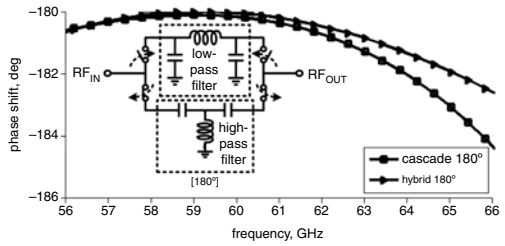


Fig. 2 *Phase difference comparison of 180° stages*

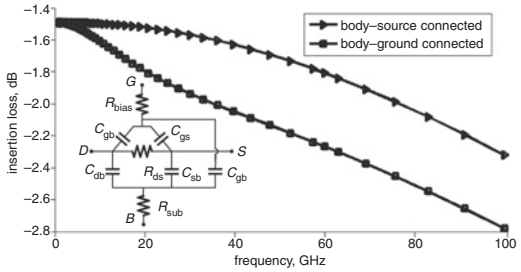


Fig. 3 *Comparison of NMOS transistor with body–source and body–ground connection*

Inductor realisation: The quality factor Q of an inductor could be expressed together with the inductive Q_L and the capacitive Q_C. Q_L represents the magnetic quality factor, which is strongly influenced by the resistive series loss of the inductor. The resistive loss is affected by the intrinsic line resistance, skin and proximity effect, and substrate loss due to eddy current on lossy substrate. To reduce the resistive loss, we could use thicker metal or combine more metal layers to reduce intrinsic metal resistance, increase the distance between turns, or use deep trench to increase the substrate resistivity. Q_C represents the capacitive quality factor, mainly influenced by the capacitive coupling to the substrate. The parasitic capacitance allows the electric fields to penetrate the substrate, which introduces more eddy current.

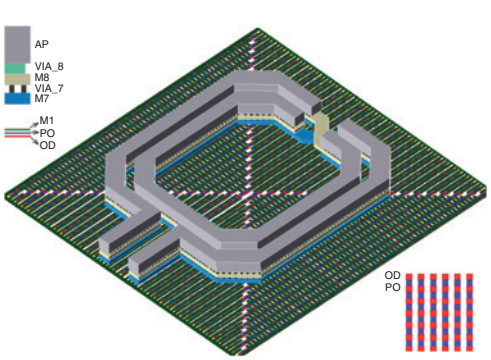


Fig. 4 *On-chip inductor patterned shielding with artificial dialectical EBG structure, and stacked metals method*

In a digital 40 nm CMOS technology without ultra-thick metal, the implemented on-chip inductor is shown in Fig. 4. Metal layers 7 and 8 are combined together with the aluminium layer. Patterned shielding is implemented in metal layer 1. The shielding pattern is implemented by metal slots perpendicular to the current flow on the signal path. In this way, less magnetic and electric field will penetrate into the substrate, alleviating the eddy currents flowing in the substrate. The poly layer and oxide layer form an EBG [5] structure to increase the dielectric constant. The EBG structure can decrease the size of the inductor so as to reduce the loss from the inductor.

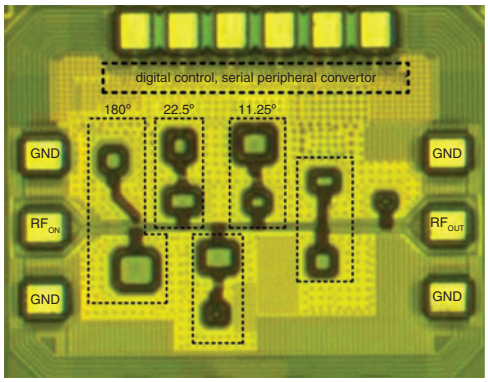


Fig. 5 *Die photograph of 5-bit digital controlled phase shifter*

Measurement results: The chip photograph of the proposed 5-bit switch-type RF phase shifter is shown in Fig. 5 with a circuit area of 0.6×0.4 mm^2.

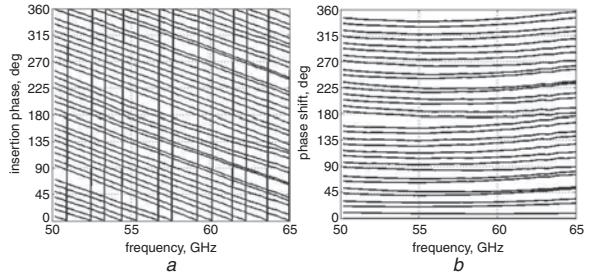


Fig. 6 *Measured insertion phase and relative phase shift of 32 different phase states from 50–65 GHz*

a Measured insertion phase
b Measured relative phase shift

The measured insertion phases of the 32 phase settings are depicted in Fig. 6*a*. The phase step is ~11.25°. Fig. 6*b* highlights the relative phase shifts for 32 phase settings by setting the phase state 00000 as a reference. Derived from the measured insertion phase and gain shifts, Fig. 7 shows the measured RMS phase errors and RMS gain errors of the 32 phase states, giving 5° RMS phase error and 2 dB RMS gain errors at 60 GHz.

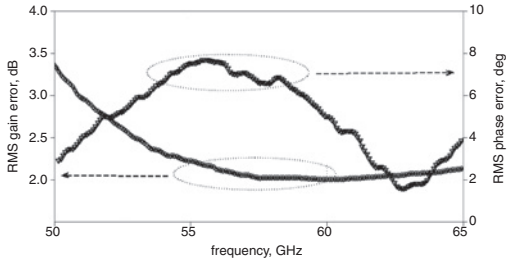


Fig. 7 *Measured RMS phase and gain errors of phase shifter*

Conclusion: This Letter presents a state-of-the-art digitally controlled passive phase shifter with a hybrid 180° stage in 40 nm CMOS technology. The method of body–source connection is applied to decrease the loss from the switches. A patterned shielding with EBG structure, and a stacked metals method are applied to increase the on-chip inductor quality factor. Table 1 summarises the measured circuit performance and compares to recently published RF phase shifters. Compared with the other RF phase shifters, the proposed 5-bit phase shifter has less phase error and less area, while achieving a comparable linearity and loss without ultra-thick metal.

Table 1: Performance summary and comparison

Ref./ technology	[3]/0.18 µm SiGe BiCMOS	[4]/0.13 µm SiGe BiCMOS	[1]/ 65 nm CMOS	[6]/ 90 nm CMOS	This work/ 40 nm CMOS
Frequency (GHz)	40–45	57–64	55–65	57–64	57–65
Phase range (deg)	360	180	360	360	360
Resolution (deg)	n/a	n/a	22.5	11.25	11.25
Max. loss (dB)	12.5	8	16	18	20.9
Loss flatness (dB)	n/a	±1.5	±2	±0.8	±1
Max. phase error (deg)	9	n/a	9.2	10	6.8
Min. phase error (deg)	6.5	n/a	5.5	2	1.5
Gain deviation (dB)	n/a	n/a	n/a	1.8	2
DC power (mW)	40	0	0	0	0
Area (mm^2)	0.11	0.56	0.2	0.34	0.24

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One or more of the Figures in this Letter are available in colour online.

H. Gao, K. Ying, M.K. Matters-Kammerer, P. Harpe, B. Wang and P.G. M. Baltus (*Eindhoven University of Technology, The Netherlands*)

✉ E-mail: H.Gao@tue.nl

W.A. Serdijn (*Delft University of Technology, The Netherlands*)

B. Liu (*Holst Centre, imec, Eindhoven, The Netherlands*)

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