0.75 V micro-power SI memory cell with feedthrough error reduction

C. Sawigun and W.A. Serdijn

A simple technique to realise a switched current memory cell operating from low supply voltage (0.75 V) with clock-feedthough (CFT) error reduction is presented. Unlike previous techniques that try to minimise current error by compensation at the output, this technique prevents the occurrence of current error by removing the feedthrough voltage from the input port of the memory transistor directly. As a result, the CFT error current at the output is almost completely eliminated employing a simple and compact circuit structure. Simulation results are given, showing good agreement to the theory.

Introduction: A switched current (SI) memory is a basic building block for analogue sampled data signal processing that can be implemented in standard digital CMOS processes [1]. The major problem that degrades the accuracy and limits high frequency performances of the memory is feed-through error due to the non-ideal characteristic of a MOS switch [2]. Fig. 1*a* shows a basic first generation SI memory, switch S_1 implemented by a MOS device. After turning off, S_1 injects charge into the gate of memory transistor M_2. This results in an undesired gate voltage fluctuation of M_2 (V_{CFT}) which is consequently transferred into an output current error. Although V_{CFT} depends on the dimensions of the switch, the speed and amplitude of the clock signal and the input current (i_{in}), for simplification, V_{CFT} is usually considered a signal independent parameter. Nevertheless, after calculating the output current using the square-law input-output relation of a MOSFET operating in strong inversion saturation, the result shows that the error current contains both offset and signal-dependent parts [2]. To minimise the error, several techniques have been proposed, most based on generating additional error currents to cancel the original one at the output. Since there are both signal dependent and offset parts, to achieve a complete cancellation (only in theory), complicated circuit and/or clock scheme techniques are unavoidable [2–5]. In this Letter, we change the point of view from trying to compensate for the drain-current error of the memory transistor to reducing the gate-source voltage error of the same transistor so that the current error does not appear at the output.

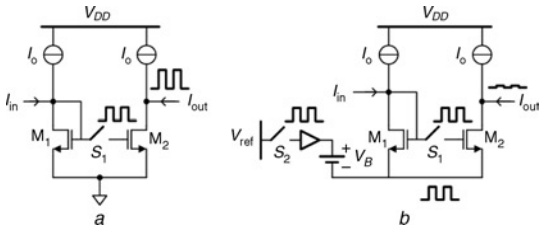

Fig. 1 *First generation SI memories*

a Without error cancellation
b With error cancellation

Voltage-feedthrough cancellation: The proposed cancellation concept can be described through the circuit shown in Fig. 1*b*. In addition to the basic memory, switch S_2, operated during the same clock phase as the main switch S_1, and a voltage follower/level shifter (VF) are added.

In the sampling phase, the source voltages of M_1 and M_2 equal $V_{S1} = V_{S2} = V_{ref} - V_B$ and their gate voltages are also equal due to closed switch S_1. Therefore, under the assumption that the drain voltages of M_1 and M_2 are equal or channel length modulation is negligible, the drain current of M_2 will equal $I_{D2} = (k_2/k_1)\, I_{D1}$, where k_i is the transconductance parameter of both transistors and $I_{D1} = I_o + i_{in}$ is the drain current of M_1. This operation is exactly the same as the basic circuit in Fig. 1*a*.

In the hold phase, while switches S_1 and S_2 are turned off, i.e. open, the charge induced by S_1 will be injected into the gate of M_2, thereby creating a gate voltage $V_{GCFT} + V_{Gsamp}$ and, at the same time, the charge induced by S_2 will be converted into a voltage at the voltage follower input and subsequently be relayed to the source terminal of M_2, thereby creating a voltage $V_{SCFT} + V_{Ssamp}$. V_{GCFT} and V_{SCFT} are the feed-through error voltages at the gate and source terminals, respectively, and V_{Gsamp} and V_{Ssamp} are the voltages at the end of the previous sampling phase at the gate and source terminals, respectively. The resulting gate-source voltage of M_2 during the hold phase becomes

$$V_{GShold} = V_{GSCFT} + V_{GSsamp} \tag{1}$$

In the case of identical switches, identical gate-source capacitances of M_2 and of the MOS transistor used in the voltage follower, and when the input current is small with respect to the bias current, the V_{GSCFT} can become nearly zero. It should be noted that, in practice, switches and capacitances can be matched relatively well and the former requirements are readily met. However, it is not worth keeping the input current very small. In fact, the opposite is true, we require a large input current for large signal-to-noise ratio. Variation of input signal amplitude induces variation of V_{GCFT}, while V_{SCFT} is kept constant because S_2 is connected to a constant V_{ref}. Therefore complete error cancellation can never be accomplished. However, large amounts of current error can be successfully reduced by this technique.

Low-voltage micro-power SI memory: Fig. 2 shows the proposed SI memory circuit. Since the circuit is designed to be implemented in a 0.13 μm *n*-well process, to avoid the body effect, *P*-channel devices are used for the memory core ($M_1 - M_2$) and the voltage follower/level shifter ($M_3 - M_4$). To bias all transistors to operate in strong inversion saturation, at least

$$V_{DD} = |V_{tp}| + V_{effo} + V_{eff1-3} + V_{eff4} \tag{2}$$

is required for voltage supply, where V_{tp} is a threshold voltage of the PMOS, V_{effo} is the minimum voltage required by current source I_o and V_{effi} is an effective voltage of each transistor. Setting V_{ref} to be equal to V_{effo}, the switch gate-source overdrive voltage becomes $|V_{tp}| + V_{eff1-3} + V_{eff4}$, which is large enough to turn on the NMOS switches ($M_{S1} - M_{S2}$). Since for this technology the threshold voltages of *N* and *P* channel devices are found to be $V_{tn} \cong -V_{tp} \cong 0.3$ V, for low current operation, a supply voltage $V_{DD} = 0.75$ V is sufficient.

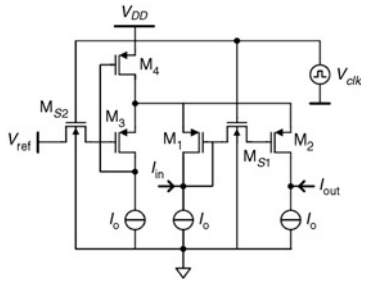

Fig. 2 *Low voltage SI memory with error cancellation*

Trying to minimise and equalise the charge injection, dimensions of M_{S1} and M_{S2} are set to be minimal and identical (150 nm/130 nm, in this case). The voltage follower/level shifter is formed by a flipped voltage follower [6], comprising M_3 and M_4, also biased by I_o. The impedance at the source terminal of M_3 is very low. M_1 and M_2 are equally sized to M_3 so that their gate-source capacitances are identical and consequently $V_{GCFT2} \simeq V_{GCFT3}$. Consequently, $V_{GSCFT2} \simeq 0$, resulting in no current error at the output.

Simulation results: To verify the proposed concept, the SI memory in Fig. 2 was simulated in Cadence using RF Spectre. Transistor width (W) and length (L) were set as $W/L_{1-3} = 1$ μm/1 μm and $W/L_4 = 2$ μm/0.13 μm. Supply voltage $V_{DD} = 0.75$ V, reference voltage $V_{ref} = 0.2$ V and bias current $I_o = 1$ μA. The quiescent power consumption equals 2.25 μW.

Fig. 3 shows the transient response of the memory employed as a track and hold circuit for a 0.8 μA, 200 kHz, sinusoidal input current (modulation index = 0.8) and 2MS/s sampling rate. The dotted line represents the output current of the memory without switch M_{S2} (i.e. the gate of M_3 connected to V_{ref}, directly) and the black solid line shows the output of the memory with the compensation switch. The grey line is the input. It can be seen that without M_{S2} the maximum current error occurs at the positive peak of the output signal and that the error is almost completely cancelled by inserting M_{S2}.

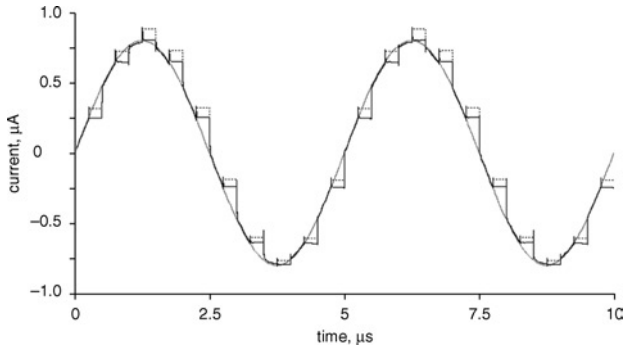

Fig. 3 *Transient response of track and hold circuit*

To estimate the error at different input signal amplitudes, the maximum errors at the peak of the output signal were collected and plotted against the input modulation index in Fig. 4*a*. Without M_{S2}, the maximum current errors were larger than 65 nA and increase with input amplitude. After insertion of M_{S2}, the errors are suppressed and remain lower than 4 nA and almost constant. Fig. 4*b* shows how much of the errors (in per cent) have been removed by inserting M_{S2}. The graph reveals that using this technique more than 94% of the feedthrough error can be removed.

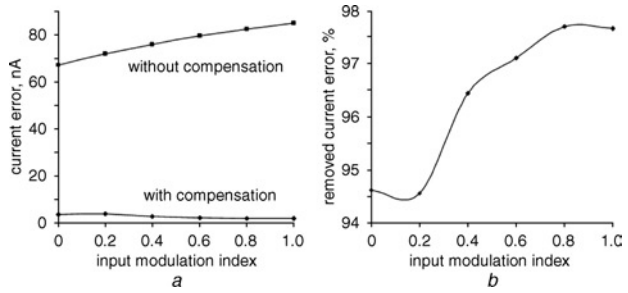

Fig. 4 *Error against modulation index*

a Output current errors of circuit in Fig. 2 with and without switches M_{S2}
b Percentage of removal error

Conclusion: A simple circuit technique to realise a compact low-voltage, micro-power, high accuracy SI memory is presented. Simulation results confirm that the proposed circuit successfully rejects a large percentage of the output current error. Therefore, the proposed circuit can be considered an effective building block for low-power, high-accuracy, analogue sampled data signal processing.

14 March 2008
Electronics Letters online no: 20080722
doi: 10.1049/el:20080722

C. Sawigun and W.A. Serdijn (*Biomedical Electronics Research Group, Electronics Research Laboratory, Delft University of Technology, The Netherlands*)

E-mail: chutham12345@yahoo.com

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