GaAs 0.5 dB NF dual-loop negative-feedback broadband low-noise amplifier IC

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A GaAs dual-loop negative-feedback low-noise amplifier (LNA) designed for the square kilometre array is presented. Effects of transformer non-idealities on LNA performance are discussed. The LNA has 0.5 dB noise figure and −10 dB input return loss from 0.6 to 1.6 GHz.

Introduction: ASTRON, The Netherlands Foundation for Research in Astronomy, is currently developing a new radio telescope that is 100 times more sensitive than the best telescope to date. This high sensitivity is obtained by increasing the collecting area to approximately one square kilometre. This square kilometre array (SKA) [1] employs approximately 100 million antennas that are connected in a phased array, forming one large antenna. Besides a large collecting area, a very low-noise amplifier (LNA) (NF = 0.5 dB) in the frequency range 0.6–1.6 GHz is needed.

To achieve a broad bandwidth, a dual-loop negative feedback topology is favourable because of the possibility of accurately defining the input impedance [2]. This Letter presents a power-to-power (i.e. having accurate input and output impedances) dual-loop negative feedback LNA with a transformer in one of the loops. The topology allows for separate (orthogonal) noise matching and impedance matching. The design procedure takes into account the influence of transformer non-idealities on the noise and impedance performance of the LNA. The complete schematic of the LNA is provided along with its simulation results.

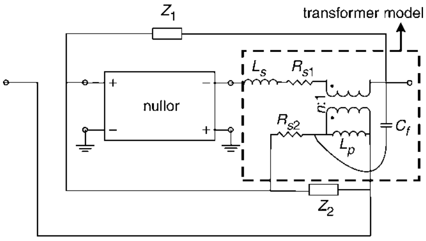

Fig. 1 *Power-to-power amplifier topology with transformer model*

LNA design: Fig. 1 shows the power-to-power dual-loop negative feedback topology with the transformer model [3, 4] and a nullor as the active part. The nullor is a high-gain block with all the transfer parameters infinite. L_s is the series inductance of the primary winding of the transformer. L_p is the parallel inductance of the secondary winding. R_{s1} and R_{s2} are parasitic series resistances. C_f models the parasitic capacitance between the windings. The substrate loss can be considered negligible due to the high resistivity of GaAs substrate. All the impedances in the Figure, Z_1, Z_2, R_{s1} and R_{s2} have series noise sources, which can be transformed to the input of the LNA to analyse the noise performance. Ignoring parasitic capacitance C_f for the moment, the input equivalent noise power spectral density (in V2/rad/s) is given by

$$S_{Vn,eq,in}(\omega) = 4kT\frac{\omega^2L_p^2(2R_2-R_S)^2/R_1+(R_2^2+\omega^2L_p^2)R_2+R_2^2R_{S2}}{\omega^2L_p^2} \qquad (1)$$

where R_s, R_1 and R_2 are the source resistance and the real parts of Z_1 and Z_2, respectively. Apart from a pole in the origin, $S_{Vn,eq,in}(\omega)$ also has a zero:

$$\omega_{zero} = -\frac{\sqrt{R_2^2(R_{S2}+R_2)/R_2+(2R_2-R_s)^2/R_1}}{Lp} = -\frac{R'}{Lp} \qquad (2)$$

The frequency response of the noise is illustrated in Fig. 2*a*. To achieve low noise, R_1 and R_2 are in the order of 1 kΩ and 1 Ω, respectively. For a source impedance R_s of 50 Ω, R_{s2} of about 10 Ω, and L_p being several nanohenries, the zero is located below 400 MHz, which means that the noise figure remains low in the frequency band from 600 MHz.

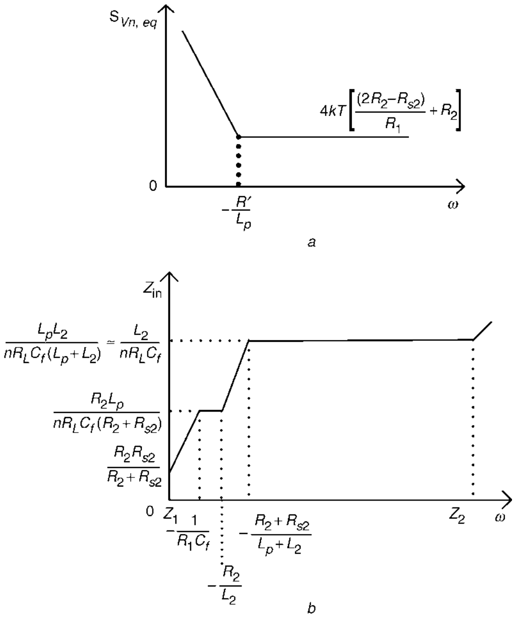

Fig. 2 *Frequency response*

a Frequency response of noise performance
b Frequency response of input impedance

When designing the input impedance, the parasitic capacitance of the transformer needs to be considered. C_f shown in Fig. 1 models the effective parasitic capacitance in the feedback loop originating mainly from the port-to-port capacitance and which introduces a pole and a zero in the frequency response of the input impedance (Z_{in}). This pole narrows the band of Z_{in} to several hundreds of megahertz. To broaden the bandwidth, Z_2 is made inductive. As a result, the input impedance becomes

$$Z_{in} = \frac{(R_2+SL_2)(1+n)R_LL_pC_fR_1(S+\omega_{zero1})(S+\omega_{zero2})}{nR_L(SL_p+R_2SL_2+R_{s2})(1+SR_1C_f)} \qquad (3)$$

where R_L is the load impedance:

$$\omega_{zero1} \simeq 0 \qquad (4)$$

$$\omega_{zero2} = -\frac{1}{n+1}\left[\frac{1}{R_LC_f}+\frac{nR_{s2}}{L_p}\right] \qquad (5)$$

The frequency response of Z_{in} is shown in Fig. 2*b*. It can be estimated that the frequency band is wide enough because the zero at $-R_2/L_2$ cancels one of the poles.

The complete schematic of the LNA, including the biasing circuitry, is shown in Fig. 3. The circuit inside the frame is integrated on chip. All five transistors adopted in the circuit are *p*-HEMTs. Three stages in the active part provide enough loop gain and ensure the accuracy of gain, input impedance and linearity. The first stage is composed of three parallel transistors, which makes the optimum source impedance for noise (Z_{opt}) close to 50 Ω. The inductor in the source lead of the third stage stabilises the LNA at high frequencies, and the input circuitry with the 47 nH off-chip inductor ensures stability of the LNA at low frequencies.

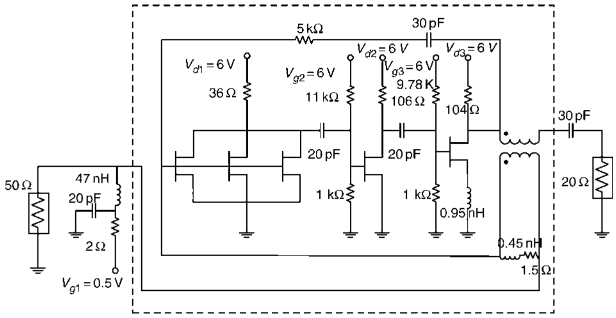

Fig. 3 *Complete schematic of LNA*

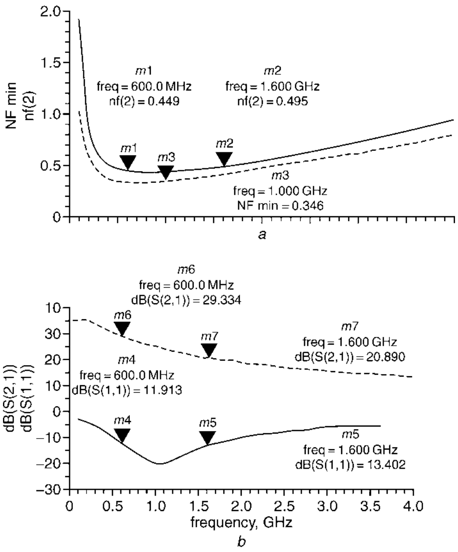

Fig. 4 *Simulation results*

a Simulation results of noise figure
——— noise figure
– – – – – $\mathrm{NF}_{\min}$
b Simulation results of *S*-parameters
——— dB(S_{11})
– – – – – dB(S_{21})

Simulation results: The LNA is to be fabricated in the 0.2 μm GaAs process of OMMIC, Philips. The process provides *p*-HEMTs with cutoff frequencies around 60 GHz and minimum gate length of 0.2 μm. The resistivity of the substrate is $>10^7\ \Omega$ cm. The transformer was designed by Momentum in ADS. The die area amounts to 1.5×1 mm. Because the manufacturer provides all the models of real elements, including the transmission lines and bends for connection, the simulation results provide a good prediction of the actual performance. Fig. 4 shows the simulation results of the LNA. The noise figure is smaller than 0.5 dB in the band 0.6 –1.6 GHz. The simulation of stability was made from 10 Hz to 100 GHz. The stability circles, together with the input and output reflection coefficient, show that the LNA is stable. Some important results are compared with the specifications in Table 1.

Table 1: Summary of simulation results

Parameters	Required specifications				Simulation results
	Min	Typ	Max	Unit	
Power consumption			1	W	0.852 W
Power gain		10		dB	20.9 dB
Noise figure			0.5	dB	0.495 dB
Output IP3	15			dBm	15.4 dBm
Input reflection coefficient			−10	dB	Smaller than −11.9 dB

Conclusions: A GaAs dual-loop negative feedback LNA has been presented. The LNA takes advantage of the dual-loop topology to independently optimise the noise and impedance matching, resulting in a low-noise broadband amplifier. The effects of transformer non-idealities on the LNA performance have been analysed and counteracted. Simulation results show that the LNA has 0.5 dB NF and −11 dB S_{11} from 0.6 to 1.6 GHz.

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