Compact nA/V triode-MOSFET transconductor

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A simple nA/V CMOS transconductor for low-frequency g_m-C filters is presented. To benefit from the lowest g_m/I_D ratio, input transistors operate in the triode region, with g_m adjusted by their (W/L) and V_{DS}, the latter a tuning-voltage replica. Since V_{DS} surmounts the equivalent noise of the replica circuit, excellent control of g_m is attained. Simulations support theoretical analysis. A 5Hz bandpass filter was designed, featuring SNR = 59.2 dB for THD < 1% at 150 mV and 17 nW consumption.

Introduction: On-chip realisations of large time constants are often required to design very low cutoff-frequency continuous-time filters in applications such as integrated sensors, biosignal amplifiers and neural networks. Owing to their low-voltage low-power (LVLP) compatibility, g_m-C structures are a natural choice to perform the desired filtering. However, to limit capacitors to practicable size, g_m values in the range of a few nA/V are typically needed.

Previous LVLP CMOS techniques to obtain such a very low g_m essentially combine different strategies of voltage attenuation, source degeneration and current splitting. The intrinsic attenuating properties of floating-gate and bulk-driven techniques are exploited in [1]. The latter solution implies in a finite input-impedance transconductor and lack of precision, as the bulk transconductance g_{mb} is very process-dependent. In the source-degeneration scheme presented in [2], a triode-biased transistor simply mimics a voltage-controlled resistor. Matching is a crucial problem in current splitting, since a large number of unity-cell transistors compose the current mirrors to implement very high division factors [3, 4].

In this Letter we discuss the advantages of a strong-inversion triode (SI-TR) transconductor in designing g_m-C filters in the hertz and sub-hertz range. Contrary to previous approaches, g_m is now controlled by a voltage rather than by a current. In an SI-TR MOSFET, by connecting the source terminal to one of the supply rails, a control voltage applied to the drain linearly adjusts g_m. Since (W/L) offers a degree of freedom in size g_m, V_{DS} values well above the equivalent noise of the replica circuit can be imposed. Consequently, filters with more predictable frequency characteristics can be implemented.

Transconductor description: The g_m/I_D ratio is listed in Table 1, for distinct MOSFET regions: SI-TR, weak-inversion saturation (WI-S) and strong-inversion saturation (SI-S). The gate-overdrive voltage is $V_{GO} = V_{GS} - V_{TO}$, where V_{TO} is the threshold voltage. U_T and n are the thermal voltage and the weak-inversion slope factor, respectively. As it can be noted, for a source-grounded device and V_{DS} small, the lowest g_m/I_D occurs for SI-TR operation, as V_{GO} can be set much higher than nU_T.

Table 1: g_m/I_D and N_{ID} ratios in different operation regions

	WI-S	SI-TR	SI-S
g_m/I_D	$1/nU_T$	$1/V_{GO} - (nV_{DS}/2)$	$2/V_{GO} - nV_s$

For a given g_m, the current level in WI-S may easily become one order of magnitude lower than the one in SI-TR. Although WI-S operation reduces power consumption, the I_D required to obtain g_m in the nA/V interval is bounded by the junction leakage and its variation with temperature. Therefore, generating such a very low current reliably is difficult to achieve.

The proposed compact triode transconductor is depicted in Fig. 1. Input transistors M_{1A}-M_{1B} have their drain voltages regulated by an auxiliary amplifier that comprises M_{2A}-M_{2B}, M_{3A}-M_{3B} and bias current sources M_{5A}-M_{5B}, while M_{4A}-M_{4B} provides the single-ended output. The gate-voltage of M_{2A}-M_{2B} is set to $V_C = V_{TUNE} - |V_{GS2}|$, whereas V_B imposes a bias current I_B through M_{5A}-M_{5B}. Both voltages V_B and V_C are derived from the bias generator. Referring V_{TUNE} to V_{DD}, denoting $\beta_1 = (W/L)_1 \mu_p C_{ox}$ and assuming transistors pair-wise matched, the transconductance of the entire circuit is

$$g_m = g_{m1} = \beta_1 V_{TUNE} \quad (1)$$

P-type input-transistors were chosen owing to lower mobility and 1/f-noise coefficients compared to similar parameters of n-MOSFETs. Except for M_{1A}-M_{1B} that stay in SI-TR, remaining devices work in WI-S.

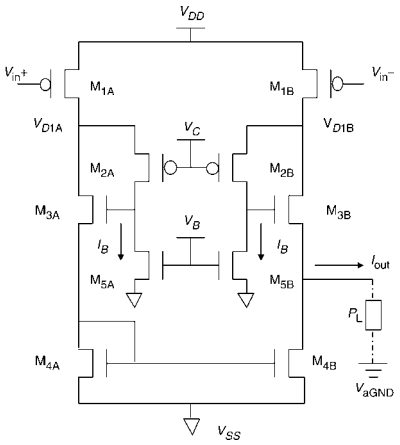

Fig. 1 *Compact triode transconductor*

Bias generator: Bias voltages V_B and V_C are derived from the circuit shown in Fig. 2. The generator is structurally like the transconductor, with M_{1G}, M_{2G} and M_{3G} ideally matched to their counterparts. A servo-amplifier (SA) regulates M_{1G} drain voltage to external voltage V_{TUNE}, so that $V_C \cong V_{TUNE} - |V_{GS2G}|$. Since $V_{GS2G} = V_{GS2A} = V_{GS2B}$, the expected value of V_C is achieved. Properly setting the current gain B (B > 1) in M_{4G}-M_{5G} ensures class-A operation of the transconductor, while tracking down parameter variations on M_{1A} (M_{1B}).

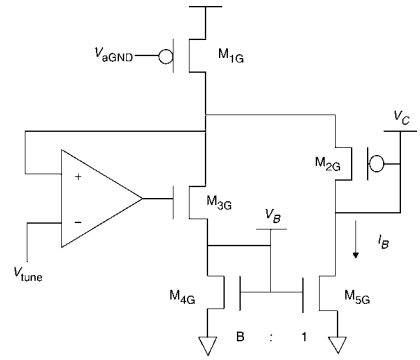

Fig. 2 *Bias generator*

Transconductor and filter design: An SI-TR transconductor was designed and used as a building part in a gyrator-capacitor bandpass filter. The design complies with $V_{DD} = 1.5$ V and a standard 0.35 µm n-well CMOS process, with typical parameters $V_{THN} = 0.50$ V, $V_{THP} = -0.60$ V, $\gamma_n = 0.58$ V$^{1/2}$, $\gamma_p = 0.45$ V$^{1/2}$, $\mu_n = 403$ cm^2/Vs, $\mu_p = 129$ cm^2/Vs and $C_{ox} = 446$ nF/cm^2.

For $10\text{ mV} \le V_{TUNE} \le 50\text{ mV}$, it turns out $1.1\text{ nA/V} \le g_{m1} \le 5.5\text{ nA/V}$. Optimal V_{AGND} is 0.6 V, which limits the signal amplitude to 185 mV. Transistor dimensions (in µm/µm) are $(W/L)_1 = (1.2/600)$, $(W/L)_2 = (10/100)$, $(W/L)_3 = (12/2.4)$ and $(W/L)_4 = (W/L)_5 = (40/40)$. Such a sizing trades-off 1/f-noise and layout area. At nominal $V_{TUNE} = 20$ mV, the calculated g_{m1} and common-mode current I_{D1CM} are 2.2 nA/V and 0.63 nA, respectively. A lossless integrator with $C_{LOAD} = 60$ pF has a unity-gain frequency f_{int} of 5.8 Hz. Setting B = 1.5 results in $I_B \cong 0.25$ nA, a good compromise between signal swing, 1/f-noise of M_{2A}-M_{2B} and M_{5A}-M_{5B}, thermal noise and power consumption in the auxiliary amplifier.

Assuming identical transconductors with $g_{m1} = 2.2$ nA/V in the bandpass filter, the calculated centre frequency f_c is 5.8 Hz. Owing to the large M_1 gate-area, the integrating capacitors should account for the transconductor input capacitance C_{in}. For an SI-TR MOSFET, $C_{GS} = C_{GD} = (1/2)WLC_{ox}$, and, since $|\alpha 1| \ll 1$, the Miller effect can be neglected, yielding $C_{in} \cong W_1 L_1 C_{ox}$. Since V_{TUNE} is shared by all stages, a single bias-generator circuit can be used.

Simulation results: Simulations were carried out using PSPICE 9.2 and Bsim3v3 models. The basic integrator exhibits $f_{int} = 5.0$ Hz and an excess phase of 0.6°, which indicates that the phase error is due to stray capacitances rather than to a finite r_{out}. The transconductor equivalent noise voltage for a 100 mHz–10 Hz bandwidth is 260 μV_{RMS}. Similarly, the input-referred noise of the V_C generator is 42 μV_{RMS}, so that for the lowest V_{TUNE} of 10 mV, a tuning-to-noise ratio (TNR) of 47 dB is obtained. Given that transistor geometries are well defined in modern fabrication processes, g_m can be controlled to a good extent, as it relies only on $(W/L)_1$ and V_{TUNE}.

The frequency response of the filter against V_{TUNE} is shown in Fig. 3. For 10 mV $\leq V_{TUNE} \leq$ 50 mV, one has 2.46 Hz $\leq f_c \leq$ 13.2 Hz. A linear control of f_c by V_{TUNE} is observed, at a rate of 0.27 Hz/mV. For comparison, the calculated f_c range and tuning rate are 2.9 Hz $\leq f_c \leq$ 14.5 Hz and 0.30 Hz/mV, respectively. The filter maximum stand-by consumption is as low as 17 nW.

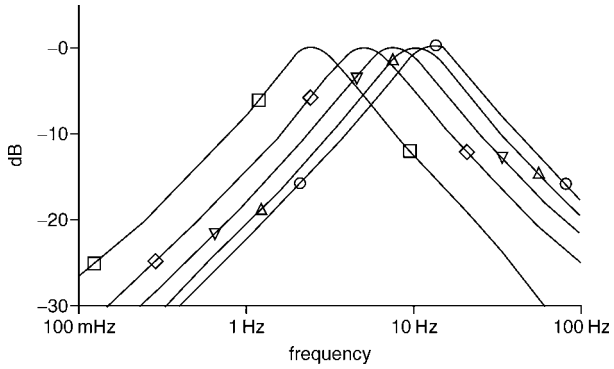

Fig. 3 *Frequency response of bandpass filter against tuning voltage*

At nominal tuning, the in-band equivalent noise is 116 μV_{RMS}. Large-signal distortion corresponds to THD = 1% for an amplitude of 150 mV, so that an SNR of 59.2 dB is attained. Since HD2 dominates, one may assume that a balanced version of the proposed transconductor would present better linearity. Monte-Carlo analysis for a spread of ±0.5% on both (W/L) and V_{TO} parameters on every transistor of the filter revealed that the amplitude should be limited to 137 mV to retain THD ≤ 1%.

Conclusion: A compact CMOS transconductor as a building part for ultra-low power g_m-C filters suitable for operation in the hertz and sub-hertz ranges is proposed. Input transistors are kept in the strong-inversion triode region to profit from the lowest g_m/I_D. Because their drain voltages are regulated to V_{TUNE} by an auxiliary amplifier, g_m scales directly with (W/L) and V_{TUNE}. Such a voltage-controlled approach offers improved accuracy in obtaining g_m values of the order of *nA/V*, as the required I_D can be set well above expected values of leakage current.

A bandpass filter was designed in accordance with $V_{DD} = 1.5$ V and a 0.35 µm *n*-well CMOS process. The tuning voltage V_{TUNE} spans from 10 to 50 mV, yielding 1.1 nA/V $\leq g_m \leq$ 5.5 nA/V. Since the tuning-to-noise ratio equals 47 dB, accurate g_m control is achieved. The filter can be tuned from 2.46 to 13.2 Hz, featuring an SNR of 59.2 dB for THD = 1% at 150 mV peak-value. Maximum stand-by consumption is limited to 17 nW.

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