Syllabic Companding Baseband Switched Capacitor Filter for WLAN 802.11a/g Receivers

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***Abstract*— The IEEE WLAN 802.11a/g standard requires short time interval (5.6μs) for automatic gain control (AGC) convergence during reception of the preamble in each data packet. Due to this stringent settling time requirement, most of the AGC is implemented after the baseband filter, which leads to high power consumption in the baseband filter. In this paper, we present syllabic companding using switched capacitor (SC) ciruits as a solution to achieve gain control in the baseband filter without sacrificing any of the AGC settling time. A 5^{th} order syllabic companding, Chebyshev type, SC filter with a cut-off frequency of 10 MHz is implemented in IBM's 1.2V, 130nm CMOS technology. The filter consumes a total power of 45 mW. It is estimated that companding by a factor of 4 achieves 12 dB improvement in dynamic range and a reduction in power consumption by a factor of 4.3 with respect to conventional filters.**

I. Introduction

Analog baseband filters are one of the key components used in wireless receivers for channel selection, i.e., to reject out-of-band signals before analog-to-digital (A/D) conversion. This relaxes the dynamic range (and therefore resolution) and speed requirements of the A/D converter (ADC), which would otherwise have to oversample the entire input signal containing large interferers. In a given integration technology, the dynamic range of these filters is limited by the supply voltage on the higher side and their input referred noise on the lower side. With the continuous decrease in supply voltage in integrated circuits due to the downscaling of modern digital CMOS technologies, in order to keep the high dynamic range of the filters, one needs to decrease their noise figure. But every 3 dB decrease in the noise power costs double the capacitor area used in the chip and around double the power consumption. An alternate, less expensive, way to accomodate the high dynamic range of the input signal within the low dynamic range of the filters is to use an Automatic Gain Control (AGC) in front of the filter. However, since most wireless receivers are subject to the presence of interferers during minimum desired signal reception, the allowable AGC gain in front of the filter is limited. Therefore, often the AGC operation is distributed throughout the filter, further amplifying the signal as interferers are attenuated [1].

In the IEEE 802.11a/g WLAN system, data transmission is done in packets consisting of preamble, header and data segments [2]. The receiver estimates the channel's characteristics during reception of the preamble. The preamble consists of 10 repetitions of a predefined data stream called a short training symbol (10×0.8μs) and 2 repetitions of a long training symbol (2×4μs). 7 out of 10 short training symbols are used for AGC convergence (5.6μs). Each time a gain setting is changed in front of or within the baseband low pass filter, extra time is needed for filter settling before any further AGC loops can work. Therefore, only limited number of AGC loops (typically one) with coarse gain settings are used before baseband filtering and fine tuning is achieved only after the filter before A/D conversion [3]. This limits the maximum gain that can be achieved in the baseband filter and thus leads to high power consumption. The maximum gain achieved using AGC before the filter is limited by the interferers. Further, the AGC works during the preamble of the data frame and once the gain is set, it remains fixed for rest of the frame. In order to take into account signal variations during rest of the reception, some headroom ($\pm$6 dB) should be given that costs extra power.

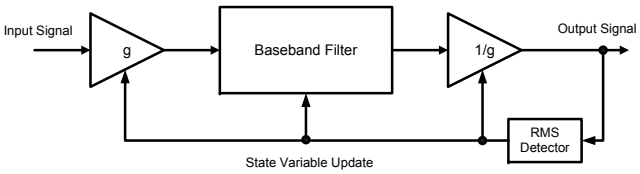

Fig. 1. Syllabic companding baseband filter.

Above mentioned issues can be resolved with the help of syllabic companding [4]. The concept is illustrated in Fig. 1. A syllabic companding filter consists of an input gain (compression) stage with gain g and an output gain (expansion) stage with inverse gain $1/g$. The value of g is adapted according to the signal strength measured at the output, e.g., using RMS detection, as shown in Fig. 1. The output of the filter is used to measure the signal strength because the interferers are highly attenuated at this point and thus a true value of the desired signal strength can be measured accurately. While the gain g is changed to the optimal value, distortion is avoided at the filter output by updating the state variables of the filter as shown at the bottom of the figure [4]. In principle, syllabic companding can be considered a type of AGC in which the gain control works at all times during data processing.

From a practical on-chip implementation point of view, however, companding, being an ELIN system [4], poses several challenges that arise due to process non-idealities. It is often difficult to ensure the accuracy and timing of compression and expansion due to mismatch and process variations in a practical design, which gives rise to distortion [4]. Successful designs have been made using companding in log domain circuits to achieve very high dynamic range filters [5] but circuits in the log domain are mainly intended for very low power, e.g., biomedical applications. Companding in the discrete time domain [4] using Switched Capacitor (SC) circuits [6], on the other hand, offers several advantages. The compression and expansion functions are carried out using an array of switched capacitors. The MiM capacitor mismatch in CMOS technologies is normally less than 0.1%, thus making it possible to use it to compress and expand the signal with high accuracy. The discrete time implementation allows the control block to have sufficient time to transmit the appropriate digital signals to execute gain control and state variable updates.

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In this paper, we present a syllabic companding baseband SC filter with a 5$^{\text{th}}$-order Chebyschev type frequency response, 10 MHz cut-off frequency, 100 MHz clock frequency and companding by a factor of 4 designed for WLAN 802.11a/g applications. Section II briefly describes the receiver architecture and the analog baseband signal chain. Section III explains the operation of the syllabic companding SC filter. Section IV presents a solution for DC offset cancellation, which would otherwise give rise to distortion. Section V presents the simulation results and finally conclusions are drawn in Section VI.

II. Analog Baseband Signal Chain

A direct conversion architecture is assumed for the WLAN receiver, which consists of a bandpass filter, low-noise amplifier (LNA), mixers, AGC loop for RF front-end, low-pass channel-select filters, AGC loop for baseband and ADCs for the I and Q channels. The RF portions of the receiver are assumed to have the following gains: -3 dB for the (off-chip) bandpass filter, 0 or $+20$ dB (selectable) for the LNA and $+10$ dB for the mixers [3]. The entire receiver has a noise figure of 5 dB and the RF front-end is assumed to have a noise figure of 4 dB. After downconversion, an amplifier provides a gain of 10 dB, and is followed by a first order anti-aliasing filter (AAF). A 5^{th} order, Chebyshev type, SC low pass filter is used for channel-selection. The low pass filter has a switchable gain, g in Fig. 1, of 12/6/0 dB at its input stage and an inverse gain of $-12/-6/0$ dB (provided by an expansion amplifier) at its output, respectively. The overall gain of the low-pass filter remains 0 dB. The internal gains are switched using syllabic companding based on the RMS strength of the desired signal measured at the expanded output of the filter. In this way, a low power high dynamic range filter is obtained. The rest of the baseband consists of another AGC loop with voltage gain amplifiers (VGA), to provide fine tuning in the gain settings, and ADCs.

Fig. 2 shows how signal levels vary throughout the receiver chain for a range of desired signal strength and worst case adjacent and alternate-adjacent interferers. The two thresholds at which the gain g changes from 0 to 6 dB and from 6 to 12 dB are -25dBm and -18dBm respectively. It is important to note that the interferers have no effect on the operation of companding. Also, it is assumed that some of the channel-select filtering for the 20 MHz interferer is provided using digital filtering in the DSP to attain the required SNR. A PAPR of 12 dB is assumed and an extra headroom of 6 dB is given on the higher end of the dynamic range of the filter. The input-referred noise of the filter is set at 30nV/$\sqrt{\text{Hz}}$ at maximum gain setting of 12 dB. The first two short training symbols (1.6μs) are used for setting the gain of the LNA [3]. The next five symbols (4μs) are used for the AGC after the filter and also for syllabic companding. Since the timing is quite relaxed, the RMS detection and the control circuit design for the filter is trivial and is not dealt with in this paper.

III. Companding Switched Capacitor Filter Implementation

A ladder type low pass filter has both feedforward and feedback paths between consecutive stages as shown in Fig. 3(a). The figure shows an example of one of the intermediate stages of the filter implemented using a companding discrete SC integrator similar to the one presented in [6]. For simplicity, we assume that all sampling capacitors have a value C_s and the integration capacitor has a value C_I. C_{os} is the opamp's dc offset storing capacitor to cancel the dc offset in integration phase ϕ_2 using Correlated Double Sampling (CDS). The operation of syllabic companding is as follows. Based on RMS detection of the signal at the output of the filter, the control

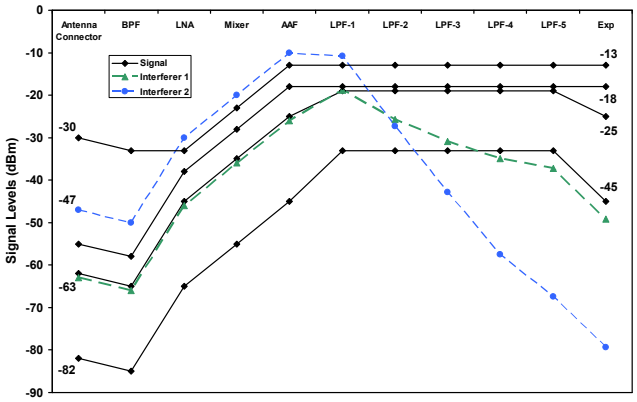


Fig. 2. WLAN 802.11a receiver gain distribution plot for 6 Mb/s rate. Interferer 1 is at 20 MHz and Interferer 2 is at 40 MHz.

block decides whether to increase or decrease the internal gain of the filter (g in Fig. 1) in steps of 6 dB and releases the control signals S_{g1}, S_{g2}, Inc and Dec. Digital signals S_{g1} and S_{g2} are used to switch the gain using an array of sampling capacitors whereas Inc and Dec are used to update the state variables of each stage (double or halve the opamp's output). Fig. 3(b) shows the timing diagram of the control signals with respect to two non-overlapping clock phases ϕ_1 (hold phase) and ϕ_2 (integration phase). The gain switching and updating of state variables for all stages are done during the same phase ϕ_2. In Fig. 3(a), the maximum value of $g_1[n]$ and $g_2[n]$ is 2 and it occurs whenever the gain needs to be increased by 6 dB (Inc goes high). There are two exceptions: for the input stage, the maximum value of $g_1[n]$ is 4 (for a 12 dB gain at the input stage) and for the last stage the maximum value of $g_2[n]$ is 1 (for 0 dB gain in the expansion amplifier). For a Chebyshev type 5$^{\text{th}}$ order low pass ladder filter, $C_I \approx 2.5 \times C_s$ and $C_s \approx 500$ fF designed for an input referred noise of 30nV/$\sqrt{\text{Hz}}$. Using these values, it can be estimated how much power overhead is needed to implement syllabic companding. As an example, for the intermediate stage shown in Fig. 3(a), the feedback factor β_c and the load C_{Lc} in both clock phases ϕ_1 and ϕ_2 are given by

$$\beta_c(\phi_1) = \frac{C_I/2}{(C_I/2 + C_{os})} \quad (1)$$

$$\beta_c(\phi_2) = \frac{C_I}{(C_I + C_s + g_1[n] \cdot C_s)} \quad (2)$$

$$C_{Lc}(\phi_1) = C_I + g_2[n] \cdot C_s + \beta_c \cdot C_{os} \quad (3)$$

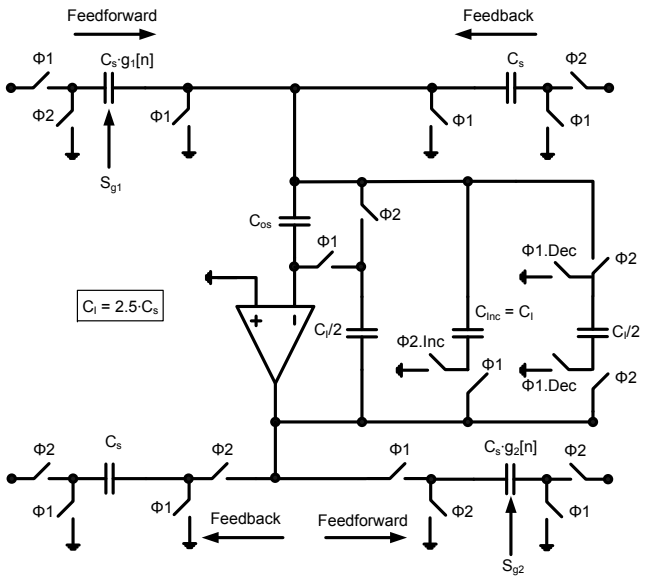
$$C_{Lc}(\phi_2) = C_s + \beta_c \cdot (g_1[n] \cdot C_s + C_s) \quad (4)$$

The capacitive load C_{Lc} during phase ϕ_1 dominates because of the presence of extra capacitance C_I. The feedback factor β of the opamp in negative feedback is kept the same during both clock phases and for different gain settings with the help of dummy capacitors so that the opamps are stable and have the same step response under all conditions. It follows:

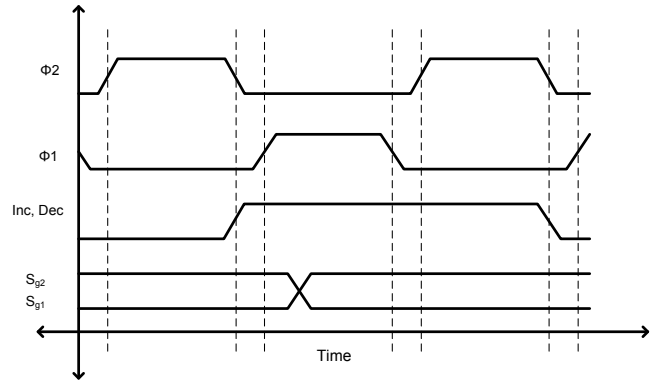
$$\beta_c(\phi_1) = \beta_c(\phi_2) = \beta_c \quad (5)$$

$$C_{os} = (g_1[n] \cdot C_s + C_s)/2 \quad (6)$$

For the non-companding case, when the filter is designed for the same input referred noise as with companding at maximum gain setting



(a)



(b)

Fig. 3. (a) Filter stage using companding SC discrete integrator, (b) Timing diagram for the control signals.

($g = 12$ dB), β_{nc} and C_{Lnc} are given by

$$\beta_{nc} = \frac{C_I}{C_I + 2 \cdot C_s} \quad (7)$$

$$C_{Lnc} = C_s + \beta_{nc} \cdot 2 \cdot C_s \quad (8)$$

A 2-stage miller compensated opamp is used in the filter in order to achieve high DC gain and to handle large output voltage swing. Let the power consumed by the first stage and second stage of the opamp be P_1 and P_2, respectively, for the non-companding case. Note that if β decreases by a factor x and C_L increases by a factor y then the current in the first and second stage of the opamp have to be increased by a factor of x^2 and y, respectively, in order to maintain same noise and settling behavior of the opamp. From above equations, $x^2 \approx 1.5$ and $y \approx 2.5$. Since P_2 is much greater than P_1 due to high capacitive load, the power overhead for each opamp is approx. 2.5 times. The opamp in the expansion stage consumes as much power as other opamps in the non-companding case ($\approx P_2$). Therefore, the power overhead becomes 2.7 times. Ideally, a 12 dB improvement in the dynamic range of the filter should result in 16 times reduction in power consumption. Taking into account the power overhead to implement companding, the syllabic companding results in approx. 5.9 times power savings for a 12 dB improvement in the dynamic range as compared to a conventional filter. There will be extra power consumed by the RMS detector and the control block but because of the relaxed requirements on these circuit blocks, their power consumption is very small as compared to the opamps.

IV. Opamp's DC offset cancellation

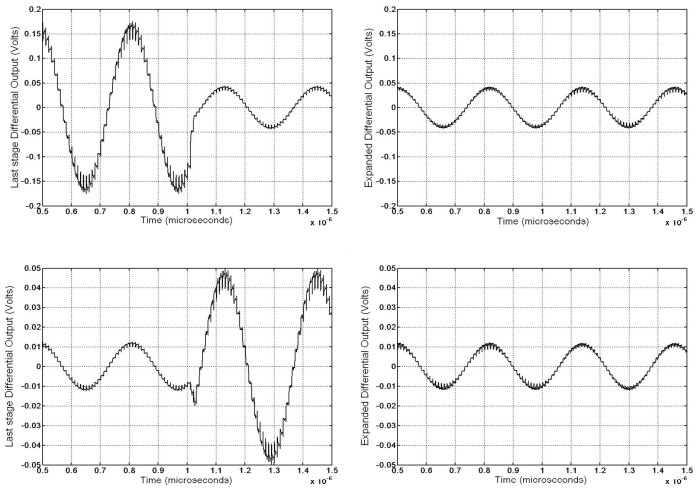
A companding SC filter is an Externally Linear Internally Non-linear (ELIN) system and any spurious signal arising from within the system would be affected by the non-linearity present in the system [4]. In our case, the major unwanted signal is the opamp's DC offset, which gives rise to distortion whenever syllabic companding takes place. Whenever the input is compressed, the opamp's DC offset originating from within the filter gets expanded at the output giving rise to distortion. Since syllabic companding works when the input in-band signals are very weak in strength (around 10mV peak), in order to maintain the required minimum Signal-to-Noise and Distortion Ratio, it is important to reduce the opamp's DC offset to a very low value less than 100μVs.

In a SC ladder type filter, the output of the opamp in each stage is sampled in both clock phases, once for the feedforward path and once for the feedback path (ϕ_1 and ϕ_2 in Fig. 3(a) respectively). Thus, the DC offset of the opamps should be eliminated in both phases. The Correlated Double Sampling technique [7] eliminates the DC offset in the integration phase ϕ_2 by a factor of the DC loop gain of the opamp. In order to get rid of the DC offset in the feedforward path as well, there can be several solutions. One solution is to insert a non-inverting delay element (offset compensated flip around Track and Hold amplifier [7]) that can sample the offset free output in the integration phase and make it available, offset free, in the hold phase for the next stage. This delay element opamp works in almost unity gain feedback configuration and drives the majority of the capacitive load given in Eq. 3 (i.e., $C_I + 2 \cdot C_s$). Therefore, in this new system, each of the integrating opamps and the expanding opamp consume almost as much power as each opamp in the non-companding case whereas the non-inverting delay element consumes 2.5 times more power. Thus, there is an overhead of 3.7 times, which means around 4.3 times power can be saved as compared to a conventional filter for a 12 dB improvement in the dynamic range.

Another solution, which is less taxing on power consumption but more complex, is to use a pair of load capacitors in the feedforward path (in phase ϕ_1). The idea is still to sample the offset free output of the opamp in ϕ_2 but, while one set of capacitors is sampling the output of the opamp in previous stage, the other set transfers the charge sampled in previous ϕ_2 to the next stage. In the next ϕ_2, these two set of capacitors switch their roles. In this implementation, the integrating opamps consume more power because of the increased load. Also, another clock phase is required that runs at half the sampling frequency to switch the two sets of capacitors. In this design, we use the first solution.

V. Simulation Results

The baseband filter for WLAN 802.11a/g receivers is implemented as a 5^{th}-order, 0.1 dB in-band ripple Chebyshev ladder type low pass filter (LPF) using companding SC integrators in IBM's 130nm, 1.2V



(a) (b)

Fig. 4. Single-tone test voltage waveforms at the output of the (a) last stage of the companding filter and, (b) after expansion for two different input signal power strength -18dBm and -26dBm.

CMOS process. The cut-off frequency is fixed at 10 MHz and the sampling clock frequency equals 100 MHz.

The filter is implemented in a differential structure using two stage, miller compensated opamps with a low-frequency loop gain of around 65 dB, a unity gain-bandwidth product of 350 MHz, a phase margin of 73 degrees and a slew rate of 300V/μs. The first stage of the opamp uses a telescopic cascode topology to achieve high DC gain while the second stage is implemented using a simple common source amplifier to handle large output voltage swing. An NMOS transistor, biased in the triode region, is used in series with the miller capacitor to improve the phase margin. The opamp used in the integrators consumes 2.9 mW (2.4 mA) power whereas the opamp used in the non-inverting delay elements consumes 4.1 mW (3.4 mA) power. The opamp used in the expansion block consumes 4.6 mW (3.8 mA) power assuming 3 pF load capacitance. The switches are implemented as CMOS transmission gates using voltage boosted clocks. The filter consumes a total power of 45 mW excluding the power consumed by the RMS detector.

For illustration, Fig. 4(a) and (b) show the differential waveforms of the last stage and at the output of the filter, respectively, in two worst case scenarios - when the gain g changes from 0 to 12 dB and from 12 to 0 dB. Fig. 5 shows the plot of sliding Signal-to-Distortion Ratio (SDR) vs. time for a single-tone test at an input frequency of 3.125 MHz for above two cases. The DFT window is 320ns long and the end point of the DFT is moved from 1μs till 1.5μs in steps of 50ns. Companding starts to take place at 1μs. The opamp's DC offset is assumed to be 10 mV. It can be seen that as companding starts to take place, the SDR dips because of inaccuracy in companding arising from circuit non-idealities. However, it results in a worst case peak distortion of around -57 dBc for a short period of time less than 400ns, which is acceptable for WLAN applications. Therefore, syllabic companding technique is a viable solution to design high dynamic range and low power real time adaptive filters that do not require any AGC convergence time as opposed to conventional filters.

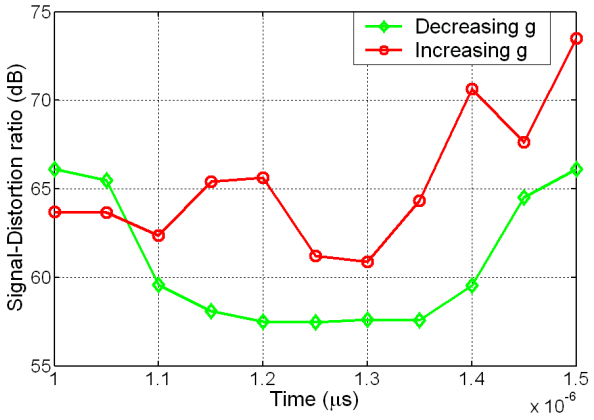


Fig. 5. Signal-to-Distortion Ratio using sliding DFT window of 320ns over a period of 500ns for decreasing gain g (green signal) and increasing g (red line).

VI. Conclusion

A syllabic companding, 5^{th}-order, baseband channel-select low pass SC filter for WLAN applications is presented. For an extra gain of 12 dB in dynamic range, it is estimated that the filter will consume 4.3 times less power than a conventional filter without using conventional AGC. One of the main reasons for distortion is found out to be the opamp's DC offset. Two possible solutions for DC offset cancellation are presented. Results show that worst case distortion peaks to around -57 dBc during gain switching for a short period of time less than 400 ns. The filter consumes a total power of 45 mW.

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