A Nano-Power Class-AB Current Multiplier for Energy-based Action Potential Detector

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***Abstract*— An ultra low-power class-AB four-quadrant current multiplier designed to be used in an energy-based action potential detector is presented. The multiplier is considered the first topology that provides fully class-AB operation. The topology is constituted by a class-AB current amplifier and a current splitter which can handle input signals in excess of ten times the bias current. The proposed circuit operation is based on the exponential characteristic of BJTs or subthreshold MOSFETs. The multiplier is designed using the latter devices and achieves very low power consumption. From a 0.65V supply, simulation results using 0.13µm CMOS model parameters show that the proposed circuit consumes 12.4nW static power while less than −30dB THD is achieved for an input modulation index up to 10.**

I. INTRODUCTION

An action potential or spike detector is an important part of neural recording implants. The detector performs on-chip data reduction by trying to capture only relevant information (real occurrences of the action potential) from the recorded signals. This data selection is indispensable since it helps reducing data rate as well as operating power for wireless data transmission of the neural sensor [1].

To locate the real-time occurrences of action potentials in noisy environments, a 'Nonlinear Energy Operator, (NEO), also called 'Teager Energy Operator, (TEO)' [2] has been widely used to discriminate between the action potentials and the noise in which their energies are considered different [3]. The NEO provides real-time energy of the signals using internal nonlinear dynamical mechanisms described by

$$y(t) = \left(\frac{dx(t)}{dt}\right)^2 - x(t)\frac{d^2x(t)}{dt^2}, \qquad (1)$$

where $x(t)$ represents the incoming signal and $y(t)$ is the output signal representing the energy of $x(t)$. It can be seen from (1) that the NEO algorithm itself is compact since only differentiation, multiplication, and subtraction are required. Therefore, using analog circuits to realize the NEO is being considered in the field of ultra low-power integrated circuit design for implantable devices as can be seen from [4]-[6].

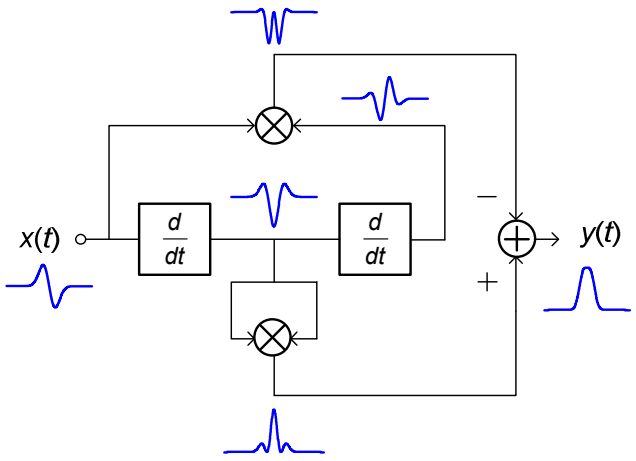

Figure.1 Nonlinear energy operator

Eq.1 can be represented in the form of a block diagram shown in Fig.1. The block diagram comprises two differentiators, two multipliers, and a block for subtraction. The latter operation is simply realized in an analog fashion by representing the signals in term of currents and using a current mirror to perform. So the design challenge is on the differentiators and the analog multipliers.

By the characteristic of the differentiator itself, high frequency components of $x(t)$ will be amplified. An optimization between frequency content of $x(t)$ and circuit time constant, power, and dynamic range, is thus required. For this reason, a G_m-C structure is considered a good candidate and has been employed in [4]-[6].

The output signal from the first differentiator is supplied to both input terminals of the lower multiplier and the second differentiator. The output signal amplitude of the second differentiator, which (for high frequency components) will be amplified again to become even higher, becomes one of the

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input signals for the upper multiplier. Now it is clear that the multiplier for NEO-based spike detector needs to handle a wide range of input signals. To keep the power low and maintain the wide input signal range, class-AB operation, current mode signal processing [7], and weak inversion MOSFETs are considered for the multiplier design.

Based on the well known exponential characteristics of BJTs or weak inversion MOSFETs, four quadrant current multiplier circuits have been designed from different principles, e.g., transconductor/conveyor based [8] and translinear circuit based [9] current multipliers. Most of them are restricted to class-A operation that does not allow the input signals swing to become higher than their bias currents.

In this paper, a fully class-AB four-quadrant analogue current multiplier is presented. The proposed multiplier is formed by a dual output current amplifier which is biased by controlled currents generated from a current splitter. Both the amplifier and splitter circuits can be realized from the same basic circuit block called *Sinh* transconductor which provides class-AB operation. Therefore, fully class-AB multiplication is obtained. Owing to the class-AB operation, the multiplier circuit can be designed to process high input signal amplitudes while its bias current can be kept low. Circuit simulation using 0.13µm model parameter shows that, for a 0.5nA bias current, input currents with amplitudes of 5nA can be applied to the circuit and good four quadrant multiplication is performed.

II. PROPOSED CLASS-AB MULTIPLIER

Fig. 2 shows the block diagram of the proposed multiplier. It comprises three identical current controlled nonlinear transconductors, G_o, G_A and G_B, forming a dual output current amplifier and a class-AB current splitter supplying controlled currents I_A and I_B to the output transconductors of the current amplifier.

For the case that the *I-V* characteristic of each transconductor is a strictly monotonic function, described by

$$I_{\text{out}} = I_o f\left(V_+ - V_-\right), \tag{2}$$

where I_o is a bias current, voltage V_i at the inverting and output nodes of G_o, which is also an input voltage to G_A and G_B can be found to be

$$V_i = f^{-1}\left(\frac{I_{in}}{I_o}\right). \tag{3}$$

Applying (2) to G_A and G_B, we obtain.

$$I_{\text{out1}} = \frac{I_A}{I_o} I_{in} \tag{4a}$$

and

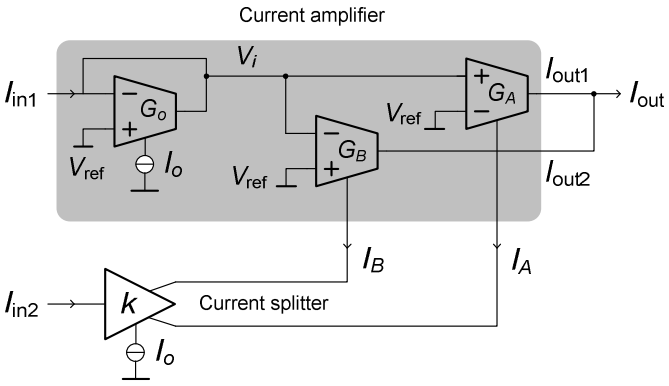

Figure 2. Current multiplier block diagram

$$I_{\text{out2}} = -\frac{I_B}{I_o} I_{in}. \tag{4b}$$

It is clear from (4) that the monotonic function shown on the right side of (2), which, in practice, comes from the nonlinear behavior of semiconductor devices, has disappeared, resulting in linear relationships between input and output currents. Therefore, the output current of the multiplier can be simply found to be

$$I_{\text{out}} = I_{\text{out1}} + I_{\text{out2}} = \frac{I_A - I_B}{I_o} I_{\text{in1}}. \tag{5}$$

Now, we can see that the gain of the amplifier is controlled by the bias current of the input transconductor (connected as a non linear input resistance) and the difference between the bias currents of the output transconductors. In this case, I_o is a constant current but I_A and I_B are generated from another input current, I_{in2}, via the current splitter, according to the following relation

$$I_{\text{in2}} = k\left(I_A - I_B\right). \tag{6}$$

Substituting (6) into (5), we arrive at

$$I_{\text{out}} = \frac{I_{\text{in1}} I_{\text{in2}}}{k I_o} = A \cdot I_{\text{in1}} I_{\text{in2}}. \tag{7}$$

We thus obtain a four-quadrant multiplication from the circuit in Fig.2 with a conversion gain of $A = (kI_o)^{-1}$. This allows us to adjust the gain electronically which helps relaxing the whole system design of the NEO detector.

In CMOS technology, the multiplier can be designed to operate in class-AB at very low power consumption down to a few nW by employing the exponential behavior of subthreshold devices to design the transconductors and the current splitter to be operated from a very low supply voltage (less than 1V) which will be described in the next section.

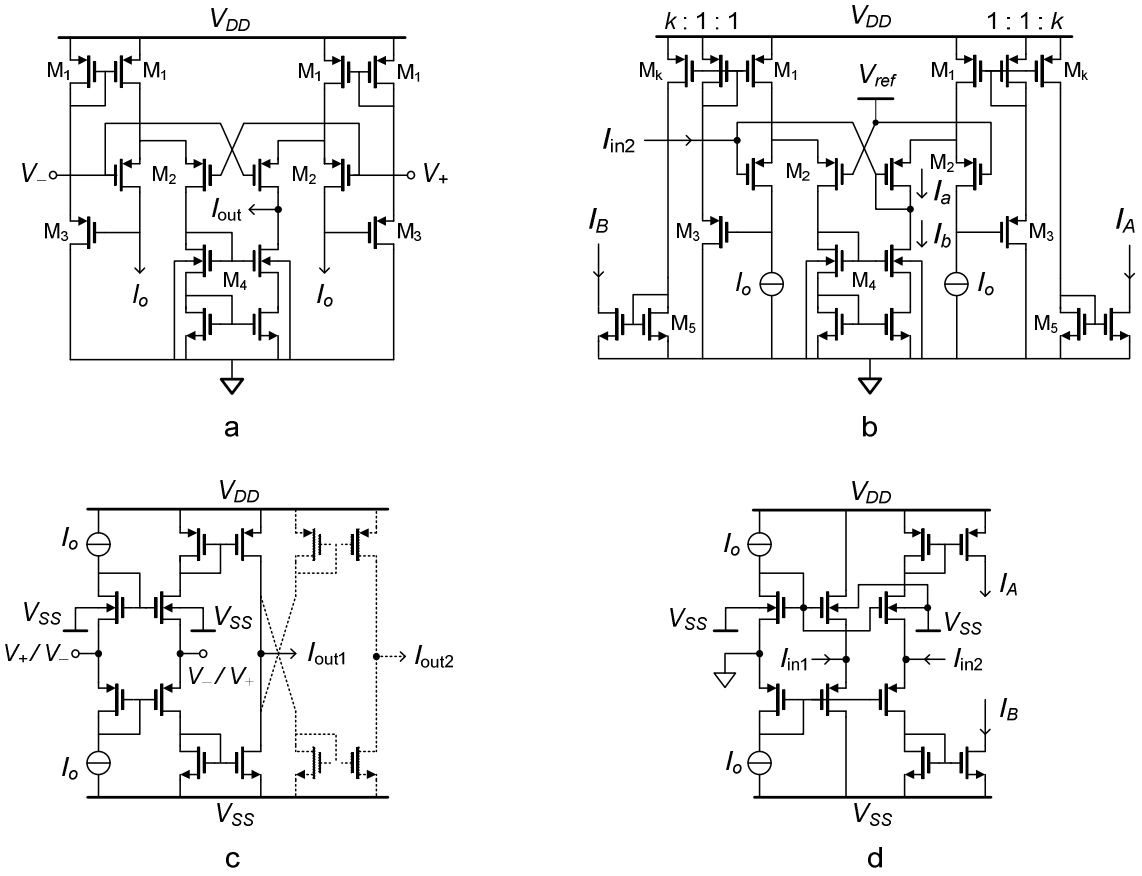

Figure 3. Circuit building blocks

a) *Sinh* transconductor b) *Sinh*-based class-AB current splitter c) Complementary *Sinh* transconductor d) Complementary *Sinh*-based class-AB current splitter

III. CLASS-AB BUILDING BLOCKS

Fig.3a shows the nonlinear class-AB transconductor which can be directly substituted for G_o, G_A and G_B of Fig.2. Using the exponential relationship of MOSFETs operating in weak inversion [10], for $V_{SD} \geq 4U_T$ (a condition to keep the devices in weak inversion saturation) and $V_{SB} = 0$ (source and body terminals are connected), it follows

$$I_D = I_{D0} \exp\left(\frac{V_{SG}}{nU_T}\right), \tag{8}$$

where,

$$I_{D0} = I_S\left(\frac{W}{L}\right) \quad , \tag{9}$$

and I_S is the zero bias current for a unit transistor, n is the sub-threshold slope factor and U_T is the thermal voltage while W, L, V_{SD}, V_{SB}, and V_{SG} have their usual meaning. We can find the input-output relation of each transconductor as

$$I_{\text{out}} = 2I_o \sinh\left(\frac{V_+ - V_-}{nU_T}\right), \tag{10}$$

This relationship complies with (2) and provides class-AB operation.

Based on the same circuit topology, connecting the transconductor in a negative feedback scheme, we obtain the current splitter shown in Fig.3b. Driven by the up-down translinear loop topology formed by a set of transistors M2 and a unity gain cascode current mirror M4, input current I_{in2} which is applied at the inverting input node, is converted into two components, I_a and I_b, under the condition that

$$I_{\text{in2}} = I_a - I_b \tag{11a}$$

and

$$I_o^2 = I_a I_b \,. \tag{11b}$$

Then the split currents (I_a and I_b) are related to bias current I_o and copied by the scaled current mirrors, M1-Mk, and their polarities are reversed again by unity gain current mirrors M5 resulting in I_A and I_B which will be delivered to G_A and G_B, respectively with scaling factor k defined by the dimensions of M1 and Mk.

Another way to design the *Sinh* transconductor and current splitter is shown in Figs. 3c and 3d, respectively. This approach employs complementary devices to implement the

same translinear loop equation and thus suffers from their different subthreshold slopes due to the body effect of the NMOS devices, something which is unavoidable in standard CMOS processes [11]. Hence, we choose the circuits in Figs. 3a and 3b to validate our design.

IV. Simulation Results

The multiplier in Fig.1 was substituted by the circuit blocks in Fig. 2a and 2b and simulated in Cadence using RF Spectre and 0.13µm CMOS model parameters. Transistor widths (W) and lengths (L) are given in Table 1. V_{DD} = 0.65V, V_{ref} = 0.4V, and I_o = 0.5nA. The quiescent power of the entire circuit equals 12.4nW.

The transient response illustrating the four-quadrant multiplication of a 5nA, 2kHz, sinusoidal current I_{in1} (Modulation Index, MI = 10) and a 5nA, 100Hz, sinusoidal current I_{in2} (MI = 10) performed by the proposed multiplier is shown in Fig.4. It is visible that the circuit performs well a multiplication function in the time domain for very high input signal modulation indices.

To examine the circuit linearity, a circuit simulation of the Total Harmonic Distortion (THD) has been performed by varying the amplitude of the 2kHz, sinusoidal I_{in1} from 1nA to 5nA ($2 \leq \text{MI} \leq 10$) and keeping I_{in2} constant at 5nA. The results shown in Fig.4 reveal that at a MI of 10, the proposed multiplier provides ≈ −30dB THD.

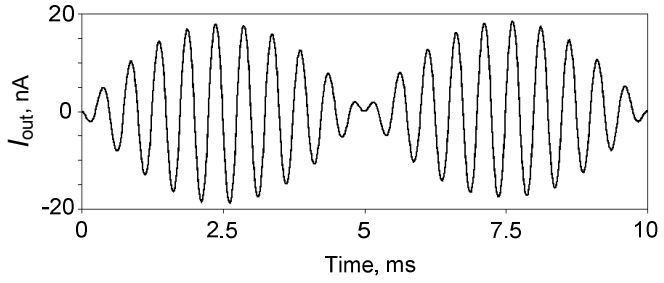

Figure 4. Transient response of the multiplier

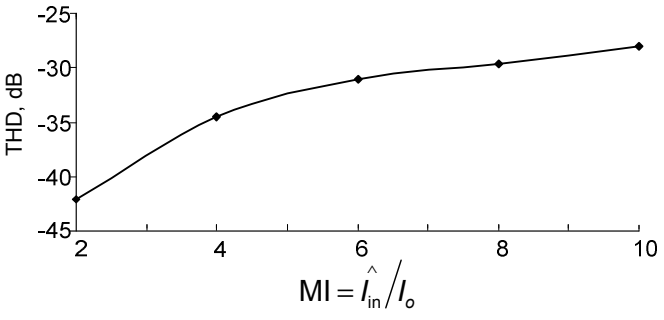

Figure 5. Total harmonic distortion

TABLE I. TRANSISTOR DIMENSIONS

MOSFET	M_1	M_2	M_3	M_4	M_5	M_k
W/L, [µm/ µm]	4/4	1/1	1/10	2/2	2/2	2/4

V. Conclusion

A new low-voltage ultra low-power CMOS four-quadrant current multiplier has been presented. By using a weak inversion *Sinh* transconductor as a basic cell, the first fully class-AB multiplication operation is obtained. This allows the multiplier to process input signals with a modulation index of 10 while the circuit power consumption can be kept very low. This multiplier is suitable not only for realizing NEO-based action potential detector but also for other implantable systems that need to be operated from very low-supply voltage and consume ultra low-power.

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