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A New Current-Mode Synthesis Method for Dynamic Translinear Filters and its Applications in Hearing Instruments

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Abstract. A new current mode synthesis method for dynamic translinear filters is proposed. As a design example, we have considered an ultra-low power second order filter working in audio frequency range, for hearing aids application, and using subthreshold MOS devices. It has a nominal supply voltage of 1.2 V and works down to 1 Volt. It has a power consumption of 5 μW. The filter cut-off frequency and its Q factor can be tuned respectively from 600 Hz to 13 kHz and from 0.6 to 1.1. Mismatch problems are investigated on the circuit level and an on-chip compensation method is proposed.

Key Words: low voltage, low power, filter design, audiofrequency, dynamic translinear, subthreshold MOS, hearing instruments

1. Introduction

The use of ultra-low power and low voltage techniques in hearing aids allows miniaturization of the supply systems and increases their autonomy. However, lowering the supply voltage leads to limitations in voltage swings. Using current mode operations in a filter design doesn't exclude the voltage importance as an information carrying quantity, since the most important function in an integrated filter i.e the integration is effectuated by a capacitance that integrates a current into a voltage. This dual importance of voltage and current in filter processing can be solved in a low voltage environment by operating in a current mode and introducing a non-linear transfer between both quantities so that the voltage swings are much lower than the current swings. Such techniques can make use of the expanding law between voltage and current, present either in the bipolar device or in the subthreshold MOS device and constitute a more general class of dynamic translinear filters or E.S.S. filters. This class was first introduced by Adams [1], and generalized to filters of arbitrary orders by Frey [2]. Recently, it has gained much interest in audio filter applications [3,4] owing to its excellent tunability, its interest for ultra-low power applications since no resistors are necessary and to the fact that it can be designed temperature independent.

Dynamic translinear circuits can be described using voltage as well as current quantities. However, a completely current mode synthesis method of T.L filters fits better with the simplicity of their current mode analysis [5], and can potentially make use of the static translinear circuit theory [6].

Moreover, subthreshold MOS translinear circuits have some fundamental advantages over bipolar translinear circuits. First, they don't suffer from the finite current gain like bipolar devices and they have a low saturated voltage which is more convenient in a low power and low voltage design. Second, unlike the bipolar device, the MOS is a four terminal device, which gives in subthreshold an extra exponential dependency of the drain current and therefore more possible configurations over bipolar realizations. However, one of the limitations of the MOS operating in weak inversion is the current mismatch between identically designed devices due to the process variations [9]. This poor control of the current match causes a number of undesirable effects in the circuit level. Traditionally, several layout techniques

such as making devices large and placing devices close to each other have been proposed for improving the transistors matching. However, it is more accurate and more area efficient to solve the problem on circuit level notably if an on-chip mismatch compensation method can be proposed.

In this paper, we present a general completely current mode synthesis method for dynamic translinear filters. Then a design example employing subthreshold MOS is proposed followed by an investigation of the mismatch effects on the circuit level. In Section 2, an overview of the proposed synthesis method is given. In Section 3, a second order controllable filter design for audio applications is presented. Section 4 is subject of an analysis of the mismatch effects on the circuit level, focusing on a robust on-chip design method to overcome mismatch problems. The full-custom realization and the measurement results of the corresponding design are presented in Section 5. Finally, the conclusion is presented in Section 6.

2. Overview of a Completely Current-Mode Synthesis Method for Dynamic Translinear Filters

2.1. Mathematical Formulation

The synthesis method starts with a variable state representation of the filter differential equation. Such representation has the general form given by

$$\dot{X} = AX + BU \tag{1}$$

$$Y = EX + DU \tag{2}$$

Where the dot indicates time differentiation, $X = (x_1, x_2, \ldots, x_n)$ is a vector of state variables and U and Y are respectively the input and the output currents. Time derivation can be accomplished by the introduction of capacitance currents as illustrated in the general key substructure of dynamic translinear

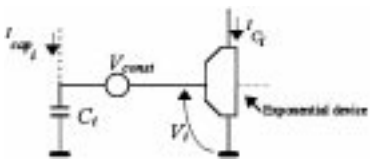

Fig. 1. General key substructure in dynamic translinear circuits.

filters represented in Fig. 1. A general relation describing the exponential device is given by

$$I_{Ci} = Ie^{\frac{V_i}{\alpha V_T}} \tag{3}$$

where I and α are constants depending on the exponential device and V_T is the thermal voltage kT/q. The constant voltage $Vconst$ is added without affecting the 1st order differential equation relating I_{C_i} and $\dot{I}_{C_i}$. It is generally introduced by a buffer of the capacitance voltage in order to avoid any interaction between the different blocks in the design. The capacitance current is found by applying the constitutive relation of the capacitance comprising the derivative of the capacitor node voltage which can be deduced from equation (3) as follows

$$Icapi = \alpha C V_T \frac{\dot{I}_{Ci}}{I_{Ci}} \tag{4}$$

Equation (4) shows that the derivative of a current can be deduced from the product of two currents. The latter can be implemented by means of a static translinear multiplier. This invites a new way of thinking in filter design and signal processors. The basic cell is no longer a linear one. Instead, It can be a multiplier or another cell dealing with current multiplication/division.

Now, taking as state variables the currents I_{Ci}, we get for equations (1) and (2)

$$Icapi \cdot I_{Ci} = \sum_{j=1}^{n} I_{i,j} I_{C_j} + J_i U_i \tag{5}$$

$$Y_i = E_i \cdot I_{Ci} + D_i \cdot U_i \tag{6}$$

for $i = 1, \ldots, n$ where

$$I_{i,j} = \alpha Ci A_{i,j} V_T \tag{7}$$

and

$$J_i = Bi\alpha Ci V_T \tag{8}$$

Equations (7) and (8) reveal the possibility of tuning the A state space matrix elements and those of the B state space vector respectively by adjusting the current sources $I_{i,j}$ and J_i. Such simplicity in tuning the design characteristics is a fundamental advantage of dynamic translinear filters. Moreover, by using P.T.A.T. current sources, temperature independent design characteristics can be achieved.

2.2. *Choice of the Exponential Device in a Subthreshold Environment*

In a saturated subthreshold MOS transistor, the drain current has two exponential dependencies, the first is with respect to its gate to substrate voltage with a process dependent slope factor and the second is relative to its back-gate to source voltage which is almost process independent. A simple model for the drain current of a MOS transistor in saturation is given by

$$I_{DS} = Io\, e^{\frac{V_{GB}}{nV_T}} e^{-\frac{V_{SB}}{V_T}} \tag{9}$$

where Io is the zero bias current, V_{GB} and V_{BS} are respectively the gate-bulk and source-bulk voltages and n is the subthreshold slope factor.

It follows from the above relation that different topologies are possible for the basic exponential device, they are presented in Fig. 2. In Fig. 2(a) and Fig. 2(b), the bulk to source junction can be biased slightly forward causing some leakage current. For high current level, the bulk voltage can increase in a way that the leakage current is no longer negligible relative to the drain current. This leads to a practical exponential range limitation of the drain current estimated to two decades [7]. In Fig. 2(c) and Fig. 2(a), the exponential relation has a slope depending on the MOS subthreshold slope factor which is a function of the applied voltage Vi. Finally, the configuration in Fig. 2(d) is free from the above drawbacks by having grounded bulks and an exponential relation which is independent of the subthreshold slope factor and given by

$$I_{Ci} = Ie^{\left(\frac{V_i}{V_T}\right)} \tag{10}$$

2.3. *Implementation of the Voltage Buffer*

To minimize the interaction between the different blocks and the capacitors in the circuit, voltage buffers are introduced. Consider the implementation of the voltage buffer shown in Fig. 3(a). The variations of the output voltage for this implementation are given by

$$\dot{V}_{\text{out}} = \frac{\dot{V}_{\text{in}}}{n_f} - \frac{\dot{n}_f}{{n_f}^2} V_{\text{in}} \tag{11}$$

where n_f is the sub-threshold slope factor of the transistor Mf. For each particular operation of the filter, the output voltage variations are such that n_f can be considered constant. However when tuning the cut-off frequency of the filter and its Q factor, this assumption is no longer valid. To solve the resultant non-linearity, a balanced configuration based on an up-down compensation is used. The latter is represented in Fig. 3(b).

3. A Design Example: A Tunable Second-Order Low-Pass Filter for Hearing Aids

The above synthesis method is applied to the design of a second-order low-pass filter for audio applications. By using the state space description defined by

$$A = \begin{bmatrix} -\omega_c/Q & \omega_c \\ -\omega_c & 0 \end{bmatrix},\ B = \begin{bmatrix} 0 \\ \omega_c \end{bmatrix},\ E = [1 \quad 0],\ D = 0 \tag{12}$$

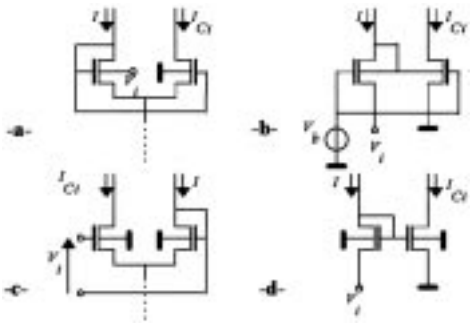

Fig. 2. Possible topologies for the basic exponential device.

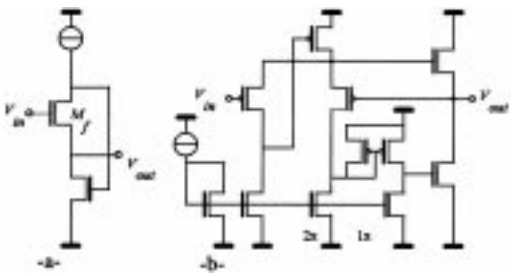

Fig. 3. Voltage buffer (a) simple implementation (b) balanced one.

where $\omega_c = 2\pi f_C$, and f_C is the cut-off frequency of the filter, we thus get to implement the following equations

$$I_{\text{cap}_1} \cdot I_{C_1} = -I_Q \cdot I_{C_1} + I \cdot I_{C_2} \tag{13a}$$

$$I_{\text{cap}_2} \cdot I_{C_2} = -I \cdot I_{C_1} + I \cdot I_{\text{in}} \tag{13b}$$

$$I_{\text{out}} = I_{C_1} \tag{13c}$$

where

$$I_Q = \frac{I}{Q}$$

The relation between the cut-off frequency and the current source I is given by

$$f_C = \frac{I}{2\pi C V_T} \tag{14}$$

In order to implement a multiplication/division of currents, an up-down translinear topology is the only possible topology in a low voltage environment. Thus, we make use in our design of the static translinear loops presented in Fig. 4. By considering successively the loops M2–M5– . . . –M9, M1–M4–M6–M7 and M2–M3–M8–M9, we get easily the following relations between the different currents

$$I_2 \cdot I_{C_2} = I \cdot I_{C_1} \tag{15a}$$

$$I \cdot I_{\text{in}} = I_1 \cdot I_{C_2} \tag{15b}$$

$$I_2 \cdot I_3 = I^2 \tag{15c}$$

where I_1, I_2 and I_3 are respectively the drain currents of transistors M_1, M_2 and M_3. Thus equation (13) come down to the following nodal equations

$$I_{\text{cap}_1} = -I_Q + I_3 \tag{16a}$$

$$I_{\text{cap}_2} = -I_2 + I_1 \tag{16b}$$

$$I_{\text{out}} = I_{C_1} \tag{16c}$$

Moreover, in some nodes such us nodes A and B, the bias voltage level should allow the flow of the needed current sink at these nodes, i.e. by having values above the saturated drain source voltage of a MOS transistor, estimated to few V_T (for example 150 mV). By connecting node C to ground, fulfilling this condition leads to a limitation in the upper signal value, especially for high control currents. Therefore, in order to give a larger room to nodes A and B and allow variations of the input signal over an extended range, node C should be connected to a bias voltage of few V_T. A simple way of generating such a source internally, which costs only the addition of small transistors, is to use a self-cascode [8] in the input and the output levels as represented in the complete design schematic shown in Fig. 5. By writing the drain currents of transistors M_4, M_5, M'_4 and M'_5, and assuming that M'_4 and M'_5 are at the edge of saturation, we get easily the following expression for the voltage V_C

$$V_C = V_T \ln\left(1 + \frac{\beta_1}{\beta_2}\right) \tag{17}$$

where β_1 and β_2 are respectively the transfer parameter $\beta = \mu C_{ox} W/L$ of transistors (M_4, M_5) and (M'_4, M'_5). The generated voltage is then first order independent of the current signal. We also notice from this expression that M'_4 and M'_5 should be as narrow as possible in order to get a sufficient value of v_C, thus v_C is practically modulated by narrow channel effects.

The cut-off frequency can be tuned linearly by varying the control current I according to the relation in equation (14) where the capacitance value C is chosen to be of 100 pF. Moreover, the Q factor, defined as the ratio of the control current I to the current I_Q, can be also tuned by adjusting I_Q. The nominal supply voltage of the design is equal to 1.2 V.

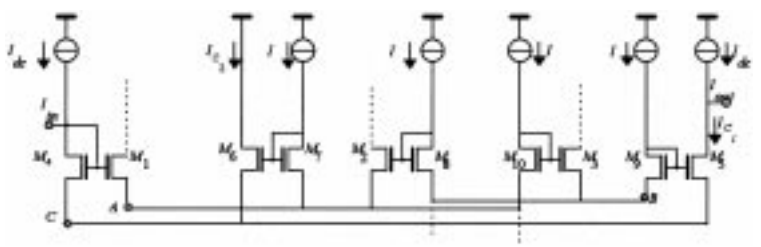

Fig. 4. Basic static translinear loops in the design.

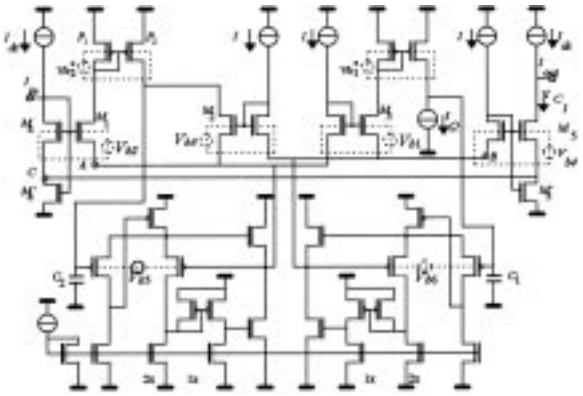

Fig. 5. Schematic diagram of the complete design.

4. Mismatch Investigation

4.1. Mismatch Analysis

Mismatch problems concern all the on-chip devices, but are more significantly affecting transistors in the signal path, which we will consider in our analysis.

A mismatch between two MOS devices can be modeled by a series voltage connected between the gates of both transistors as well as between their back-gates [9,10]. Applying the latter result to our design, the corresponding voltage sources are appended to the circuit represented in Fig. 5. However, it is worth noting that the mismatch between the up and down PMOS transistors of the followers comes down to a shift in their transfer gain, which is equivalent to a deviation in the corresponding capacitance value, let us call them respectively C1 and C2. The analysis of the whole design leads therefore to the following transfer function

$$H(s) = \frac{k_4}{\frac{k_3}{k_2} + \frac{1}{Q\omega_2 k_2 k_1}s + \frac{1}{k_1 k_2 \omega_1 \omega_2}s^2} \tag{18}$$

where

$$k_i = \exp\frac{(n-1)}{nV_T}(vb_i + vb_i^*) \text{ for } i = 1,2 \tag{19a}$$

$$k_i = \exp\frac{(n-1)}{nV_T}(vb_i) \text{ for } i = 3,4 \tag{19b}$$

and

$$\omega_{1,2} = \frac{I}{C_{1,2}V_T} \tag{19c}$$

The new cut-off frequency of the filter and its resonance factor are thus respectively given by

$$f_c^* = f_c \frac{\sqrt{C_1 C_2}}{C}\sqrt{k_1 k_3} \tag{20a}$$

$$Q^* = Q\sqrt{k_1 k_3}\sqrt{\frac{C_2}{C_1}} \tag{20b}$$

The remaining mismatch effect is a shift in the pass-band response which is deviated from a unity value to a new one given by equation (21). Since the input signal is superposed on a DC current, an offset current will appear at the output.

$$A = \frac{k_2 k_4}{k_3} \tag{21}$$

4.2. Mismatch Compensation

According to equation (19), a deviation from the cut-off frequency can be recovered by adjusting the control current I. Similarly, a deviation from the desired filter factor can be surmounted by adjusting the current source I_Q.

Finally, a compensation of the shift in the pass band response can be achieved by an on-chip offset cancellation. We can make use, for this purpose, of a negative feed-back, acting on both transistors P_1 and P_2 (see Fig. 6) back-gates so that the parameter k_2, and then the pass-band response are adjusted (since we are using an N-well technology, the action on k_3 and k_4 is not possible). The schematic diagram of this compensation is represented in Fig. 6. The grounded capacitor C_3 integrates a copy of the output current resulting in a voltage which will be transformed by D1 and D2 into a current that will be integrated by the capacitor C_4. Due to the non-linear characteristics of the diode, a large offset will be reduced very fast because of the corresponding low dynamic resistance

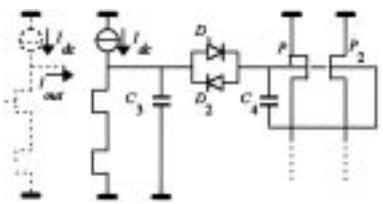

Fig. 6. On-chip offset cancellation scheme.

of the diode. Further, if there is almost no offset, the latter becomes very large so that no distortion of the design transfer function is observed. The back-gate of the PMOS transistor P_2 is connected to a voltage source, slightly below V_{DD}, which gives a certain room for the feed-back action across the capacitor C_4. This voltage is generated using a self-cascode based on the same principle used for the generation of the voltage V_C, but employing a DC current source I_B. The overall matching of the filter relies now on the accuracy of the output current copy. Therefore, we use, only at this level, special layout techniques to match the output and the sensing transistors. The value of the capacitance C3 and C4, needed for the correct operations of the offset compensation, are respectively 200 pF and 20 pF.

5. Full-Custom Implementation and Measurement Results

The second order controllable filter is implemented in the 1.6 μm CMOS process of the Delft Institute for Microelectronics and Submicron Technology (DIMES). A microphotograph of the design full custom realization is shown in Fig. 7. Its total area is about 0.2 mm^2 without including the bias block. All the design measurements are effectuated at a room temperature of 298 K (27°C). Fig. 8 shows the simulated and the measured cut-off frequency vs. the control current I, which can be tuned from 600 Hz to 13 kHz. Further, the Q factor can be tuned from 0.6 to 1.1. Correct operations of the filter can be maintained down to a supply voltage of 1 V.

The DC current ensuring correct class A operations of the filter is fixed to 1.6 μA. The total power consumption is approximately 5 μW. The THD measured at 1 kHz vs. the input current peak value,

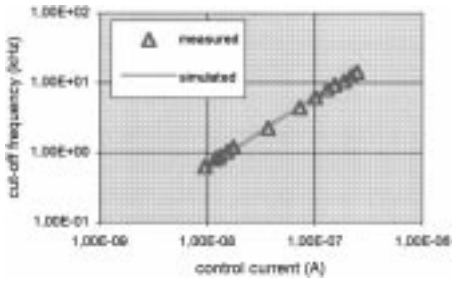

Fig. 8. Measured and simulated cut-off frequencies.

for $I = 210$ nA $(f_c = 13$ kHz) and $I_Q = 300$ nA, is presented in Fig. 9. These measurements show that the filter has a good linearity. The corresponding referred noise floor current is 1.4 nA$_{\text{rms}}$. The resultant D.R. is evaluated to 58 dB. As an example, the measured output spectrum, corresponding to an input current peak value of 1.6 μA using the same settings, is presented in Fig. 10. The corresponding THD is principally due to the second order harmonic and estimated to 1%. Further, the THD of the filter remains below 2% over the tuning range. The performance characteristics of the filter are summarized in Table 1. Moreover, the fact that the measured results agree with the simulated ones without any adjustments of the current sources, let us conclude that the considered process doesn't suffer from any serious mismatch problems. Therefore, the use of the mismatch compensation for such process can be saved to very high accuracy design performances.

6. Conclusion

We have proposed a completely current mode state space synthesis method for dynamic translinear filters

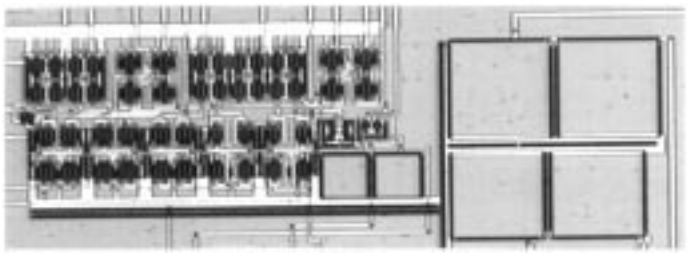

Fig. 7. A microphotograph of the design full-custom realization.

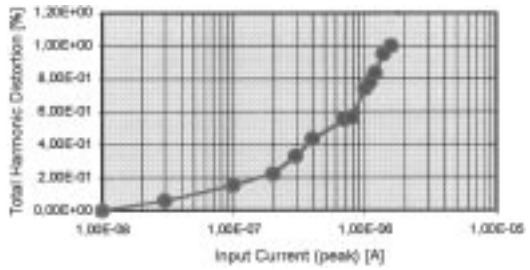

Fig. 9. Measured total harmonic distortion [%] for a 1-kHz sine wave input signal and a control current $I = 210\,\text{nA}$ ($f_c = 13\,\text{kHz}$).

that doesn't need high computational efforts. As an application, we have looked at ultra-low power design working in audio frequency range and using sub-threshold MOS devices. Mismatch errors were investigated on the circuit level and an on-chip mismatch compensation method was proposed.

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Table 1. Performance characteristics of the filter.

Technology	1.6 μm CMOS Process
Active area	0.2 mm^2
Supply voltage	1.6 V–1 V (nominal = 1.2 V)
Turning range	600–13 kHz
Turning current	9.1 nA–210 nA
Q factor	0.6-1.1
Dynamic range	57 dB (THD < 2%)

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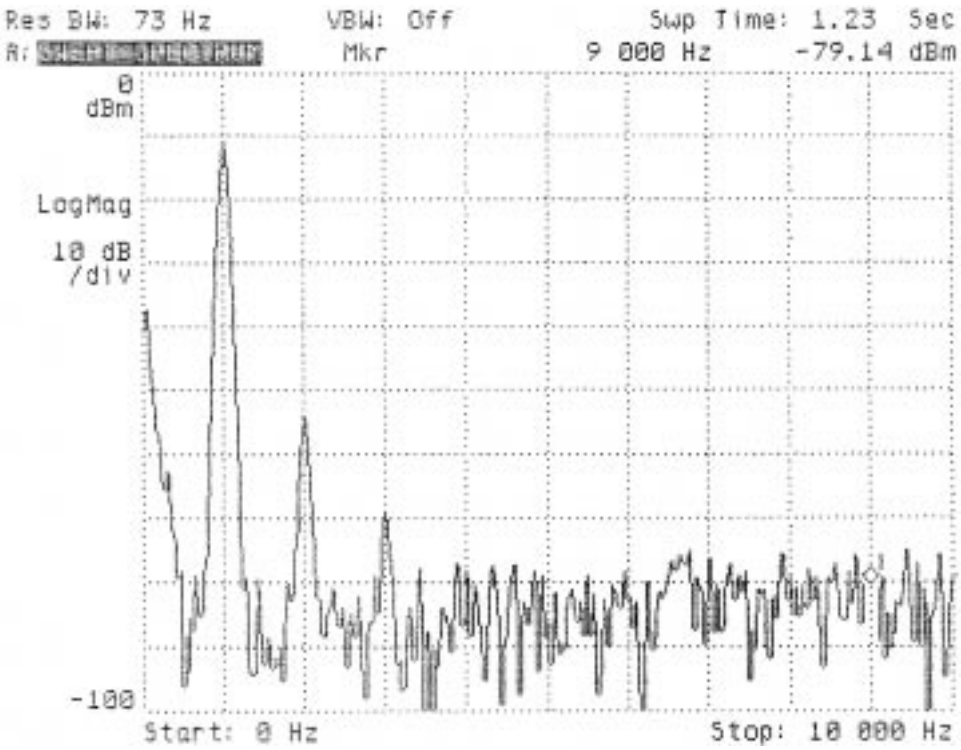

Fig. 10. Spectrum output for a 1-kHz, 1.6 μA (peak value) input signal and a cut-off frequency of 13 kHz.

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Dorra Masmoudi was born in Sfax, Tunisia in 1969. She received her M.Sc. degree in electrical engineering from the National Engineering School of Sfax, Tunisia, in 1994. Subsequently she joined the Microelectronics Research Laboratory IXL, at the Bordeaux University to work towards a thesis. Her research includes low-voltage low-power design for medical applications.

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He is co-editor and co-author of the books *Analog IC Techniques for Low-Voltage Low-Power Electronics* (Delft University Press, Delft, 1995), *Low-Voltage Low-Power Analog Integrated Circuits* (Kluwer Academic Publishers, Boston, 1995) and *Dynamic Translinear and Log-Domain Circuits* (Kluwer Academic Publishers, Boston, 1998). He has authored and co-authored more than 60 publications. He teaches Analog Electronics, Analog IC Techniques and Structured Electronic Design.

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