Design and Custom Fabrication of a Smart Temperature Sensor for an Organ-on-a-chip Platform

Ronaldo Ponte*, Vasiliki Giagka*† and Wouter A. Serdijn*
*Section Bioelectronics, Dept. Microelectronics, Faculty EEMCS, Delft University of Technology
†Technologies for Bioelectronics Group, Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany
Email: r.martinsdaponte@tudelft.nl, v.giagka@tudelft.nl, w.a.serdijn@tudelft.nl

***Abstract*—This paper reports on the design and fabrication of a time-mode signal-processing *in situ* temperature sensor customized for an organ-on-a-chip (OOC) application. The circuit was fabricated using an in-house integrated circuit (IC) technology that requires only seven lithographic steps and is compatible with MEMS fabrication process. The proposed circuit is developed to provide the first out-of-incubator temperature monitoring of cell cultures on an OOC platform in a monolithic fabrication. Measurement results on wafer reveal a temperature measurement resolution of less than $\pm 0.2\ ^{\circ}C$ (3σ) and a maximum nonlinearity error of less than 0.3% across a temperature range from 25 °C to 100 °C.**

***Keywords*—Smart temperature sensor, organ-on-a-chip, time-mode signal-processing, IC MEMS co-design**

I. Introduction

Incubators in cell cultures are used to grow and maintain cells under optimal temperature alongside other key variables, such as pH, humidity, atmospheric conditions etc. As enzymatic activity and protein synthesis proceed optimally at 37.5 °C, a temperature rise can cause protein denaturation, whereas a drop in temperature can slow down catalysis and polypeptide initiation [1].

Inside the incubator, the measurements are gauged according to the temperature of the heating element, which is not exactly the same as that of the cells. Time spent outside the incubator can greatly impact cell health. In fact, out-of-incubator temperature and its change over time are unknown variables to clinicians and researchers, while a considerable number of cell culture losses are attributed to this reason. To accurately monitor the temperature of the culture throughout cell growth, an *in situ* temperature sensor with at least ±0.5 °C of resolution is of paramount importance. This allows the growth of the cultured cells to be optimized.

To the authors' best knowledge, no *in situ* temperature-sensing fully integrated on an organ-on-a-chip (OOC) platform exists to date. This is the first time such integration is being performed using a custom-designed circuit fabricated on the same silicon substrate as that of the OOC. For a better visualization of the system, the reader is referred to Fig. 1.

The simple, robust, and custom IC technology used for the sensor fabrication grants a very cost-effective integrated solution in virtue of the reduced cost per wafer along with the large silicon area available on the platform [2]. Moreover, no further complicated assembly and subsequent protection of the pre-fabricated components is required. This minimizes the extra processing steps, along with the related handling risks, leading to higher yields. Finally, the freedom enjoyed by the MEMS-electronics co-design offers a large degree of versatility to accomodate electronics in a range of different OOC shapes and structures.

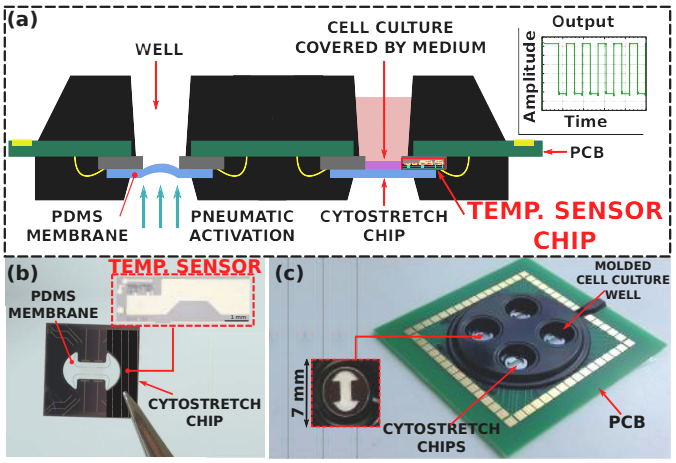

Fig. 1. The OOC platform (cytostrech device [3]) used to integrate the temperature sensor chip: a) cross-section of the system, b) top-view detailing the silicon die comprised of a PDMS membrane and the monolithically integrated temperature sensor, c) optical image of the multi-well plate including four cytostretch chips. Reproduced with permission of the authors.

II. System Design

The overall temperature sensing system consists of two main blocks: a proportional to absolute temperature (PTAT) current generator (comprising of npn bipolar transistors to sense the temperature information) and a current-controlled relaxation oscillator (Fig. 2).

The idea behind this design is to produce a periodic signal, presenting a square-wave-like format, which contains the temperature information encoded in the time domain. In this way, the overall system level is more energy efficient because the data transfer is carried out through one wire only. As a result, the energy per sample is reduced compared to that required by conventional digital designs [4]. In addition, the conditioned signal becomes more robust against noise and interference.

The circuit operation can be understood through an inspection of Fig 2. After start-up, the output of the comparator is set to a logic "0", the current source is switched on and the charging cycle takes place. During this cycle, the PTAT current generated is integrated on the capacitor (C), forcing

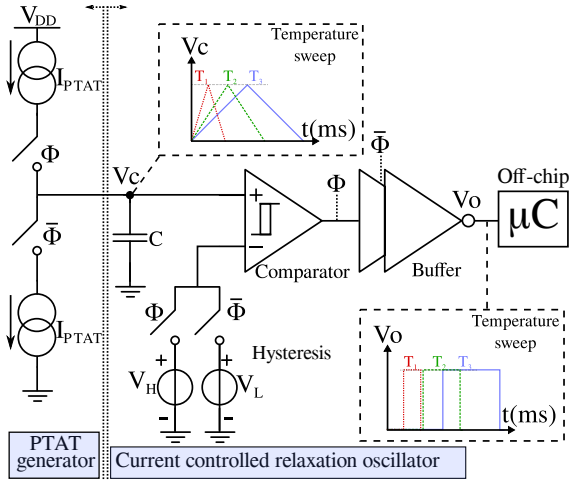

Fig. 2. System-level design detailing the main blocks: a PTAT generator and a current-controlled relaxation oscillator

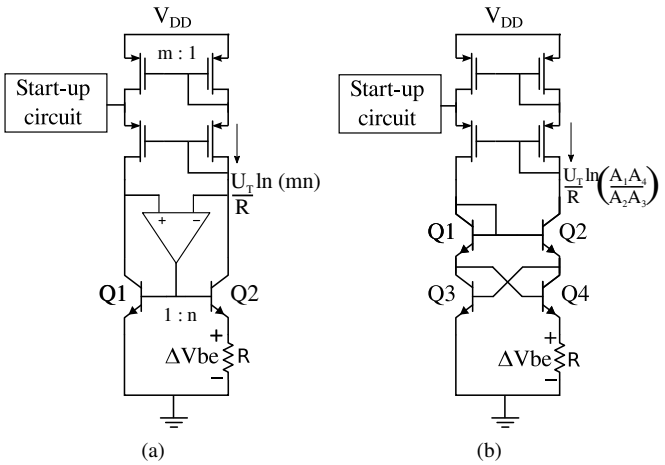

Fig. 3. PTAT current source and sink generators: (a) Implementation using opamp as a nullor; (b) Translinear loop cross-quad cell

the voltage (V_c) to ramp up. This voltage is compared to two different voltage references that are produced by the hysteresis block: the high (V_H) and low thresholds (V_L) denoting the charging and discharging cycles, respectively. When V_c equals V_H, the output of the comparator switches its logical state and the discharging cycle takes place, discharging the capacitor through the PTAT current sink. When V_c reaches V_L, the discharging cycle ends and the whole process repeats itself again, indefinitely. The comparator outputs a signal, the period of which is PTAT according to the following equation:

$$T = \frac{C\Delta V}{I_{PTAT}}, \tag{1}$$

where ΔV is the difference between the two threshold voltages V_H and V_L.

A. PTAT generators

For the PTAT current source and sink generators, two different designs were constructed (Fig. 3).

The first PTAT current generator (Fig. 3(a)) yields a current according to the voltage drop across resistor R: $\Delta V_{BE} = V_{BE1} - V_{BE2}$. Since this voltage is the difference of the two V_{BE} voltages, the current produced, $I = \Delta V_{BE}/R$, is PTAT. Cascode current mirrors with a m:1 ratio send the copy of the current to the integrator. The opamp acts as a nullor to keep the collector voltages the same, regardless of variations in the power supply or in the temperature, as well as providing the necessary base current to the bipolar transistor. The expression of the current is:

$$I = \frac{U_T}{R} \ln\left(\frac{I_{C2} I_{S1}}{I_{S2} I_{C1}}\right) = \frac{U_T}{R} \ln(mn), \tag{2}$$

where U_T is the thermal voltage, I_S is the saturation current (which is dependent on the emitter area), m is the current mirror ratio and n is the bipolar emitter area ratio. Therefore, the responsivity of this cell is mainly determined by the current mirror and emitter area ratios. For this design, values of five and four for m and n, respectively, were chosen. In addition, because of the self-biasing mechanism involved in this PTAT cell, this generator shows a second operating point when all currents are equal to zero. Hence, a starting circuit is of paramount importance to guarantee the proper operation of the circuit.

The second PTAT generator (Fig. 3(b)) uses a translinear cross-quad as a PTAT cell [5]. Following the translinear loop, the voltage drop ΔV_{BE} across the resistor is now computed as:

$$\Delta V_{BE} = V_{BE3} + V_{BE2} - V_{BE4} - V_{BE1}. \tag{3}$$

The expression for the current now becomes:

$$I = \frac{U_T}{R} \ln\left(\frac{A_1 A_4}{A_2 A_3}\right). \tag{4}$$

The responsivity here is determined by the emitter areas of the four bipolar transistors. Hence, this topology is less sensitive to any mismatch in the cascode current mirror. However, the circuit is slightly sensitive to the finite current gain of the bipolar transistors. For this design, A_1 and A_4 were chosen to be four times larger than A_2 and A_3.

B. Hysteresis circuit

A hysteresis circuit is often designed to prevent multiple transitions of the threshold voltage in the comparator that occur due to noise or other disturbances in the signal. In order to increase the responsivity of the temperature sensor circuit, the hysteresis is made inversely proportional to the absolute temperature (IPTAT, also known as CTAT). As a result, the overall circuit responsivity in respect to the period of the signal is increased.

The hysteresis circuit is comprised of nine stacked diode-connected bipolar transitors biased with a weighted copy of the PTAT current in order to yield values for V_H and V_L, at 37.5 °C, of 6 V and 3.5 V, respectively. These values were chosen to ensure enough headroom for the devices.

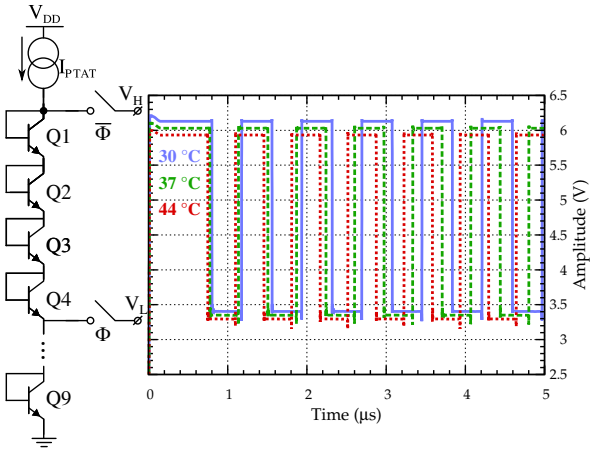

Fig. 4. Hysteresis circuit used to yield the threshold voltages for the comparator operation, V_H and V_L, and simulated output waveform generated.

III. Simulations

Circuit simulations of both PTAT cells with respect to the temperature are shown in Fig. 5.

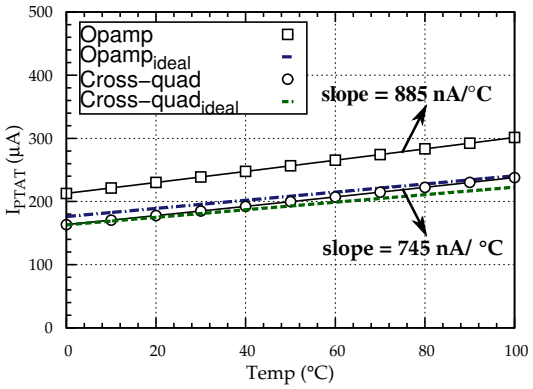

Fig. 5. Simulation result of both PTAT generators (opamp-based and cross-quad) in respect to the temperature and their respective ideal theoretical curves. Deviations in value from their ideal characteristics are mainly explained by high injection effects in the base region and non-zero emitter resistances both present in the SPICE model.

Simulations reveal a responsitivity of 745 nA/°C and 885 nA/°C for the cross-quad and opamp-based PTAT generators, respectively. Further, simulations disclose less than 0.3% of maximum nonlinearity error across the range from 0 °C to 100 °C. The difference in the value of the opamp-based generator from its ideal theoretical characteristic, as shown in Fig. 5, is mainly due to the value of the reverse beta high current roll-off (I_{KF}) included in the SPICE model. As a result, high injection effects in the base region modify the ideality factor (η) of the collector current, causing it to deviate from its theoretical exponential behaviour. On the other hand, the difference in the cross-quad output from its ideal characteristic is mainly due to the higher sensitivity of this topology to non-zero emitter resistances that were also included in the SPICE model.

IV. Fabrication

A planar BiCMOS IC technology that requires only seven masking steps is used to fabricate the three main devices in the

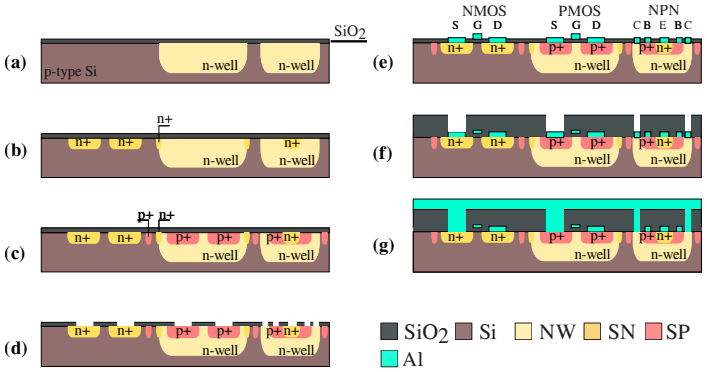

Fig. 6. Cross-sections of the custom-made BiCMOS technology used in EKL (Else Kooi Lab).

circuit: bipolar transistors (npn), nMOS and pMOS transistors (Fig. 6) with 1-μm of minimum gate length. The process starts with a double-polished p-type silicon wafer with <100> of crystolographic orientation and 5 Ω·cm of resistivity.

The first mask (Fig. 6.a) is used to define the n-well and the collector area of the bipolar transistor using a 5e12-dose of phosporus implantation followed by 415 minutes of annealing. The second and third masks (Figs. 6.b and c, respectively) define the n/p-type diffusion areas for the CMOS and the emitter/base area for the bipolar device using arsenic and boron as dopants, respectively. After this step, another boron implantation is carried out to adjust the threshold voltages in four different quadrants of the wafer, followed by 115 minutes of oxidation to activate the dopants. After adjustment, the threshold voltages of the nMOS and pMOS transistors change to about 2.0 V and -2.5 V, respectively. As a result, the circuit is operated from a 10 V power supply in order to provide enough headroom for saturation of the FET transistors.

Contact openings are wet-etched with a BHF (buffered hydrofluoric acid) solution after the patterning of the fourth mask (Fig. 6.d), while the fifth mask (Fig. 6.e) is used to pattern the interconnect and gate material via the deposition of AlSi (1%). The process continues with a 2-μm deposition of SiO_2 using PECVD (plasma-enhanced chemical vapor deposition) on the front and back of the wafer to create the dielectric of the MIM (metal-insulator-metal) capacitor.

Masks 6 and 7 (Figs. 6.f and g) are used to open the vias using dry etching, before depositing the second layer of metal. The result of the chip fabrication, with the main building blocks highlighted, is shown in Fig. 7.

The total chip area used, including the MIM capacitor, is about 10.88 mm^2.

V. Results

Measurements were carried out through a wafer microprobe station that includes a thermal chuck for sweeping the temperature across the desired range. The time-domain output of the circuit was probed using a digital oscilloscope (Fig. 8) at the reference temperature (37.5 °C).

To calculate the resolution, the total root mean square (rms) period jitter was measured by tracing the histogram of the period over 10,000 random samples for each temperature

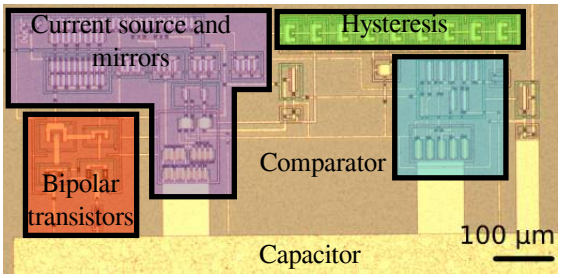

Fig. 7. The result of the fabricated chip using the in-house EKL technology with the: PTAT current source, current sink and current mirrors, bipolar transistors, capacitor, hysteresis block and comparator.

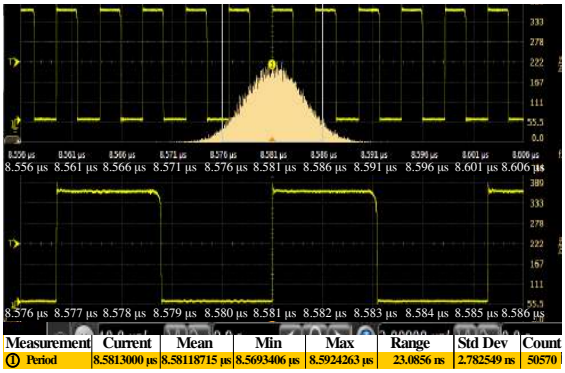

Fig. 8. Transient result of the temperature sensor at the reference temperature of 37.5 °C for the opamp-based PTAT generator. The standard deviation over 50,000 random samples of the measured period reveals a jitter of 2.78 ns.

point, from 25 °C to 100 °C, and computing the standard deviation. The result of this temperature sweep is shown in Fig. 9. The difference in slopes shown in this figure stems from the different responsitivities of both PTAT generators, as well as of non-idealities present in both circuits: high-level injection and emitter resistances. Further, the measurement results reveal a maximum nonlinearity error of 0.26% and 0.75% for the opamp and cross-quad circuits, respectively.

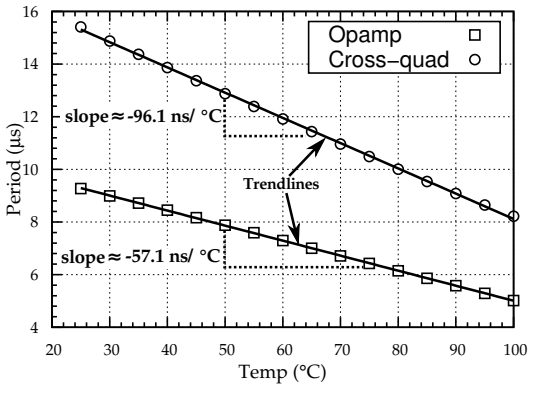

Fig. 9. Temperature conversion of the smart temperature sensor. The least-squares polynomial regression reveals a responsivity of 57.1 ns and 96.1 ns for the opamp-based and cross-quad PTAT generators, respectively.

At 37.5 °C, the total rms jitter was measured for more than 50,000 random samples and is equal to 2.78 ns and 5.98 ns for the opamp-based and cross-quad sensor, respectively. Two main reasons account for this difference: firstly, the large open loop gain of the opamp provides additional robustness against power supply variations; secondly, the current drawn by the opamp-based PTAT generator core is slightly higher than the current drawn in the cross-quad, thus, its total rms period jitter is lower. The resolution ($\mathcal{R}$) is calculated as the ratio of the jitter for 3σ and the responsivity, and equals:

$$\mathcal{R}_{\text{opamp}} = \frac{3 \times 2.78 \text{ ns}}{57.1 \text{ ns/°C}} = 0.15 \text{ °C } (3\sigma), \quad (5)$$

$$\mathcal{R}_{\text{cross-quad}} = \frac{3 \times 5.98 \text{ ns}}{96.1 \text{ ns/°C}} = 0.19 \text{ °C } (3\sigma). \quad (6)$$

The measured resolutions are about three times better than the initial intended resolution (± 0.5 °C). As a result, we will undertake the co-fabrication with the OOC platform as a follow-up to this work, and the opamp-based PTAT cell to be used at the final integration due to its better resolution. For a practical use on the OOC, the circuit is anticipated to have a 2-point calibration to correct for offset and non-idealities in the slope of the curve.

VI. Conclusions

A smart temperature sensor for an OOC platform, which produces the temperature information in the time domain, was designed and fabricated using an in-house IC technology that requires only seven lithographic steps and is compatible with MEMS fabrication process. Measurement results reveal a responsitivity of 57.1 ns/°C and a total rms period jitter of 2.78 ns, yielding an resolution of less than $\pm$ 0.2 °C (3σ), from 25 °C to 100 °C. The maximum nonlinearity error found is less than 0.3%. When operating from a 12 V power supply, the circuit consumes about 36 mW.

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