A 0.5V Signal-Specific Continuous-Time Level-Crossing ADC with Charge Sharing

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***Abstract* — This paper presents a novel continuous-time level-crossing analog-to-digital converter (LC-ADC) targeted at biomedical signal sensing applications. The conventional digital-to-analog converter (DAC) is replaced by a charge sharing block, leading to lower power consumption, less design complexity and more flexibility for various resolution applications. Designed to be implemented in 90 nm CMOS technology, the proposed ADC achieves a maximum SNDR of 51.4dB and consumes a minimum power of 538nW from a dual supply of 0.5V and 0.7V.**

I. INTRODUCTION

Analog-to-digital converters are indispensable building blocks of wearable and implantable biomedical data acquisition systems. Conventional ADCs utilize uniform sampling, which is based on periodically sampling the magnitude of the signal. Among those ADC structures, the successive approximation register (SAR) ADC is the most popular one in low power applications, because the only analog circuitry within it is a comparator, while the rest of the circuits are digital and thus easily scale down with technology. Basically, SAR-ADCs periodically sample the input and use binary search algorithms to successively approximate the sampled input signal from the most-significant bit (MSB) to the least-significant bit (LSB). However, SAR-ADCs are not that power-efficient for biomedical signal recording, as most of the signal components have small signal magnitudes, while the SAR-ADC repeats the same searching procedure from MSB to LSB for each input sample even when the input signal varies slowly.

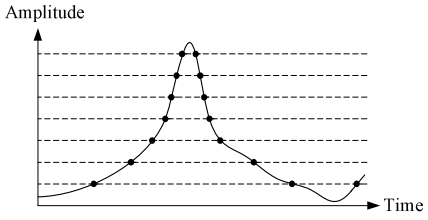


Fig. 1 Level-crossing sampling

A new and promising ADC approach for biomedical data acquisition is based on so called level-crossing sampling [1], which operates in the continuous time domain. As is shown in Fig. 1, samples are generated only when the input signal crosses the threshold levels, while the time in between two consecutive samples is measured by a timer. The output of this LC-ADC is thus composed of digital codes and the time interval. Its advantages include: 1) low-frequency and low-amplitude inputs are sampled less densely in time than high-frequency and high-amplitude inputs. Hence, a much lower average sampling rate is achievable for biomedical applications; 2) non-uniform sampling is used, thus no aliasing occurs; 3) lower EMI emission [1][2][3]; 4) a clock is only used to count the time for each sample, so the requirements on this clock and its related circuits are much more relaxed; it is also possible to process the non-uniform samples by a continuous-time DSP without a clock [3][4]; 5) in a LC-ADC, magnitude quantization shifts to time quantization, which can be more precise when using a low supply voltage.

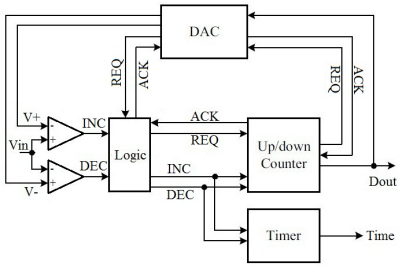


Fig. 2 Block diagram of a conventional LC-ADC

A few LC-ADCs have been reported in recent years [4]-[6]. Typical LC-ADCs consist of comparators, a DAC, an Up/Down counter, a timer and control logic, as is shown in Fig. 2. The DAC converts the digital outputs of the Up/Down counter to an analog quantity, often voltage, which sets two levels V_+ and V_- for the comparator (V_+ is 1 LSB higher than V_-). The DACs in LC-ADCs are either implemented by a resistor string or a switched-capacitor array with operational amplifiers (op-amps). Unfortunately, the DAC consumes static power in both cases, which is not that power-efficient for biomedical applications.

In this paper, we present a new and simple topology that provides a low-power low-voltage LC-ADC with charge sharing. The power consumption of the LC-ADC is reduced

significantly because 1) the conventional DAC is replaced by a charge sharing block, which does not consume static power and is more suitable for a LC-ADC; 2) the requirements on the comparator design are relaxed due to an offset injection mechanism; 3) the input voltage range is not limited by a voltage reference or even the power supply. More details of the proposed LC-ADC are discussed in the following sections.

II. System structure of LC-ADC

A. Architecture of a conventional LC-ADC

As is shown in Fig. 2, the operation of a conventional LC-ADC can be summarized as follows. As long as the input signal is between the two levels (V+, V-), the outputs of both comparators are low and no sample is generated. When the input signal moves outside this range, one of the comparators will detect the level-crossing, outputs a logic "1" on INC (increment) or DEC (decrement) and a conversion is triggered. The control logic generates a corresponding signal to control the up/down counter and the timer. The up/down counter outputs the previous digital code and increases by 1 (or decreases by 1). Meanwhile, the timer outputs the duration of the previous sample, then resets and starts to record the duration of the next sample. The DAC converts the new digital code of the up/down counter to analog voltages, which are fed back to the inputs of the comparators. The input signal is then between the refreshed two levels again.

There are some drawbacks of such a LC-ADC. Firstly, the basic principle of a LC-ADC is to keep tracking the input so that it is always between the two nearest levels. Therefore, the DAC refreshes its outputs by increasing or decreasing both levels by only 1 LSB for each sample. It is not power-efficient to use a binary weighted DAC, as a binary scheme is not optimized for changing the output by 1 LSB each sample. Consequently, it is necessary to design a block that is able to convert 1 LSB to an analog voltage at the least cost.

Secondly, in conventional LC-ADCs, the output voltages of the DAC track the input voltage over the full scale voltage range, which means the input common-mode voltage of the comparator varies a lot during data conversion. An input common-mode related error thus affects gain, bandwidth, delay etc. and thereby generates different time offsets and distortion for different input signal levels.

B. Architecture of proposed LC-ADC

The system structure of the proposed LC-ADC is shown in Fig. 3 (a). We apply differential inputs (Vip, Vin) that act as two single-ended signal with opposite polarity, so one fixed reference voltage level instead of two is able to detect both level-crossings. A dual supply is used: 0.7V for the switches in the charge sharing block; 0.5V for the remaining circuits. The information of increment and decrement is converted into "change" and "up/down" in our system. "Change" is the logic OR of INC and DEC while "up/down" indicates the direction of the change. The working principle is similar to the previous LC-ADC except for that of the charge sharing block.

We replace the DAC with a charge sharing block, which tracks the input signal and "resets" its differential outputs to a level that is 1 LSB lower than a fixed level V_{REF}. The output node voltage follows the input voltage until the reference level is reached. Then, depending on the input variation direction, a negative 1 LSB offset or a positive 1 LSB offset is added. This mechanism goes on throughout the whole input swing. See Fig. 3 (b)

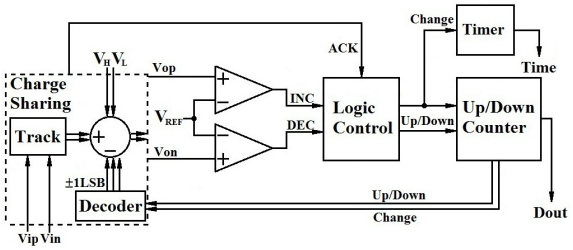
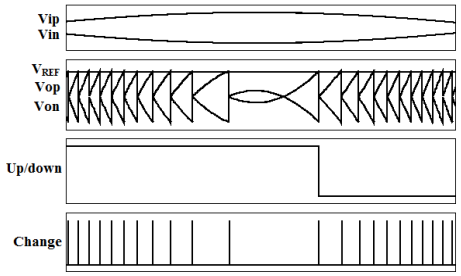


Fig. 3 (a) Proposed LC-ADC



(b)Example waveforms

In the proposed ADC, we make use of only one fixed reference level and perform subtraction or addition on two tracked differential inputs. The input common-mode voltage of both comparators is thus fixed, which solves the problems mentioned above in a more power-efficient way.

III. Circuit blocks

A. Control logic

The control logic is similar to the one in [4]. Basically, it takes the comparator outputs of INC and DEC and then translates the 2 bits information of increment and decrement to change and up/down, which then control the charge sharing process. The logic equations can be represented by:

$$Change = INC + DEC$$
$$Up/Down = INC \cdot \overline{DEC} \quad (1)$$

B. Charge sharing

One half of the differential charge sharing block is shown in Fig. 4. Fig. 4 (a) depicts the capacitor array and the control signals for the switches. Fig. 4 (b) shows the decoder. There are two identical branches in the capacitor array in Fig. 4 (a). The right one is responsible for tracking the input while the left one is for offset injection (OI). Two capacitors in each branch are connected in series in order to achieve an AC-coupled input and share charge without affecting the input. nMOS transistors are utilized as switches. To increase the on-resistance of the switches, a 0.7V supply is used to control the three switches S_1-S_3. A level converter is thus necessary for interfacing the circuits that operate from a supply voltage of

0.5V and those that operate from 0.7V. The level converter is shown in Fig.4 (b) and its working principle is discussed in [7].

The charge sharing block simply increases or decreases the tracked input voltage by 1 LSB for each sample. It works as follows: assume the situation when the input signal increases and crosses a level. Subsequently, "change" and "up/down" pulses are generated and entered into the decoder, which translates "change" and "up/down" into Φ_1-Φ_3 to control the charge sharing process, as shown at the right hand side picture of Fig. 4 (a). S_1 is switched off first to disconnect the OI branch from the tracking branch, while the latter one still keeps tracking the input. S_2 is then switched on to connect the OI branch to the lower voltage reference V_L to discharge. After a short while (depending on the settling time) S_2 is switched off and the two capacitor arrays are connected again by switching on S_1. V_{OUT} is then decreased by 1 LSB. The charging process is similar to the discharging process, but uses Φ_3 instead to charge C_2 to V_H.

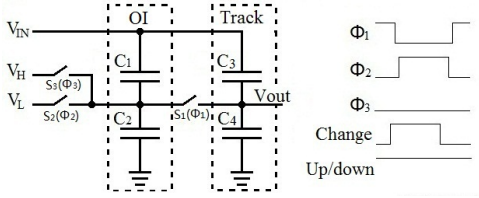
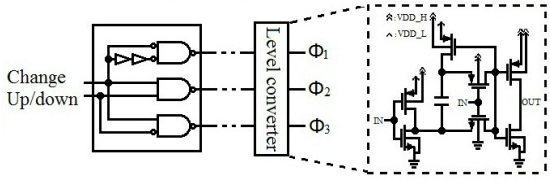


Fig. 4 (a) Schematic of capacitor array



(b) Schematic of decoder and level converter

Φ_1 and Φ_2 are non-overlapping to avoid connecting the output node directly to voltage reference V_H or V_L. C_1 (C_3) is set to 100fF while C_2 (C_4) is 9 times larger, so that the majority of the input voltage variation falls on the upper plate of C_2 (C_4). In the proposed structure, because the output node of the tracking capacitor array is floating, it takes some start-up time for the voltage on the node to reach the working point.

There are some differences between the proposed charge sharing block and previous works. In [5], although its DAC also does subtraction from the input, the maximum input range is limited by the voltage reference and the capacitor array used is much larger. In [8], the ADC is not able to track the input signal during discharging and an offset is thus introduced for each sample. In [9], a power-hungry amplifier is used in order to do charge injection. The advantages of the proposed approach include: 1) the input voltage range is not limited by the voltage reference. The input voltage range is shifted up or down within the input dynamic range as soon as the tracked input voltage reaches the fixed level. In other words, the voltage reference can be much smaller and the input signal can be larger than in conventional structures; 2) the dynamic power consumption of the capacitor array is lowered, as the capacitor array is much smaller than the conventional ones and a voltage step of only 1 LSB per conversion is required; 3) the charge sharing technique is tolerant to clock feedthrough and charge injection of the switches, because the errors introduced due to these mechanisms are practically the same during each cycle.

C. Comparator

The continuous-time comparator used is shown in Fig. 5. It comprises a PMOS input differential amplifier followed by two common source stages. Two inverters are added at the output to achieve a rail-to-rail swing. Since the input common mode voltage is fixed, the propagation delay does not vary due to input common mode variation, but due to: 1) the offset between the two comparators; 2) the variation in slope of the input signal. The former can be viewed as a shift in the lower threshold level relative to the upper threshold level [5]. The latter leads to offsets in time for different inputs. All these will influence the harmonic distortion and degrade the SNDR. To cancel the comparator offset, we can use a calibration mechanism similar to [4]. To minimize the time offset, a maximum delay that is smaller than the resolution of the timer must be guaranteed.

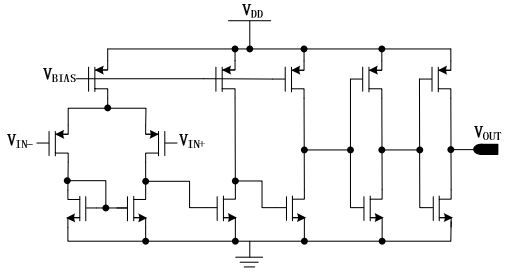


Fig. 5 Schematic of comparator

IV. SIMULATION RESULTS

To evaluate the performance of the designed ADC, simulations using IBM's 90nm CMOS process have been carried out. The switches in the charge sharing block operate from a 0.7V supply while the rest of the circuits operate from a 0.5V supply. The up/down counter and timer are realized by verilogA, so their power consumption is not included in the entire system. In a future design, we plan to use an asynchronous bi-directional shift register to replace them.

Note that the input voltage range is not limited by the voltage reference or even the supply voltage. We can achieve a bigger LSB from a higher input for a given number of levels. In other words, the number of levels, LSB and full scale input range are flexible and are related by

$$V_{FS} = Number_{Levels} \times LSB \quad (2)$$

Although a bigger LSB enables the LC-ADC to be more tolerant to charge injection and clock feedthrough, more power will be consumed. Therefore, V_H and V_L are set to 80mV and 70mV, respectively. 1 LSB thus equals 10 mV.

At the input, a 1.1 kHz sinusoidal signal with the amplitude of 740mV is applied, leading to the output with 63 levels. The output spectrum for the signal is shown in Fig. 6. The timer works at 10MHz and a reconstruction sampling frequency of 51.2 kS/s is used. 63 levels were detected in the simulation. To compute a standard FFT for the simulation results, a third-order polynomial interpolator was used in MATLAB. One

thing worth mentioning is that different reconstruction algorithms possibly lead to slightly different results. The third order distortion is due to the input slope-dependent delay of the comparator.

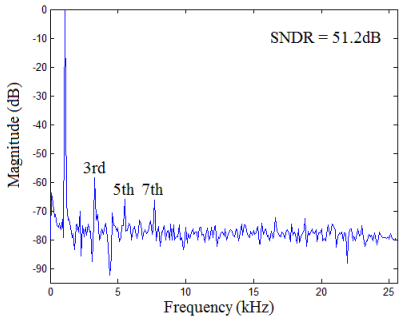


Fig. 6 FFT plot for 1.1 kHz sinusoidal input

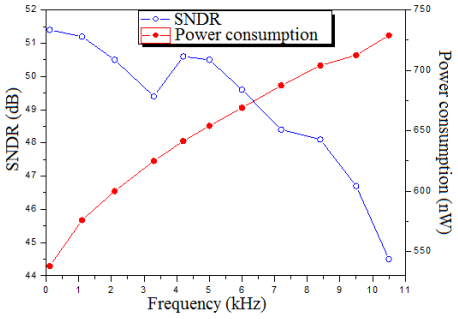


Fig. 7 SNDR and power consumption versus input frequency

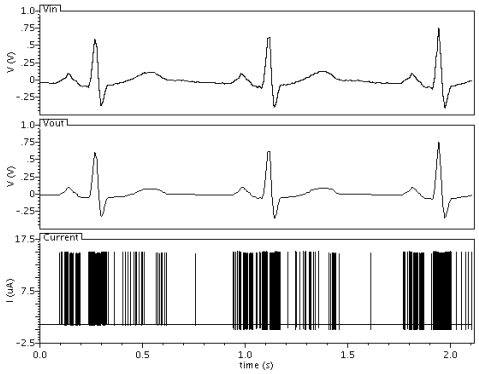


Fig. 8 ECG signal simulation and current consumption (bottom)

Fig. 7 shows the signal-to-noise-and-distortion ratio (SNDR) and power consumption of the ADC for various input signal frequencies (0.11 kHz to 10.5 kHz), but with the same amplitude. As can be seen from Fig. 7, the power consumption is related to the input frequency: a higher input frequency results in more power consumption and vice versa. SNDR drops 7dB from the lowest input frequency to the highest input frequency. At low frequency, SNDR is limited by the accuracy of the analog components [5]. When input frequency increases, the oversampling ratio in time decreases, while the loop delay of LC-ADC introduces higher harmonic distortion in the shorter time interval between each sample.

The dynamic power saving can be easily seen from Fig. 8 when we use an ECG signal as an input signal. The top picture and middle one show the original input and the one after conversion, respectively. The corresponding total current consumption is shown at the bottom. A summary of the simulation performance is given in Table I.

Table I Performance summary

Technology	90nm CMOS
Supply Voltage	0.7V for switches 0.5V for the remaining circuits
Resolution	8bits
Power Consumption	538nW@0.11kHz 729nW@10.5kHz
SNDR	51.4dB@0.11kHz 44.5dB@10.5kHz
Input Swing	Not limited by voltage reference

V. CONCLUSION

In this paper, we have proposed a level-crossing ADC with charge sharing, which is based on positive or negative 1 LSB offset injection for each sample. The circuit has been designed and simulated in IBM 90nm CMOS process. Less than 1 microwatt of power consumption is achieved due to the smaller capacitor array and relaxed requirements for the comparator. The event-driven characteristic makes the proposed ADC especially suitable for biomedical applications.

ACKNOWLEDGMENT

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