An Ultra Low-Power Peak-Instant Detector for a Peak Picking Cochlear Implant Processor

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Abstract—**This paper presents the design of a sub-threshold CMOS peak-instant detector to be used in a phase-locking peak-picking (PL-PP) bionic ear (BE) processor. The detector is formed by a current sample and hold circuit and a voltage comparator to perform the detection of occurrences of maximum and minimum values of the input. Circuit simulation results using CMOS 0.35 μm AMIS technology confirm that the proposed detector can be operated from a 1.2 V supply and consumes less than 1μW static power for detecting a 5kHz input signal (maximum frequency of the processor). For lower input frequencies the power consumption can be scaled down to further reduce the BE processor's power consumption.**

I. Introduction

Trying to allow a bionic ear processor to convey phase and temporal fine structure (TFS) in addition to the envelope of the speech signal to the auditory nerve fibers, several speech processing strategies have been proposed to be used in the BE processor including phase-locking zero-crossing detection (PL-ZCD) [1], asynchronous interleaved sampling (AIS) [2], and PL-PP [3] strategies. They are based on the idea of imitating either phase locking [4] or random firing [5] of the spike train in the auditory nerve fiber.

A recent comparison in terms of correlation factor of the input and reconstructed signals and hardware complexity pointed out that with a comparable correlation factor, the PL-PP strategy provides a compact solution for the BE electronic hardware design since this strategy does not require a high precision envelope detector [6].

In this paper, we present the design of low-power peak-instant detector for supporting the PL-PP strategy to be incorporated together with the continuous interleaved sampling (CIS) strategy [7] within an ultra low-power BE processor. To operate the entire CMOS circuit in weak inversion region for the purpose of very low power consumption, the switched current (SI) technique is applied to let us benefit from the mismatch insensitive feature of the SI memory cell.

The remaining sections of the paper are organized as follows. In Sec. II, a review of the PL-PP speech processing strategy is given. The fundamental concept and its accompanying circuit description of the proposed peak-instant detector (PID) are presented in Sec. III. Next, Sec. IV presents the simulation results. This work will be finally summarized in the last section.

II. Peak-picking Strategy for Low-Power Cochlear Implants Processor

In the normal mammalian auditory nerve fibers, the spike trains synchronize with the stimulus waveform periodicity up to 5 kHz [4]. Beyond that frequency range, the spike trains are generated randomly [5]. These mechanisms are missing in the conventional CIS strategy since the pulse stimulation rate is fixed [7]. To gain the perception of tonal languages and music, an effort of realizing the BE processor that imitates the inner hair cells and the auditory nerve behavior more precisely is necessary. One way to achieve this is introducing the Hilbert Transform (HT) to the BE processor to extract temporal envelope, instantaneous frequency and phase, and thereby the TFS [8] and try to convey them to the stimulation electrodes. Although extraction is possible, conveying all of the information to the brain via electrical pulse trains is still a challenge that remains. Besides, performing the HT imposes a large computational cost for both digital [9] and analog [10] processors. The comparative study in [6] suggests that the PL-PP strategy provides a compact solution to partially convey the TFS suitable for an ultra low-power analog BE processor.

Fig. 1 shows a block diagram of the PL-PP speech processing strategy. It comprises four main elements; a pre-emphasis block, a band pass filter (BPF) bank, a number of peak-instant detectors (PIDs), and modulators. The incoming sound is pre-emphasized by non-linearly amplifying it before entering the bank of BPFs. This mechanism is adapted from the role of the outer hair cells that map the wide range of the incoming sound pressure onto the limited dynamic range of the ear. The BPF bank roughly mimics the basilar membrane behavior by decomposing the signal into a limited number (N) of frequency bands (channels). The peaks of the signal coming from BPF of each channel will be extracted by the PID enabling the modulator to perform multiplication of a rectangular pulse signal and the peak amplitude.

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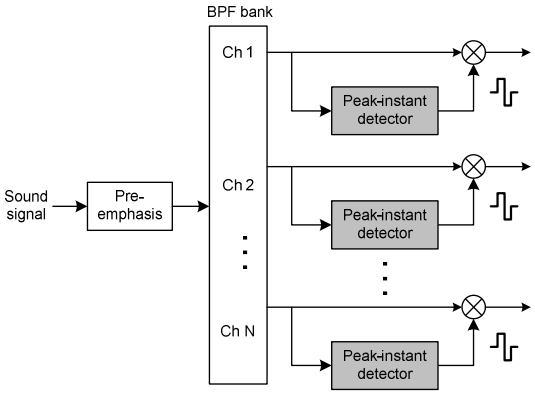

Figure 1. PL-PP speech processing block diagram

This results in a set of rectangular stimulation pulses of which the amplitude is defined by the peak of the signal of each channel and the pulse frequency change according to the speech signal of each channel. Note that there is a possibility that the resulting stimulation pulses from different channels can appear at the same time introducing simultaneous interactions between stimulation electrodes which degrades the hearing perception. This undesired mechanism still needs to be eliminated. This is beyond the scope of this work.

Fig. 2 shows a fraction of the speech signal from the word 'die' after 4th-order butter-worth BP filtering with a center frequency of 150 Hz (Ch. 1 of the block diagram in Fig. 1). The signal obtained from Ch. 1 is represented by the dashed line. The HT (which is not part of the PL-PP strategy) is applied to the dashed line signal and the envelope is extracted and shown by the dotted line. The resulting pulses taken from the output of the modulator are represented by the solid line. As we can see from the peaks that always touch the Hilbert envelope, the BPF output signal and the detected peaking moments can be used to generate the stimulation pulses directly without the need for a very precise envelope detector. The precision requirement of the stimulation pulse amplitudes is relayed onto the precision of a PID instead.

III. Current Mode Peak-Instant Detector

A. Concept

The basic idea of the proposed PID is shown by the block diagram in Fig. 3a [11-12]. Input signal x_t is split into two signal paths. First, it goes to the sample and hold amplifier, SHA, (with a unity gain) generating a half delayed signal, x_{td}. Second, it goes to the summing node. The sample and hold time period are controlled by a clock signal with 50% duty cycle indicated as the middle trace of Figs. 3b and 3c. The subtracted result of x_t and x_{td} at the holding period will change its polarity when x_t reaches its maximum and minimum values. For this reason, the comparator can decide on its logical output y_t according to its input sign reversing moment.

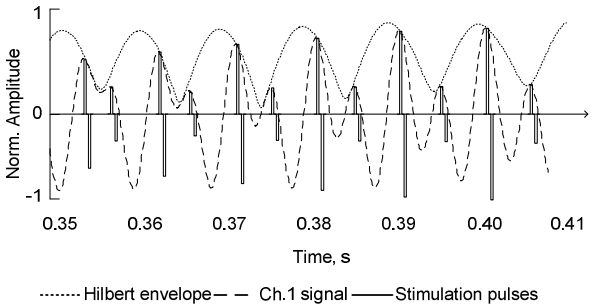

Figure 2. Waveforms obtained from PL-PP strategies

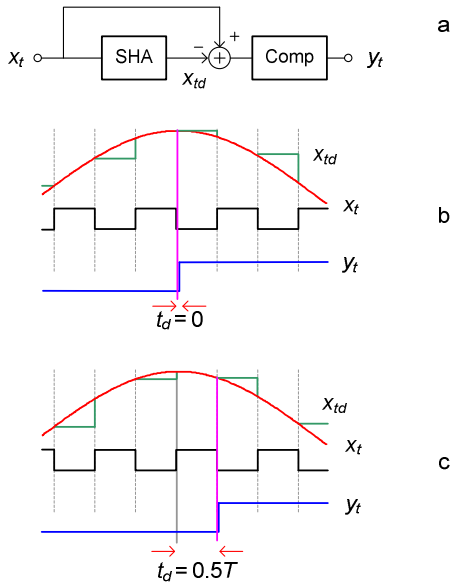

Figure 3. SI peak detection concept a) operational block diagram b) best case detection c) worst case detection

Since the incoming signal is random, this concept gives us two extreme cases of delay time (assuming the comparator is ideal). Firstly, the minimum delay time (t_d) occurs when the falling edge of the clock signal is located exactly at the peak of x_t (See Fig. 3b). In this case, the detected y_t will not be delayed. Secondly, the maximum delay time occurs when the rising edge of the clock is located exactly at the peak. In this case, t_d becomes a half period of the clock signal. In practice, the charge injection error and output noise of the SHA and minimum detectable input signal and delay time of the comparator introduce additional errors. In circuit level design, the architecture of the SHA needs to be insensitive to the switch charge injection error and the resolution and speed of the comparator need to be sufficiently good to decide on its logical output within a half clock period.

B. Circuits

Fig. 4 shows a macro-model of the proposed PID. It comprises a fully differential SI-SHA and a voltage comparator. The PID is controlled by two non-overlapping clock phases S_1 (sampling) and S_2 (holding). When the set of

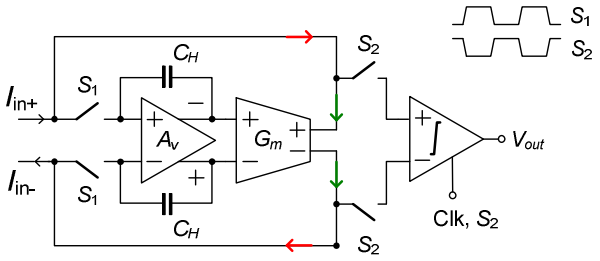

Figure 4. Macromodel of the SI peak-instant detector

switches S_1 turns on, the differential input current will be converted into voltages across C_H. In the next phase, S_1 turns off and the set of switches S_2 turns on. Both identical C_H's will memorize the voltages across them producing a constant differential current via transconductor G_m. The memorized current will be compared with the input current and converted into a differential voltage at the input nodes of the comparator. The comparator will make a decision within this phase and generate an output logical voltage V_{out}. The clock control signal is applied to allow the comparator to operate only at the holding period otherwise the logical output remains. Due to the large loop gain providing by voltage amplifier A_v, voltages across switches S_1 are forced to be fixed at the input common mode level. This leads to signal-independent charge injection errors after the (practical MOS) switches are turned off and thus will be cancelled out by the differential operation at the input of the comparator [13].

The sub-circuits used to realize all active elements in Fig. 4 are shown in Fig. 5. A_v is formed by the circuit of Fig. 5a and its output common-mode level V_{C2} is controlled by the common-mode feedback (CMFB) circuit depicted in Fig. 5b. G_m is realized by the circuit in Fig. 5c and its output common-mode level V_{C1} is controlled by the CMFB circuit in Fig. 5d. Stability of the feedback loop can be maintained by setting a fixed ratio of bias currents I_{B2} and I_{B1} and a value of C_H that needs to be bigger than the parasitic capacitances present at the input nodes of the A_v and those of G_m when the loop is closed [13]. We satisfied this condition by setting $I_{B2} = 2.2I_{B1} = 220\text{nA}$ and realizing C_H by NMOS capacitors biased in their strong inversion region. We thus set supply voltage $V_{DD} = 1.2\text{V}$, common-mode voltages $V_{C1} = 1\text{V}$ and $V_{C2} = 0.2\text{V}$. All the transistors in the entire circuit are working in weak inversion and the parasitic capacitances are smaller compared to those of MOS transistors in strong inversion region for the same device size.

The comparator is realized by the circuit shown in Fig. 6. It is composed of a differential input stage cascaded by a chain of CMOS inverters to enhance the overall gain. Input parasitic capacitors $C_{\text{in+}}$ and $C_{\text{in–}}$ are employed to memorize the input voltage for keeping the output voltage at the same value for the whole sampling period (switches S_2 are turned off). It is worth to mention here that the comparator employed here is just a simple high gain open-loop amplifier which does not provide high speed and high sensitivity. Better results can be expected from using more sophisticated comparator circuit, if needed.

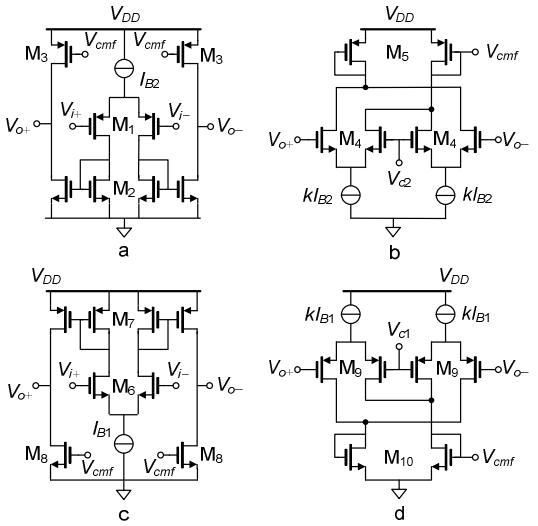

Figure 5. Sub-circuits of SHA a) transconductor G_m b) CMFB circuit for the G_m c) voltage amplifier A_v d) CMFB circuit for the A_v

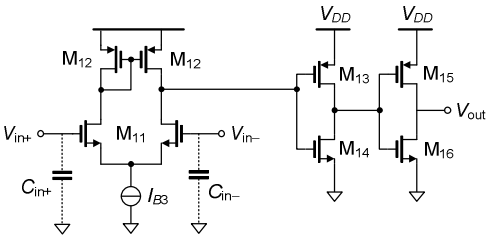

Figure 6. Comparator circuit

TABLE I. TRANSISTOR DIMENSIONS

MOSFET	W [µm]	L [µm]
M_1, M_4, M_6, M_9	24	6
M_2, M_3, M_5, M_7, M_8, M_{10}	3	3
NMOS M_H (C_H)	11	11
M_{11}	6	3
M_{12}	3	3
M_{13}, M_{14}, M_{15}, M_{16}	0.5	0.35

IV. CIRCUIT SIMULATION

The PID circuit has been designed to be implemented in AMIS 0.35µm CMOS process technology. The bias current of the comparator is set to I_{B3}= 50nA. The total bias current becomes 720 nA (excluding that of the bias generator circuit). This results in a static power consumption of 864nW. Dimensions of the MOS transistors used are listed in Table I. The transistors are largely sized to alleviate the mismatch problem of MOS transistors in weak inversion.

Fig. 7 demonstrates the transient response of the proposed PID circuit in the worst case detection (see Fig. 3c) for a sinusoidal differential input current with an amplitude of 80 nA, a 5 kHz frequency and a 100kS/s sampling frequency. The input current and the holding current are shown on the top by the dotted and solid lines, respectively. There are large transient glitches appearing at the beginning of the holding

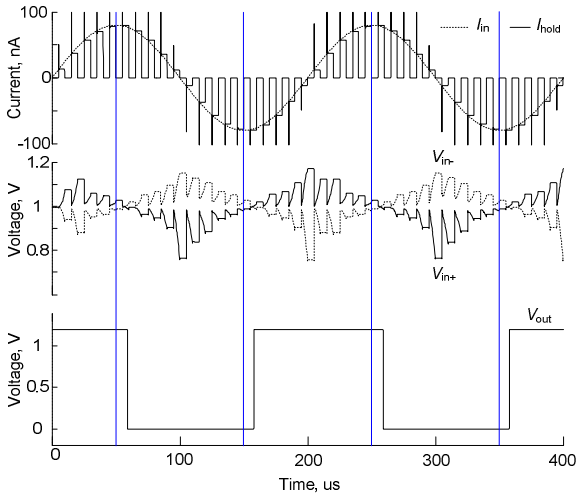

Figure 7. Signal swings within the proposed PID circuit.

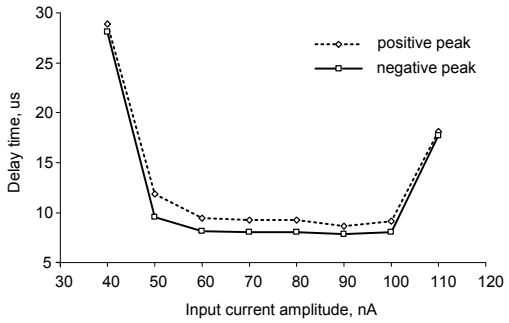

Figure 8. Delay time versus input amplitude

phases but they do not affect the corrected circuit operation. In the middle graph, we can see that the voltages at the input nodes of the comparator are swinging up and down crossing each other within the first holding period after the peak occurred. This operation is consistent with the theory explained in Sec. IIIA but, as we can see from the output waveform V_{out} shown in the bottom graph, the comparator produces an additional time delay. Also it can be seen that the delay time for the negative peak is slightly shorter.

In Fig. 8, it is indicated that the delay times of the PID circuit for both positive and negative peaks depend on the input amplitude. For very small input amplitudes less than 50nA the proposed circuit gives a delay time bigger than 10us which is 5% of the period of the input signal. This is due to limited resolution of the comparator. For the range of input amplitude of 50nA to 100nA, the delay time remains less than 5% of the input signal period. The delay time goes up again for the input amplitude higher than 100nA. This is not because of a limitation of the comparator but of the SHA. As the internal voltage swings at the input of G_m go too high, the charge injection error cannot be completely cancelled out leading to a wrong decision of the comparator.

Since the mismatch in weak inversion is worse than in strong inversion, a Monte Carlo simulation has been performed to verify the circuit operation. For the same condition of the transient response shown in Fig. 7, with 300 runs, it gives the mean values ($\langle x \rangle$) and standard deviation (σ) of 8.8μs and 2.16μs for the positive peak and $\langle x \rangle$ = 8.2μs and σ = 2.4μs for the negative one. These numbers indicate that the delays spread around 5% of the input signal's period.

V. Conclusions

An ultra low-power PID designed for a PL-PP BE processor has been presented. The instants detected are delayed within less than one clock period even if the transistors' mismatch is taken into account. Either the rising or the falling edges of the output signal together with the input signal amplitude are expected to be used as control parameters in a stimulator for cochlear epical electrodes which operates in the frequency range of 300Hz-5kHz.

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