A Least-Voltage Drop High Output Resistance Current Source for Neural Stimulation

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Abstract—**This paper presents a feedback technique to increase the output resistance of a MOS current mirror circuit that requires only one effective drain-source voltage drop. The proposed circuit requires a few additional current braches to form two feedback loops. With its compact structure, the proposed circuit is suitable as a current generator for neural stimulation. Simulation results, using 0.35 μm AMIS I3T25 technology, show that the proposed current generator, applied for bi-phasic stimulation, can convey more charge to a series resistive-capacitive load compared to the widely use low-voltage cascode current source.**

I. INTRODUCTION

Implantable neural stimulators can be effective for the treatment of many pathologies. Examples of applications include cochlear implants [1], retinal implants [2], deep brain stimulators [3] (to treat for example, Parkinson's disease) [4] and many other applications. From an electrical point of view neural stimulation essentially means conveying a particular amount of charge into the tissue.

Because the stimulators are implanted inside the body, there are very strict requirements on the size and power consumption of the device. Therefore it is important to be able to convey as much charge as possible into the tissue while using an as low as possible voltage supply to minimize power consumption. This paper discusses a novel method to maximize the charge transfer for constant current neural stimulators. To do this the output impedance of the current source is maximized using a double loop feedback topology.

The paper is organized as follows. In Sec. 2 a basic discussion is presented on constant current stimulation and the need for a high output impedance is explained. In Sec. 3 the working principle and performance limitation of the existing systems are discussed, while in Sec. 4 the circuit design of the architecture proposed in this paper is described. Sec. 5 shows the simulation results when the proposed and existing circuits are applied as neural stimulators. Finally, in the last section, this work will be summarized.
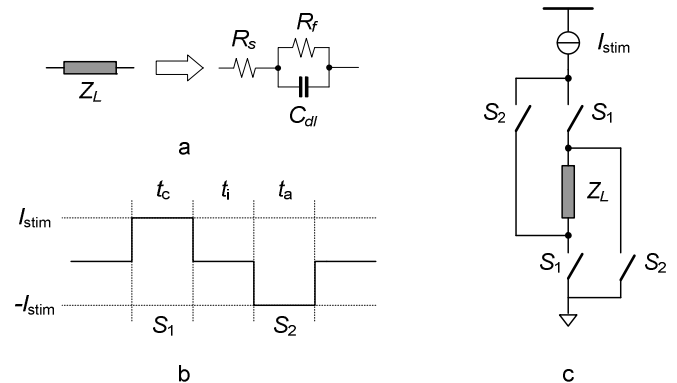

Figure 1. Biphasic current stimulation concept

II. CONSTANT CURRENT STIMULATION

To understand the underlying principles of electrical stimulation, the tissue can be modeled in the electrical domain. Despite the fact that the tissue shows a highly non-linear and non-stationary response, it can be modeled to a first approximation using the linear model Z_L depicted in Fig. 1a [5]. Here R_s corresponds to the resistance of the tissue, while C_{dl} and R_f correspond to the interface between the electrode and the tissue.

Since stimulation comes down to lifting the potential of the tissue either above or below a particular threshold and the tissue can be modeled as being merely capacitive in nature, stimulation performs inserting a particular amount of charge into the tissue. This makes charge the most fundamental quantity for neural stimulation. When charge is built up at the electrodes, electrolysis will start to occur at the interface [6]. This will damage the tissue and therefore it is important to remove any charge built up at the electrodes. Charge cancellation can be conveniently achieved by the stimulation scheme called constant current stimulation [7].

The principle of constant current stimulation can be described using Fig. 1b. During the first stimulation phase S_1, a particular amount of charge $Q_1 = I_{stim} \cdot t_c$ is injected. This
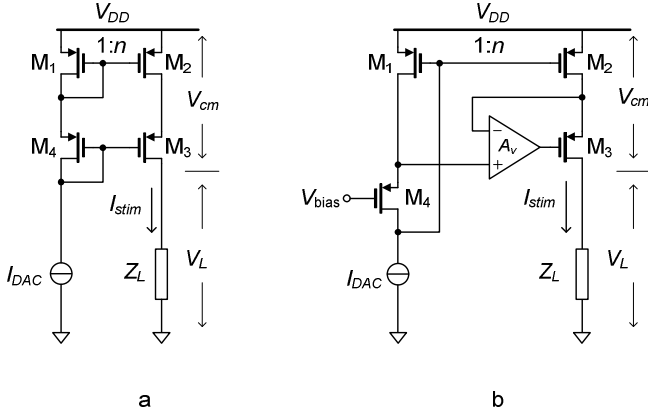
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Figure 2.   Cascode current sources a) simple cascode b) regulated cascode

Figure 3.   Proposed circuit

should either generate or block an action potential. After a short inter-pulse interval t_i, the second pulse is injected for which $Q_2 = I_{\text{stim}} \cdot t_a$. If $Q_1 = -Q_2$, charge cancellation is assured. Therefore in this case the amount of charge can be easily controlled by the pulse duration.

In Fig. 1c the circuit principle for constant current stimulation is depicted. The switches allow the current to reverse its direction in between the two stimulation phases S_1 and S_2. The advantage of using switches over a schematic using positive and negative current sources is that only a positive supply voltage is needed. To ensure charge cancellation, it is important that the current through the tissue remains constant during both stimulation phases. When capacitor C_{dl} is charged, the tissue voltage is increasing. To maintain a constant current through the tissue, it is important to have a current source with an output impedance as high as possible.

III. HIGH OUTPUT RESISTANCE CURRENT SOURCES

When current mirror circuits are used as current generators for neural stimulation, a cascode connection is needed to have sufficiently high output resistance [8]. Fig. 2a shows the simplest version of a PMOS cascode current mirror. A low reference current I_{DAC} is usually generated from a digital to analog converter and is applied through the diode connected transistors in the left branch (M_1 and M_4). Subsequently, the current is scaled up by a factor of n to become the stimulation current flowing through transistors M_2, M_3 in the right branch and load Z_L. In this case, the output resistance is many times higher than that of a simple current mirror (without the cascode connection). However, the minimum required voltage across the current source (voltage compliance, V_{cm}) becomes one source-gate voltage (V_{SG}) plus one effective source-drain voltage (V_{eff}). This limits the voltage head room V_L and the amount of charge conveyed to the tissue (load).

To increase V_L thereby reducing V_{cm}, opamp A_v is applied to equalize the drain voltages of the transistors at the top of
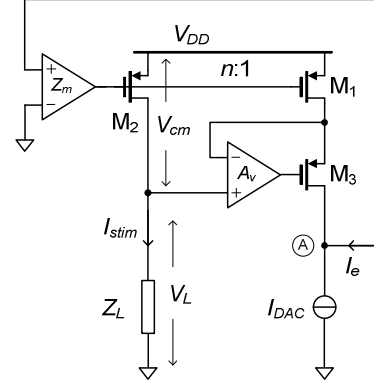
the circuit in Fig. 2b (M_1 and M_2). Regulated by the large voltage gain of A_v, the aforementioned condition for V_{cm} becomes $V_{\text{eff3}} + V_{\text{eff2}}$. Due to the fact that the output resistance of this mirror is higher than in the previous cases but requires less V_{cm}, this cascoded structure is popularly used in neural stimulation [9]-[10].

IV. PROPOSED CURRENT SOURCE

In order to allow for an even higher V_L, yielding a higher amount of charge conveyed to the tissue, we propose a new high output impedance current source that requires V_{cm} to be only a single V_{eff}. The concept of the proposed current source is shown in Fig. 3. It contains two feedback loops. The first internal one is used for high precision down scaling of I_{stim} (to I_{stim}/n). This current will be compared with I_{DAC} and error current I_e will be forced to be zero by the large loop gain of the second global feedback loop creating a relationship of

$$I_{\text{stim}} = nI_{DAC}. \tag{1}$$

Let's take a closer look at the internal loop. Transistor M_2 generates I_{stim} flowing through Z_L. The gate terminal of transistor M_1 is connected to the gate terminal of M_2 to accurately scale down the current flowing through M_3 to summing node A. Based on the same principle used for the current mirror of Fig. 2b, A_v is used to force the drain terminals of M_1 and M_2 to be equal, resulting in a very precisely copied current I_{stim}/n flowing into node A. The voltage headroom of node A is limited by $V_{DD} - V_{\text{eff3}} + V_{\text{eff1}}$ (the same as the mirror in Fig. 2b) but this does not create any problem since the impedance seen when looking into this node will be forced to be very low and the node voltage will be fixed by the global feedback loop.

The global feedback loop starts from node A. Error current

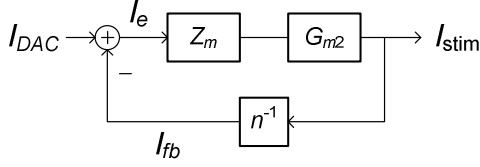$$I_e = \frac{I_{\text{stim}}}{n} - I_{DAC}, \tag{2}$$

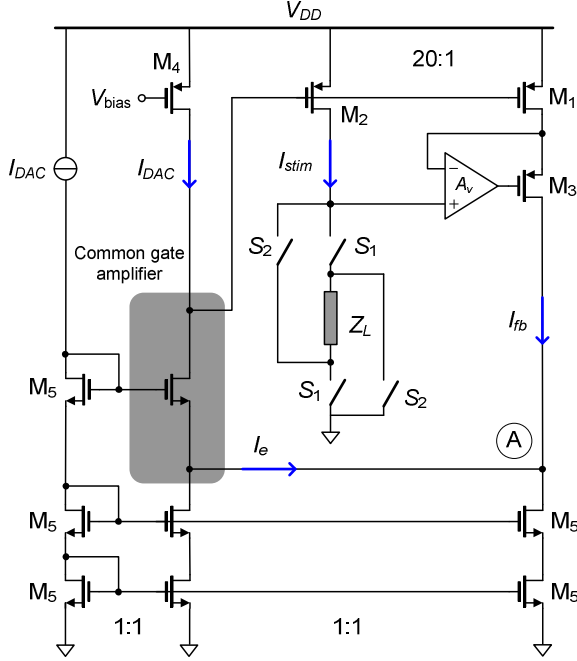Figure 4. Feedback block diagram of the proposed circuit

Figure 5. Current stimulator

flows into transimpedance amplifier Z_m converting the very small I_e into the voltage needed at the gate of M_2 to produce I_{stim} (where the loop is closed). Assuming the inner local feedback loop works perfectly, we can simplify the feedback block diagram of the proposed mirror circuit as shown in Fig. 4. From the block diagram, loop gain LG of the system can be found as

$$LG = \frac{G_{m2}Z_m}{n},\qquad(3)$$

where G_{m2} is the transconductance gain of transistor M_2.

To maintain the desired current presented in (1), LG needs to be as large as possible. Since G_{m2} is limited by the values of I_{stim} and the dimension of M1 and n is preferred to be high (10-100) to keep the total power consumption low, a large Z_m becomes the main factor that defines the accuracy of the proposed circuit.

Fig. 5 shows the circuit schematic of the proposed current stimulator. The double cascode current mirror M_5 provides two functions: 1) generating a copy of I_{DAC} and 2) forming the common gate (CG) amplifier (shown in the shaded area) which is used to realize the transimpedance

amplifier. V_{bias} is applied to the gate terminal of M_4 to provide an active load for the CG amplifier. In this case, the voltage at node A is kept at $2V_{GS5}$. The transimpedance amplifier provides

$$Z_m \cong r_{o4},\qquad(4)$$

where r_{o4} is the small signal output resistance of M_4.

Switches S_1 and S_2 are applied to allow for biphasic stimulation. The charge and discharge times can be controlled by the switching periods.

V. Circuit Simulation

To verify the proposed concept, the CMOS I3T25 AMIS technology (0.35μm) which allows a supply voltage as high as 18V is used for circuit simulations. The current sources in Figs. 2a, 2b and 5 are designed to generate a 1mA stimulation current to Z_L via ideal control switches S_1 and S_2 arranged in the same way as shown in Fig. 5. All transistors are high voltage devices and the dimensions are indicated in Table 1. Note that not all the transistors need to be high voltage devices. Some of them can be replaced by low voltage devices to reduce area. In this case, we used high voltage devices for easy verification. V_{DD} is set at 18V and I_{DAC} is 50μA, yielding $I_{stim} = 1$mA with a scaling factor of $n = 20$. Ideal op-amps with a gain $A_v = 200$ are used for the circuits in Figs. 2b and 5. Z_L is realized by a 10kΩ resistor connected in series with a 10nF capacitor which approximately models an auditory nerve electrode tissue [11]. The pulse widths for t_c, t_i and t_a are set equally to 100μs with a period of 2ms.

Fig. 6 shows the transient simulation presenting the currents flowing trough Z_L from three different current stimulator architectures: the simple cascode (Fig. 2a), the low-voltage cascode (Fig. 2b), and the proposed circuit. What we can see is that all three current generators work well for negative pulses but the waveforms of the positive pulses are distorted. This is due to the voltage headroom limitation. During the first stimulation phase, the tissue voltages will clip to the voltage compliance of the current sources as will be shown shortly. During the second phase the tissue terminals are switched, yielding a much lower starting voltage and therefore there is no clipping.

Fig. 7 magnifies Fig. 6 to give more detail on the limitation of the current sources. The solid line represents the stimulation current from the circuit of Fig. 5. The dotted and dashed lines represent the stimulation currents from the circuits of Figs. 2a and 2b respectively. It is clear from the range of $2.04\text{ms} \leq t \leq 2.1\text{ms}$ that the stimulation current obtained from the proposed current source can be kept constant for a longer time than those of the others. This verifies that the proposed current source provides high output resistance for a wider range of voltage headroom.

Fig. 8 shows the voltages across Z_L obtained when the currents in Fig. 7 are flowing through them. The highest

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voltage across the load (solid line) is obtained from the proposed current generator. The middle result represented by the dotted line is from the circuit in Fig. 2b and the lowest one is from the simple cascode current generator. This also confirms that the proposed circuit can convey more charge to the tissue.

VI. CONCLUSIONS

We have proposed a high output resistance current source that requires a very small voltage compliance. This is achieved by applying dual loop negative feedback that continuously monitors the voltage across and the current flowing through the load. The monitored signals are fed back to control the gate voltage of the transistor that generates the output current directly. As a result, the output resistance and the accuracy of the current source are regulated by the system loop gain. The main benefit we achieve for neural stimulation is the larger amount of charge that can be conveyed to the stimulation electrode. In other words, for the same amount of charge required, the supply voltage can be reduced.

ACKNOWLEDGMENT

REFERENCES

[1] J. Georgiou and C. Toumazou, "A 126 µW cochlear chip for totally inplantable system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 430-443, 2005.

[2] S. C. De Marco et al., "An arbitrary waveform stimulus circuit for visual protheses using a low area multibias DAC," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1679-1690, 2005.

[3] M. M. van Dongen and W. A. Serdijn, "Design of a versatile voltage based output stage for implantable neural stimulators," , *IEEE Latin American Conference on Circuits and Systems (LASCAS)*, Brazil, Feb. 2010.

[4] A. Benabid, et. Al., "Deep brain stimulation for Parkinson's disease," *Advances in Neurology*, vol. 86, pp. 405-412, 2001.

[5] E.T. McAdams and J. Jossinet, "Nonlinear transient response of electrode-electrolyte interfaces", Medical & Biological Engineering & Computing, Vol. 38, pp 427-432, 2000.

[6] J. Lily, J. Hughes, E. Alvord, and T. Galkin, "Brief noninjurious waveforms for stimulation of the brain", *Science*, Vol. 121, pp. 468-469, 1955.

[7] M. Ortmanns, "Charge balancing in functional electrical stimulators: A comparative study," *IEEE International Symposium on Circuits and Systems*, pp. 573–576, May 2007.

[8] M. Ghovanloo and K. Najafi, "A compact large voltage compliance high output impedance programmable current source for implantable microstimulators," *IEEE Tran. Biomed. Eng.*, vol. 52, pp. 97-105, Jan. 2005.

[9] M. Sivaprakasem, W. Lui, M. S. Humayun, and D. J. Weiland, 'A variable range bi-phasic current stimulus driver circuitry for an implantable retinal prosthesis device," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp 763-771, Mar. 2005.

[10] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors," *IEEE Tran. Biomedical Circuits Systs.*, vol. 2, no. 3, pp. 231–244, Jan. 2008.

[11] J. J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balance electrode stimulator chip with less than 6nA DC error for 1mA full-scale stimulation," *IEEE Tran. Biomedical Circuits Systs.*, vol. 1, no. 3, pp. 172–183, Jan. 2007.

TABLE I. TRANSISTOR DIMENSIONS

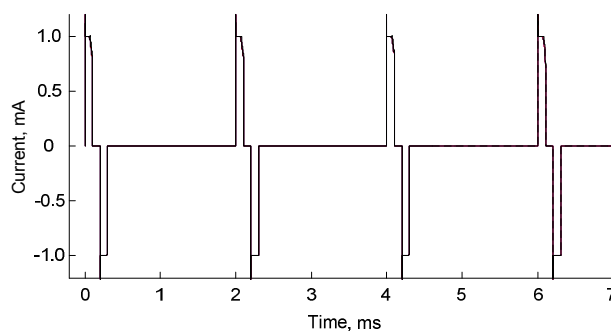| MOSFET	W [µm]	L [µm]
M1, M3, M5	5	1.6
M_2, M_4	100	1.6

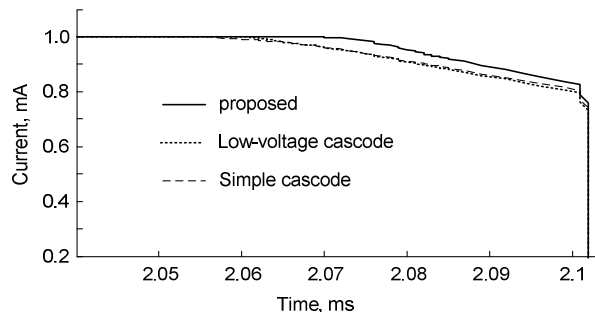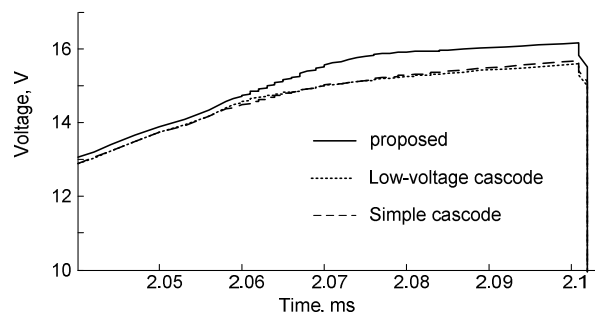Figure 6. Stimulation current waveforms

Figure 7. Magnified stimulation current waveforms

Figure 8. Voltages across loads