A Compact, Nano-Power CMOS Action Potential Detector

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***Abstract*—Real time action potential (AP) detection is an important requirement for development of fully implantable neuroprosthetic devices. We present an ultra low-power CMOS analog circuit for detection of APs embedded in a noisy signal. The proposed strategy isolates APs by detecting subsequently a positive and a negative spike of each AP. An AP is detected only if the positive spike is detected within a short period of time after the negative spike was detected. The proposed circuit has been designed to be implemented in AMIS 0.35 μm technology (I3T80) and has been verified in Cadence using RF spectre. The final circuit operates from a 1-V supply and consumes only 1.5 nA. The detector is verified by means of simulations with synthetic neural waveforms and is able to successfully detect APs in noisy signals.**

***Index Terms*—analog integrated circuits, action potential detector, biomedical signal processing, CMOS, extracellular recordings, low-voltage, multichannel recordings, prosthetic devices, ultra low-power**

I. Introduction

Neuroscientists and neuroprosthetic devices require often real-time monitoring of biopotential activity of multiple neurons. Due to advances in microelectrode array technology, sensing devices of 100 or more electrodes are possible [1]. Efforts to develop fully implantable sensing devices bring along several circuit design challenges. Such clinical devices need to be as less intrusive as possible. Recorded data needs to be transmitted wirelessly to avoid tissue infections. Yet the power consumption of small implantable devices needs to be minimized to prevent heating and damage to nearby cells. Safety, power consumption and limited area are important parameters that need to be satisfied.

In scientific and neuroprosthetic devices, there is a need to automatically detect APs from each electrode. By detecting APs in low density neural waveforms and transmitting only relevant data, we can greatly decrease the power consumption of implantable devices [2]. Alternatively, automatic AP detection can be used to trigger recording around each AP [3]. By detecting APs close to the electrodes we can also help classifying APs and distinguish between different neurons. The remaining problem is how to perform this automatic AP detection from a noisy neural waveform in a small, low-power device.

In a typical AP detector, the signal is preprocessed to attenuate noise and to accentuate spikes. Subsequently, a threshold detector is used to determine spike locations [4]. Adaptive threshold spike detectors monitor the background noise and automatically adapt the threshold according to the noise level [5], [6]. Although simple thresholding detectors tend to be sensitive to noise, they remain attractive for real-time implementations because of their minute computational time. The efficacy of simple and adaptive threshold detectors is reduced by overlapping spikes.

Energy based spike detectors have also been used to detect APs [3], [7], [8], [9], [10], [11]. The nonlinear energy operator (NEO), also called the Teager energy operator, first characterized by Kaiser [12], estimates the square of the instantaneous product of amplitude and frequency of the input signal. In this regard, the NEO may be superior to other energy estimators as it explicitly takes frequency into account. However for low power multichannel applications, it is outperformed by simple threshold AP detectors [13].

Matched filter (MF) detectors are particularly effective when the spike waveform to be detected is already known. Since this is often not the case, the user must manually select a template [14]. Moreover, these detectors tend to exceed the limited chip area and power consumption. Besides, their computation time may preclude them in real-time multichannel detectors [4]. If the system is not limited by its power consumption, a matched filter with a non-specified template will be the detector of choice. [13].

Our strategy is to combine the simplicity of a simple threshold detector with the performance of semi MF detectors. We compare three predefined AP features with the measured signal. The AP is detected only if a positive peak is detected in a predefined time after a negative peak was detected. This "dual threshold" AP detection algorithm was originally proposed in [15], including additional filtering.

In this paper, we present an ultra low-power circuit for dual threshold AP detection. Its principle and system level design are reviewed in Section 2. In Section 3, the design of the AP detector circuit employing CMOS transistors operating in the subthreshold region is given. Section 4 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 5.

II. Proposed Dual Threshold AP Detector

The dual-threshold algorithm attempts to detect AP's in noisy signals by subsequently detecting the positive and the negative peaks of each AP. Occasional noise peaks will not

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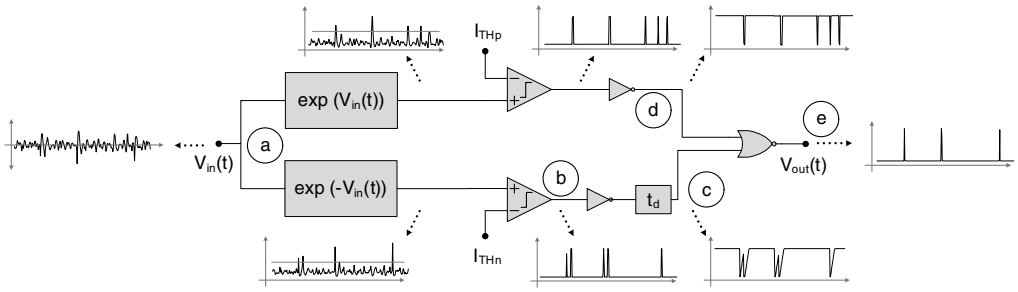

Figure 1. Blockdiagram of the proposed dual threshold AP detector.

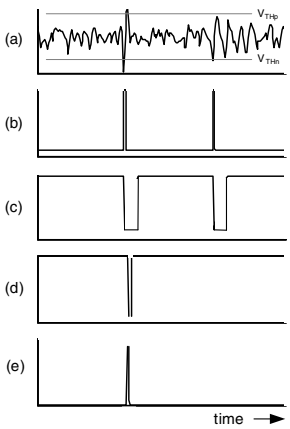

Figure 2. Waveforms at the various nodes in the AP detector. (a) Input neural waveform. (b) Negative peak, lower than V_{THn} is detected. (c) Detected negative peak LP filtered. (d) Detection of positive peak if the input signal is higher than V_{THp}. (e) In case (c) and (d) occur at the same time, an AP will be detected.

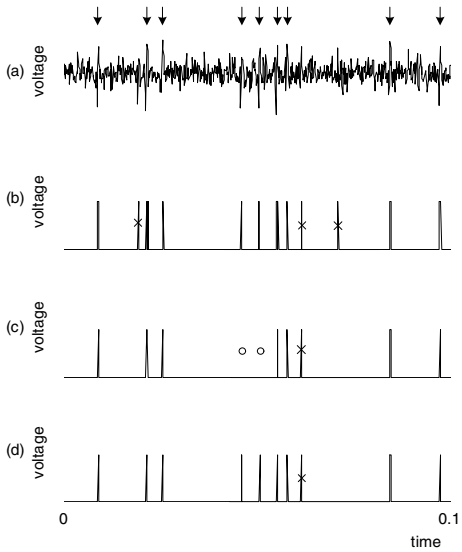

Figure 3. Transient response of three different algorithms. (a) Input neural waveform. (b) NEO response. (c) ATA response. (d) DTA response. O = false negative, X = false positive.

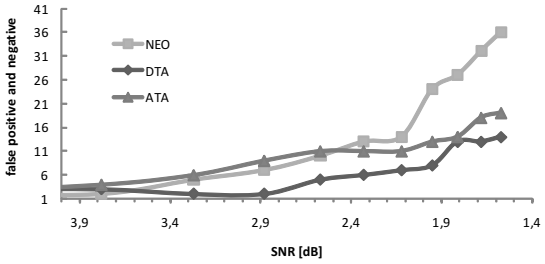

Figure 4. Performance comparison of three different algorithms

trigger the AP detector and incidental detection of false positives and false negatives will be minimized.

Fig. 1 shows the block diagram of the detector. It comprises 8 building blocks: two simple pre-processors, two comparators, two inverters, a delay t_d and a NOR logical gate. The two nonlinear pre-processors extract the input signal, enhancing the difference between the peaks and the noise level. Comparators are used with threshold levels I_{THp} and I_{THn} that can be adjusted separately. A delay is applied to hold the detected negative peak signal for a particular time. Its time constant depends on the AP duration. Finally, the NOR gate performs a logical NOR on the inverted positive peak detected and the delayed output signal. It produces a logical "true" when an AP is detected. A logical "false" is produced in the absence of AP's.

Fig. 2 illustrates the waveforms at the various stages in the detector. In Fig. 2a we see the input signal. Fig. 2b illustrates the detection of the negative peak. The inverted and delayed version of the detected negative peak signal is shown in Fig. 2c. Inverted detection of the positive peak is shown in Fig. 2d. Detection of the AP is depicted in Fig. 2e.

To verify the performance of the dual threshold algorithm (DTA), we compare it to the NEO and adaptive threshold algorithms (ATA) as described in [5]. As test signal we use a synthetic signal made from a real waveform sampled at 30 kHz. AP shapes are extracted from the real waveform and randomly distributed according to the Poisson law with variable firing rates. Subsequently, white noise, band-limited at 7 kHz, is added to emulate various SNR's.

Fig. 3 shows the transient responses of the three algorithms. The signal of Fig. 3a has SNR of 2.9 dB and is applied to each algorithm. Fig. 3b represents the output of the NEO. The output of the ATA can be seen in Fig. 3c. Finally, in Fig. 3d, the output of the DTA, described in this paper, is depicted. We can see that false detections of the DTA are less likely to occur than in the case of the NEO and the ATA.

Fig. 4 indicates the performance of the different detectors as the SNR ratio is decreasing. At high SNR ratios, the

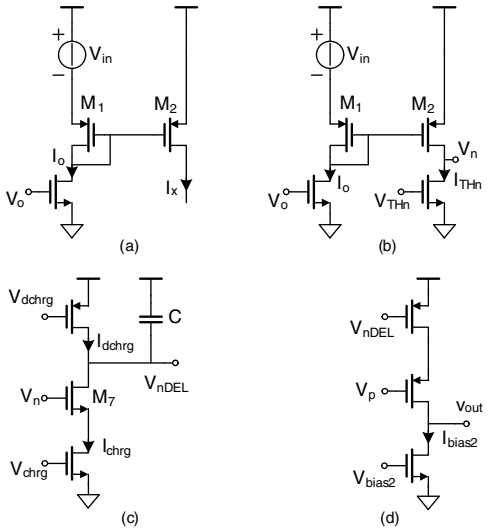

Figure 5. (a) Simple pre-processor performing mathematical exponential operation. (b) Implementation of current comparator. (c) Delay circuit. (d) NOR-gate analog implementation.

NEO shows good performance. As the SNR decreases, the performance degradation of the NEO becomes more severe than that of the other two detectors. ATA and DTA have the same performance in case of high SNR. As the SNR decreases, we can see that DTA outperforms ATA.

III. Dual Threshold Detector Building Blocks

A. Pre-processors

Fig. 5a shows the circuit implementation of the pre-processor. Using the exponential relationship of PMOSTs operating in weak inversion [16], for $V_{DS} \geq 4U_T$ (a condition to keep the devices in weak inversion saturation) and $V_{SB} = 0$ (source and body terminals are connected), it follows

$$I_D = I_{D0} \exp\left(\frac{V_{SG}}{nU_T}\right), \tag{1}$$

where

$$I_{D0} = I_S \left(\frac{W}{L}\right) \tag{2}$$

and I_S is the zero bias current for a unit transistor, n is the sub-threshold slope factor and U_T is the thermal voltage while W, L, V_{SD}, V_{SB}, and V_{SG} have their usual meaning. From Fig. 5a we can find that

$$V_{SG2} = V_{SG1} + V_{in}. \tag{3}$$

Substituting (3) into (1) we get

$$I_x = I_o \exp\left(\frac{V_{in}}{nU_T}\right), \tag{4}$$

which clearly states the exponential relation between input voltage and output current depending on bias current I_o, which is set by the voltage V_o.

B. Current comparators

Implementation of the current comparator is performed by adding a current source I_{THn}, set by V_{THn}, to the exponential pre-processor output node, as shown in Fig. 5b. In case $I_{\text{THn}} > I_x$, V_n will become 0V. Otherwise it will be V_{DD}, as illustrated in Fig. 2d.

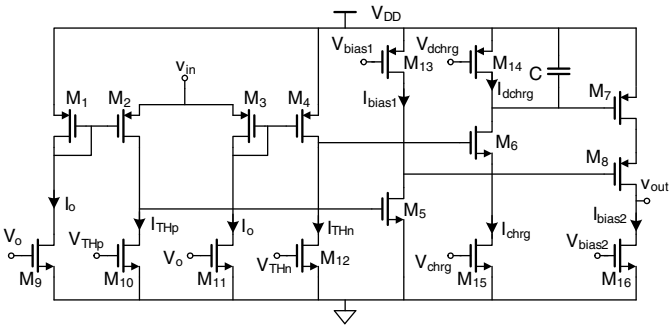

Figure 6. Dual threshold AP detector circuit.

C. Delay circuit

Fig. 5c shows the implementation of the delay circuit. Transistor M_7 acts as a switch. In case $V_n = 0$V, M_7 will be open and we have

$$I_{dchrg} = C\frac{dV_{\text{nDEL}}}{dt}. \tag{5}$$

Slightly rewriting (5), we can find the discharging slope

$$\frac{dV_{\text{nLPF}}}{dt} = \frac{I_{dchrg}}{C}. \tag{6}$$

In case $V_n = V_{DD}$, in charge mode, M_7 will be closed and we have a different situation. The charging slope is then defined as

$$\frac{dV_{\text{nLPF}}}{dt} = \frac{I_{chrg} - I_{dchrg}}{C}. \tag{7}$$

The threshold voltage of M_7 and the discharging slope determine the delay time t_d, where $I_{chrg} >> I_{dchrg}$. Voltages V_{chrg} and V_{dchrg} are setting I_{chrg} and I_{dchrg}, respectively.

D. NOR-gate

The circuit diagram of the NOR-gate is depicted in Fig. 5d. Current I_{bias2} , set by the voltage V_{bias2}, will flow only if both inputs V_p and V_{nDEL} are low. This will pull down the voltage at V_{out} and it becomes 0 V. Otherwise, current will not flow and $V_{out} = V_{DD}$. Fig. 2e illustrates the output of the NOR-gate.

The complete circuit diagram of the AP detector can be found in Fig. 6. It is a combination of the building blocks from Fig. 5. An inverter, formed by M_5 and M_{13}, is inserted for pre-conditioning of the NOR gate to achieve the desired operation from the detector.

IV. Simulation Results

The operation of the AP detector circuit was verified in Cadence using RF spectre and AMIS 0.35 μm technology (I3T80). MOS transistor widths (W) and lengths (L) were set as $W/L_{1-8} = 3\,\mu\text{m}/10\,\mu\text{m}$ and $W/L_{9-16} = 3\,\mu\text{m}/7\,\mu\text{m}$. Supply voltage $V_{DD} = 1$ V. At $37\,^{\circ}C$ the quiescent power consumption equals 1.5 nW and the average power consumption over 200 ms equals 1.8 nW. Capacitor $C = 3$ pF.

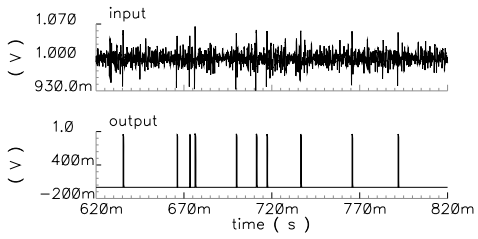

Figure 7. Transient response of the DTD in case input signal SNR of 6 is used.

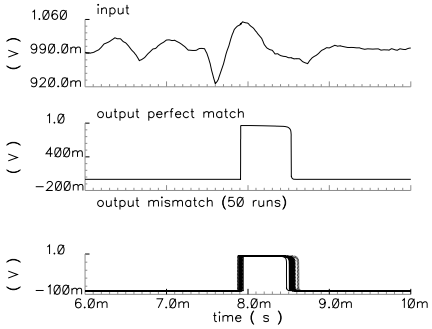

Figure 8. Monte Carlo simulation zoom in. Input signal SNR of 10.

The various current source values are given in Table 1. The threshold currents I_{THp} and I_{THn} are selected such that there is an almost equal minimum number of false positive and false negative detections over the time period of 200 ms.

Fig. 7 shows the transient response of the dual-threshold detector (DTD) circuit. It can be seen that the detector is able to successfully isolate APs from the noisy signal.

A Monte Carlo simulation of 50 runs over the period of 200 ms is performed. Zoomed-in version of a single AP detection for two different input signal-to-noise ratios (SNR) are depicted in Fig. 8 and Fig. 9. As we can see, mismatch variations have bigger influence on the circuit operation in case SNR decreases. For the input signal with SNR = 6, we can see that one false detection occurred in 50 runs.

V. Conclusions

In this paper, a dual-threshold action potential detection circuit to be used in real-time applications has been presented. The CMOS version of the resulting circuit comprises one capacitor and a handful of transistors. Simulations show that

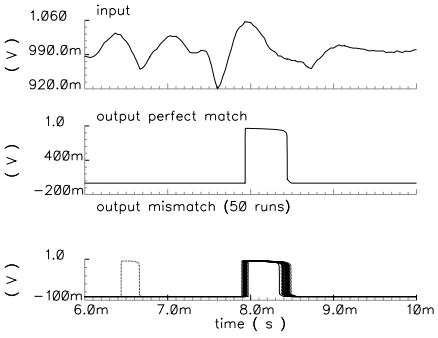

Figure 9. Monte Carlo simulation zoom in. Input signal SNR of 6.

Table I
Current sources

source	I_{o}	I_{THp}	I_{THn}	I_{bias1}	I_{bias2}	I_{chrg}	I_{dchrg}
I [nA]	0.37	0.85	0.72	0.71	0.5	103	1.9

the proposed circuit consumes very little power and is able to reliably detect the action potentials in the input signals even in case of very limited SNR. Thanks to the compact circuit architecture and the low power consumption, the proposed circuit is a good candidate for multi-electrode spike detection.

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