Energy-Efficient Low-Power Circuits for Wireless Energy and Data Transfer in IoT Sensor Nodes

Gustavo C. Martins, *Student Member, IEEE,* Alessandro Urso, *Student Member, IEEE,* André Mansano, *Member, IEEE,* Yao Liu and Wouter A. Serdijn, *Fellow, IEEE*

***Abstract*—In this paper, we present techniques and examples to reduce power consumption and increase energy efficiency of autonomous wireless sensor nodes for the Internet of Things. We focus on RF energy harvesting and data transfer, all of which have a large impact on the device cost, lifetime and functionality. We explore the co-design of antenna and electronics to increase RF-DC conversion and efficiency and to improve the performance of the LNA. A high-efficiency orthogonally switching charge pump rectifier is presented. Its measurement results are presented, along with a discussion on how to define its power conversion efficiency. To boost the rectifier output voltage, while presenting the best output load to it, a DC-DC converter with maximum power point tracking is presented. To transmit slowly-varying signals in a low-power manner, an asynchronous data converter is discussed and two modalities of data transmission are presented. The first one is a passive transmitter implementation and the second a novel low-power sub-GHz UWB transmitter.**

***Index Terms*—Co-design of antenna and electronics, DC-DC converter, energy harvesting, Internet of Things, rectifier, UWB transmitter, wireless sensor nodes**

I. Introduction

WIRELESS Sensor Nodes (WSNs) are an important part of the Internet of Things (IoT). Every WSN of a network allows monitoring relevant parameters for a given application. Due to the increasing number of WSNs, the need for low cost devices is becoming larger and larger.

Batteries are still used as the main source of energy in WSNs. The disposal of batteries is an expensive and polluting process, and sometimes the cost of batteries is even higher than the cost of the electronics involved. Furthermore, WSNs that need replacement of batteries are not suitable to be used in areas where human access is very limited. For these reasons there is the need for autonomous WSNs that can be remotely powered.

With technology improvement, the power consumption of WSNs tends to reduce whereas the efficiency of energy harvesters tends to increase, as depicted in Fig. 1. However, the gap cannot yet be closed for most applications. To further illustrate this, Tables I and II present the typical power necessary for data transmission (the task that usually requires most of the power in a WSN) and the input available power of state-of-the-art energy harvesters, respectively. Further improvements in energy harvesting and data transfer must be achieved to close this gap. The purpose of this paper is to present and discuss the techniques that allow to bring the two curves of Fig. 1 as close as possible or even cross each other. We will show how the circuit techniques presented in the paper help achieving this task.

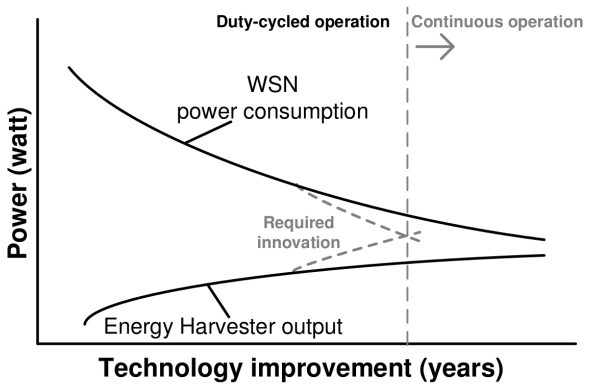

Fig. 1. Typical power consumption scenario of a WSN [1].

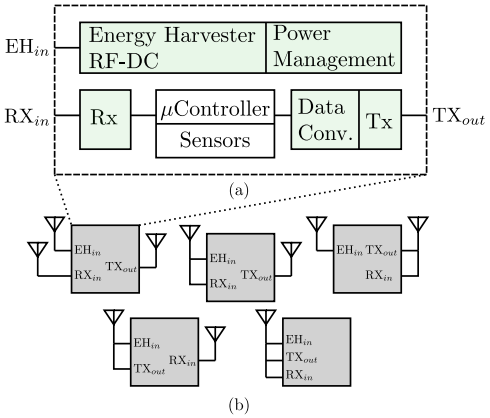

Fig. 2. (a) Detailed block diagram of an autonomous wireless sensor node. (b) 5 possible configurations based on the number of available antennas.

In Fig. 2, a general architecture of a typical autonomous WSN is depicted. When powered, the microcontroller reads and processes data from sensors, which can subsequently be sent to a transmitting antenna. The parts highlighted in green will be discussed in this paper, while the microcontroller unit and the sensors are considered to be complementary to the

G. C. Martins, A. Urso, A. Mansano, Y. Liu and W. A. Serdijn are with Delft University of Technology, Section Bioelectronics, Mekelweg 4, 2628 CD Delft, the Netherlands (email: g.c.martins@ieee.org, a.urso@tudelft.nl, yaoliuhust@gmail.com, amansano@gmail.com, serdijn@ieee.org)

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TABLE I
TYPICAL DATA TRANSMISSION POWER CONSUMPTION.

Work	Power consumption
[2]	123 mW (peak value)
[3]	1.3 mW
[4]	1.7 mW

TABLE II
STATE-OF-THE-ART ENERGY HARVESTERS INPUT POWER.

Work	Input power range	Peak eff.
[5]	$\sim 160\,\mathrm{nW}$-$19\,\mu\mathrm{W}$	40%
[6]	$\sim 19\,\mu\mathrm{W}$-$126\,\mu\mathrm{W}$	44.1%
[7]	$4\,\mu\mathrm{W}$-$13\,\mu\mathrm{W}$	11.5%

work presented here. In order to transmit and receive data and power from a WSN, an antenna or multiple antennas are needed. For the sake of simplicity, let's suppose that a node cannot transmit power to power up any of the other nodes, hence each node can use one, two or three antennas. As depicted in Fig. 2 (b), based on how the available antennas are connected, 5 different scenarios can be considered:

a) A WSN having one antenna. The antenna is shared among the transmitter, the receiver and the EH. In this scenario, these three blocks all have to work at the same frequency.
b) A WSN having two antennas. One antenna is used by the EH, while the other is shared among the transmitter and receiver.
c) A WSN having two antennas. One antenna is used by the transmitter, while the other is shared among the receiver and the EH.
d) A WSN having two antennas. One antenna is used by the receiver, while the other is shared among the transmitter and the EH.
e) A WSN having three antennas. One antenna for the receiver, one for the transmitter and one for the EH.

The e) scenario has the most degrees of freedom. This means that the most suitable frequency for each block can be used. For instance, the energy can be received at $13.56\,\mathrm{MHz}$, while the data can be transferred at higher appropriate frequencies, hence higher data rates can be achieved.

This paper is organized as follows. Section II discusses the RF to DC conversion and the power management unit. With respect to the Radio-Frequency Energy Harvester (RFEH) module, it is shown that the characteristic impedance of the antenna-electronics interface not necessarily has to be $50\,\Omega$. Therefore co-design of the antenna and the RFEH allows to boost the overall performance of the system. A topology of a charge pump rectifier and its design are presented. Measurements of the circuit and a new analysis of the power conversion efficiency is provided. To boost the rectifier output voltage and charge a storage capacitor, a DC-DC converter which employs a Maximum Power Point Tracking (MPPT) technique is presented. This allows to change the input resistance of the DC-DC converter in order to maximize the energy conversion efficiency of the power conversion chain.

In Section III, the concept of co-designing the antenna and the electronics for data reception is presented. Unlike the co-design of the antenna and the rectifier in an RFEH, we optimize the interface between the antenna and the LNA in this section. Circuit simulations prove once more that the overall performance of the system is improved. Section IV focuses on data conversion and data transmission. An asynchronous event-driven transmitter to lower the power consumption of a WSN is presented. It is designed with a level-crossing analog-to-digital converter. Moreover, the design of a novel low-voltage low-power sub-GHz Ultra-Wide-Bandwidth (UWB) transmitter is presented. Its mathematical analysis is provided and its correct operation is validated by means of circuit simulations and measurements.

Finally, in Section V, a summary of the paper and conclusions are given.

II. RF ENERGY HARVESTING AND POWER MANAGEMENT

RF energy harvesting can reduce costs of WSNs, enabling many applications in the IoT domain. To increase the output power of such a harvester, the efficiency of the power conversion chain must be optimized. Here we explore the antenna-rectifier interface, rectifier design and rectifier-load interface, keeping in mind that all stages contribute to the overall efficiency.

A. Co-design of antenna and rectifier

To maximize the power transfer from the antenna to the rectifier, their impedances must be matched. If an IC is directly connected with an off-chip antenna and the length between them is electrically short, the antenna and the circuitry can be directly matched without any intermediate stage(s). An optimum choice of antenna impedance Z_A and load impedance Z_L allows us to increase the voltage or current at the antenna load for the same available power at the antenna. As addressed in [8], one needs to design the electronic circuit for the largest quality factor of Z_L possible and subsequently co-design the antenna impedance for conjugate matching. This conclusion is a key point that needs to be considered during a co-design procedure. If Z_A is conjugately matched with Z_L, and the antenna resistance R_A is much smaller than the antenna reactance X_A, the load voltage can be approximated as:

$$V_L|_{R_A \ll X_A} \approx \sqrt{2P_{av}}\frac{X_A}{\sqrt{R_A}}, \tag{1}$$

which suggests that the output voltage is passively boosted by the presence of the antenna reactance, which forms an LC resonator with the load. Significant improvement of the rectifier input voltage for large values of Q can be achieved at the expense of bandwidth. This property is exploited in [5], where the input voltage of the RF energy harvester is effectively increased using a high-Q loop antenna. This voltage boost improves the rectifier sensitivity, meaning that a wireless sensor node with an RF energy harvester can be operated at a larger distance from the RF energy source.

In summary, the two conditions that need to be met for an optimum co-design are as follows. The first condition is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is related to the fact that, since the available input

TABLE III
RFEH COMPONENT VALUES

Device	Value	Device	Value
C_B	7.5 pF	C_{DC}	$\simeq$ 90 fF
C_D	19.5 pF	R_{DC}	350 kΩ
$C_{R,T}$	$\simeq$ 17 pF	C_{R1}, C_{R2}	9.7 pF
C_C	9 pF	M_1, M_2	750 μm/0.2 μm

power and the antenna load are fixed, the voltage at the load cannot be increased to an higher value only by means of proper antenna design. Therefore, one should determine at which impedance level conjugate matching should occur in order to further increase the load voltage or current.

B. Charge Pump Rectifier Topology

The RF power presented at the rectifier's input must now be converted into DC power, generating a DC output voltage in an efficient manner. The theoretical model and analysis of the rectifier designed in this work have been first presented in [9]. Fig. 3 shows the block diagram of the designed RFEH that comprises a passive voltage boosting network and an orthogonally switching charge pump rectifier (OS-CPR). The circuit diagram of the boosting network and on-chip OS-CPR are shown in Fig. 4(a) and Fig. 4(b). To adequately drive the OS-CPR, the boosting network delivers large swing control (V_{b+} and V_{b-}) and energy signals (V_{r+} and V_{r-}). The resonant circuit of the boosting network is modeled by the self-inductance of the antenna, L_A, its series resistance, R_A, and capacitance $C_{V,T}$, which is the sum of the on-chip tuning capacitances (C_D and C_B) and input capacitance of the rectifier ($C_{R,T}$). An inductive choke L_C provides a DC short at the input terminals of the rectifier to ensure a zero DC offset error at the input of the OS-CPR. In the boosting network design there is a trade-off between the value of $C_{V,T}$ and L_A. If L_A is made too large, to increase voltage gain, $C_{V,T}$ has to be very small. In such a case, the resonance frequency will be too sensitive to the rectifier input capacitance that changes with the load and input power. Moreover, increasing the value of L_A requires an inductor that is physically bigger and consequently has a bigger R_A, which limits the voltage gain of the boosting network.

The rectifier circuitry (of a single stage) is made up of PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and energy storage (C_{R1} and C_{R2}) [9]. In order to minimize bulk effects on the threshold voltage, isolated transistors are required. PMOS transistors are used rather than NMOS because of their intrinsic isolation with the substrate. Isolated NMOS devices are available in the chosen technology but a large area is required due to the deep N-Well and the isolation ring. Table III shows the component values of the designed RFEH.

Due to DC voltage differences within the stage, the transistors may conduct current in the backward direction in the phase they should be turned off. Known as flow-back current this effect reduces the efficiency of the rectifier. To reduce

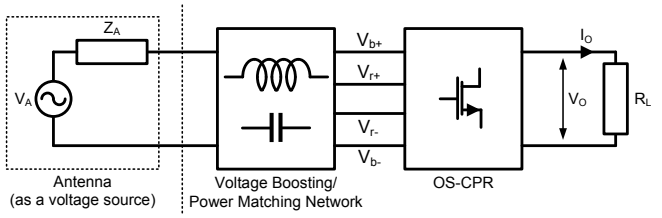


Fig. 3. Block diagram of the RF energy harvester [9].

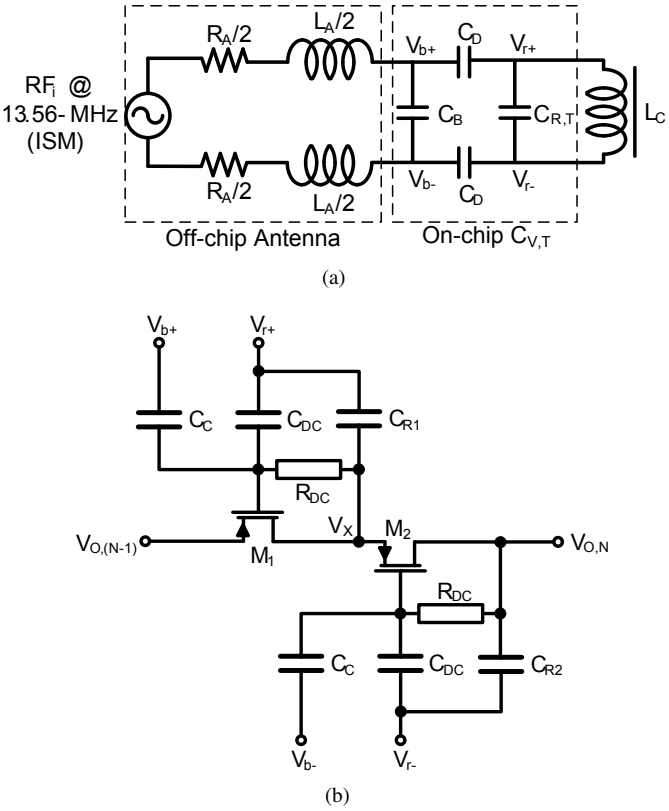


Fig. 4. Circuit diagram of (a) boosting network and (b) a single stage of the on-chip rectifier in the RFEH [9].

the flow-back current, capacitors C_{DC} and resistors R_{DC} set the DC voltages V_{CR1} and V_{CR2} at the gate of M_1 and M_2, respectively, to guarantee that the drain and source potentials are smaller than the gate potential in the off phase.

C. Measurement and Analysis of Power Conversion Efficiency

In this subsection, a new analysis of the power conversion efficiency of the rectifier is presented and compared with the state of the art EHs for IoT applications shown in Table II. First, three possible definitions of power efficiency are given and then discussed and compared. The measurements of the rectifier presented in the previous section are discussed.

The power conversion efficiency is the ratio between the power delivered to the load and the input power. Although the PCE definition is very clear, the input power can be defined in several ways. We recognize three definitions of input power to present PCE measurement results.

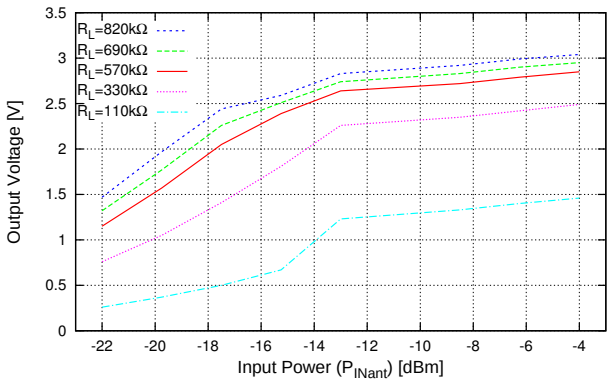


Fig. 5. Measured output voltage of the RFEH as a function of input power for $110\,\mathrm{k\Omega} \leq R_L \leq 820\,\mathrm{k\Omega}$

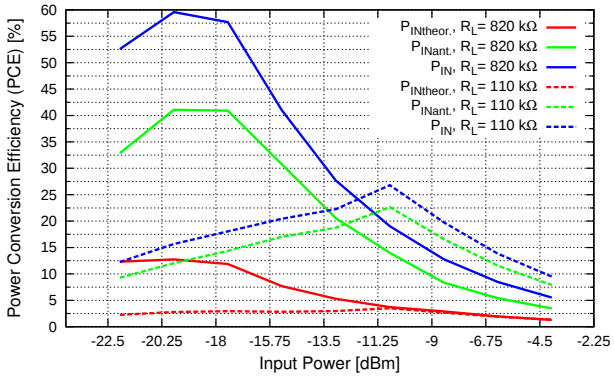


Fig. 6. Measured power conversion efficiency of the RFEH as a function of input power for $R_L = 110\,\mathrm{k\Omega}$ (dashed lines) and $820\,\mathrm{k\Omega}$ (drawn lines)

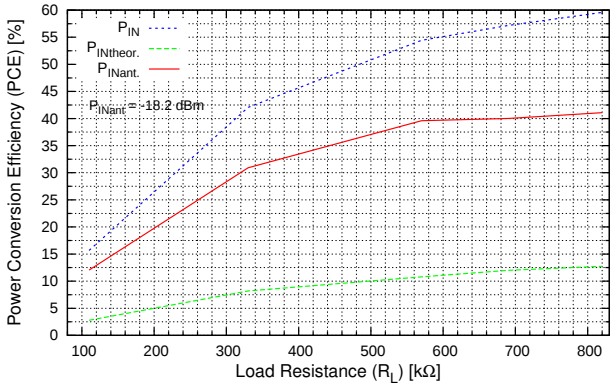


Fig. 7. Measured power conversion efficiency of the RFEH as a function of $\mathrm{R_L}$ for $\mathrm{P_{IN}} = -18\,\mathrm{dBm}$

The first definition is the *theoretical input power* ($\mathrm{P_{INtheor.}}$), which is the input power defined as $\mathrm{P_{INtheor.}} = \mathrm{V_A^2}/(2\mathrm{Re}\{\mathrm{Z_A}\})$. The second definition is the *measured input power at the antenna* ($\mathrm{P_{INant.}}$). The third definition is the *estimated input power at the rectifier circuit* ($\mathrm{P_{IN}}$). Most of the references on RF energy harvesting present the power conversion efficiency using $\mathrm{P_{IN}}$ as input power definition. Comparing the three definitions, PCE will be the lowest for the $\mathrm{P_{INtheor.}}$ since it does not take into account losses in the antenna and loading effects. The highest PCE is seen for an input power $\mathrm{P_{IN}}$ that takes into account all the losses in front of the input of the rectifier, therefore $\mathrm{P_{IN}}$ is smaller than $\mathrm{P_{INant.}}$ and consequently PCE is bigger.

The rectifier presented here has been implemented in silicon using AMS 0.18μm CMOS IC technology. In order to select the operating frequency of the rectifier, we analyzed the rectifier PCE in three different ISM bands: 13.56, 433 and $915\,\mathrm{MHz}$. The low frequency $13.56\,\mathrm{MHz}$ ISM band, compared to the others, presents better performance since at high frequencies the parasitic capacitances of the transistors add significant losses [9]. Moreover, at this low frequency more power can be radiated from the RF power source [10].

Table III shows the component values of the designed RF energy harvester for $N = 5$. For all the measurement results presented in this subsection, the RF power source at $13.56\,\mathrm{MHz}$ is calibrated for a distance of $10\,\mathrm{cm}$ (coupling factor of 0.004) between the antenna of the RF source and the antenna of the RF energy harvester. Fig. 5 presents the measured output voltage of the RFEH as a function of $\mathrm{P_{INant}}$ for $100\,\mathrm{k\Omega} \leq \mathrm{R_L} \leq 850\,\mathrm{k\Omega}$. From Fig. 5 it can be noticed that the output voltage increases with input power and $\mathrm{R_L}$, which means that a system powered by the RFEH has to operate from very little power, otherwise the sensitivity (minimum input power required for system operation) to the RF source is degraded.

One way of increasing the sensitivity is to increase the power conversion efficiency of the RFEH, which is not an easy task since the charge pump rectifier is a non-linear circuit that is sensitive to input power and load variations. Fig. 6 and Fig. 7 show the PCE behavior as a function of input power for different loads.

One can see that different PCEs are achieved for different loads and input power levels, which indicates that the design of the RFEH strongly depends both on its output power and on the power received by the antenna. The latter may change due to different coupling factors as a result of variations in distance and/or alignment of antennas.

In Table II, some energy harvesters already published in the literature have been listed. The input available power heavily depends on the source of energy used, therefore, when comparing this EH with the work in Table II, not only the peak power efficiency should be considered, but also the input power range across which the EH can operate, plays an important role. The input power range of the EH presented is $-20\,\mathrm{dBm} - -4\,\mathrm{dBm}$ with a maximum PCE of 60% achieved at $P_{INtheor} = -20\,\mathrm{dBm}$. This important achievement allows to pull up the curve of the output power of an energy harvester depicted in Fig. 1.

The RFEH presents a peak PCE that changes with loading conditions. The lower the input power is, the lower is the voltage to switch on the transistors of the charge pump rectifier. For high input power the transistors may not be completely turned off, which increases flow-back current. In addition, the input impedance of the RFEH changes, which degrades matching with the antenna and therefore the power transferred to the load is not optimal. To partially overcome this issue, the rectifier load can be modulated to some extent by using a DC-DC converter, which will be discussed next.

D. DC-DC conversion with optimized interface with rectifier

Several RF energy harvesting systems systems reported in the literature apply DC-DC converters to up-convert the rectifier output [6], [11], [12]. When using this approach, the DC-DC converter switching frequency can be designed to be much lower and its amplitude to be higher than that of the RF signal, resulting in a combined efficiency of a single-stage rectifier and a DC-DC converter that can be higher than that of a rectifier with multiple stages in some cases.

The DC-DC converter is then used to charge a battery or a storage capacitor. Whenever possible, a storage capacitor is preferred due to its cost, small size and longer lifetime.

The DC-DC converter must present the optimum load to the rectifier in order to extract the maximum power out of it. The most straight forward way to boost the rectifier output is to use a boost converter, which most likely will be operating in Discontinuous Conduction Mode (DCM) due to the low load current, limited by the low available power. However, the average input resistance of the boost converter is dependent on the output voltage:

$$R_{in} = \frac{2L}{D^2 T}\left(1 - \frac{V_{in}}{V_{out}}\right), \tag{2}$$

in which T is the switching period, D is the duty cycle, L is the inductor value, V_{in} is the rectifier output voltage (input of the DC-DC converter) and V_{out} is the boost converter output voltage. While charging a storage capacitor, V_{out} will increase every cycle, taking the rectifier load away from its optimal value. This problem can be solved by employing a buck-boost converter, which isolates the input from the output while operating in DCM and which presents the following average input resistance [13]:

$$R_{in} = \frac{2L}{D^2 T}. \tag{3}$$

In this work we propose a non-inverting buck-boost converter to operate with an input power ranging from $1\,\mu$W to $1\,$mW, and an input voltage V_{in} ranging from 0.38 to $1.3\,$V, respectively. The core of the converter is formed by switches S_1-S_4, inductor L and storage capacitor C_{store} as depicted in Fig. 8. Ultimately, the goal of the energy harvesting front-end is to charge C_{store}, which will then be used to power the sensor node's circuits. Capacitor C_{supply} stores the energy necessary to operate the energy harvesting circuits, i.e., it provides supply voltage V_{dd} to them. The start-up circuit charges capacitor C_{supply}. It consists of a charge pump and a ring oscillator that can operate with V_{in} down to $250\,$mV. It is then turned off by the voltage monitor when C_{store} has enough voltage so that the buck-boost converter can operate and charge C_{store} by itself. When the voltage on C_{supply} reaches its maximum value ($1.8\,$V) the voltage monitor redirects the switching signal V_S to switch S_4 and keeps S_5 off, to start charging C_{store}. When V_{DD} drops below $1.2\,$V, S_5 will be switching while S_4 will be off and the converter will charge C_{supply}. Capacitor C_{rec} must be large enough so that its voltage ripple due to the inductor current is negligible. Not depicted in the block diagram are the Zero Current Detection (ZCD) circuit, which switches off S_5 or S_4 when the inductor current drops to zero, the oscillator and the ON-time generator [13].

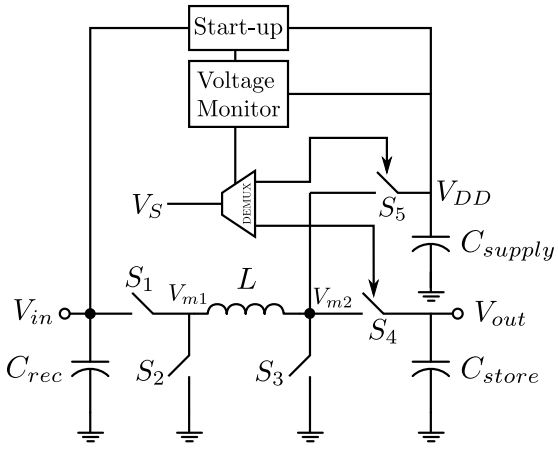


Fig. 8. Buck-boost converter core circuit

When the input/output power decreases the converter efficiency reduces and the switching loss becomes one of the dominant energy loss factors [14]. This loss can be reduced by decreasing the switching frequency and increasing the inductor value, which will increase the size of the device. Because off-the-shelf inductors with larger inductance are bulky, and in order to keep the system size as small as possible, in this work we have selected a 220-μH power inductor with a parasitic series DC resistance of $21.1\,\Omega$ (Coilcraft XPL2010-224ML). The switching loss can be further reduced by using smaller switches, but there exists a trade-off with conduction loss, since the ON resitance of the switch will increase as its width decreases. When the input/output power increases the conduction loss becomes dominant. To design a converter that is efficient both at $1\,\mu$W and $1\,$mW input power, the switches S_1-S_4 can be configured to operate in either low-power or high-power mode. Fig. 9 presents the circuit diagrams of the switches. The signal hp controls in what mode the switches will operate. In the low-power mode, only the M_{LP} transistors are switching while the M_{HP} transistors are always turned off. In the high-power mode, both M_{LP} and M_{HP} are switching. Therefore, in the low-power mode, the power necessary to drive the switches is reduced and in the high-power mode the switches series resistance is reduced. Because for low input power the voltage V_{in} is also low, in switch S_1 the low-power transistor M_{LP1} is an NMOS. In switch S_4 an extra NMOS is used ($M_{LP4,N}$) in order to increase the efficiency when the output voltage is low. However, most of the power transfer happens when V_{out} is high ($E = CV^2/2$), so we use only one NMOS and keep the added parasitic capacitance at node V_{m2} low. Switch S_5 consists of a single transistor, because the charging of C_{supply} is very short and does not have a strong influence on the efficiency.

In the ZCD circuit, the voltage at node V_{m1} is compared to the ground voltage to detect when the inductor current crosses zero. The comparator operates during a brief period after switches S_1 and S_3 are turned off. After the current crosses zero, the comparator is switched off again. This reduces the

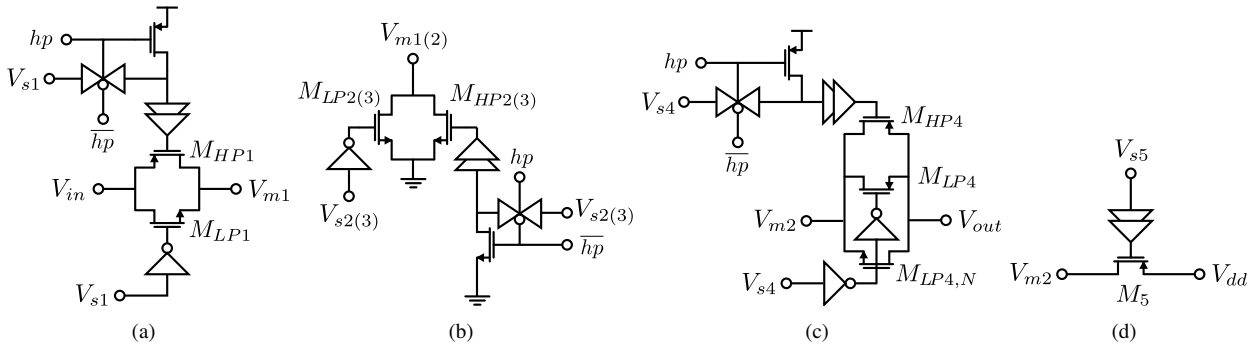


Fig. 9. Switches circuit schematics: (a) switch S_1, (b) switches S_2 and S_3, (c) switch S_4 and (d) switch S_5

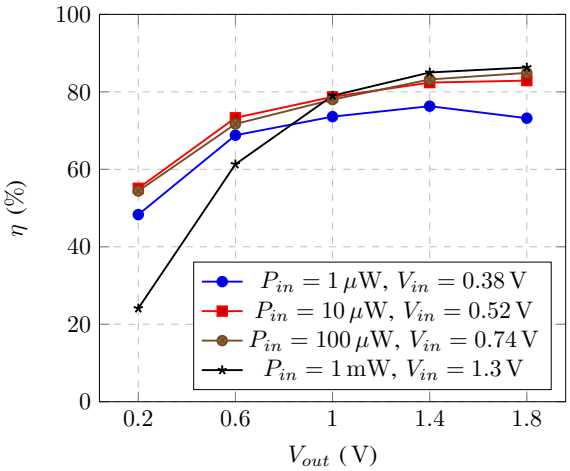


Fig. 10. Efficiency results of the buck-boost converter for various output voltages.

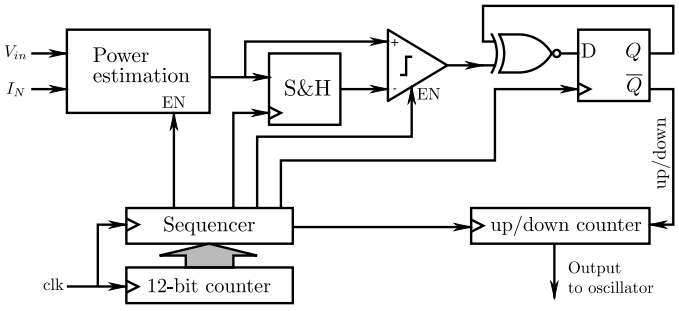


Fig. 11. MPPT block diagram.

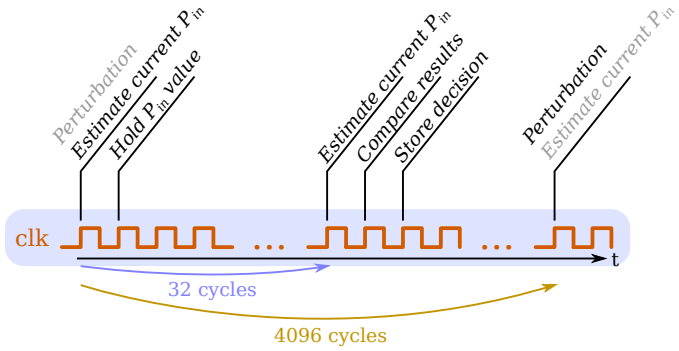


Fig. 12. Timing diagram of the MPPT circuit.

average power consumption, but it can be further decreased, while maintaining its speed, by applying dynamic biasing to the comparator [13].

The simulated efficiency (in AMS $0.18\,\mu$m CMOS technology) of the buck-boost converter for various output voltages is presented in Fig. 10. The peak efficiency of the buck-boost converter is 76.3% at an input power of $1\,\mu$W and 86.3% at 1 mW.

The switching frequency of the buck-boost converter can be selected dynamically, so its average input resistance can change (according to (3)). Here, the MPPT circuit performs this frequency selection in order to provide the best load to the rectifier.

E. Maximum Power Point Tracking

The rectifier is usually the least efficient block in the power conversion chain [11]. Therefore, by maximizing its output power we optimize the entire power conversion chain efficiency. As mentioned before, one of the steps for doing so is optimizing the rectifier load, which is the average input resistance of the DC-DC converter. The MPPT circuit designed to achieve this goal is based on the Perturb and Observe algorithm, due to its inherent low-power consumption [15]. The MPPT block diagram is presented in Fig. 11.

The sequence of events that results in maximum power tracking is presented in Fig. 12. At first, the rectifier output power is estimated and held in the sample and hold (S&H) block. A perturbation is applied, i.e., the oscillator frequency is either increased or decreased (depending on the D flip-flop output). After 32 clock cycles the output power is estimated once again and it is compared to the previous value. If the result of the comparison is positive (i.e., the power increased due to the perturbation) the value stored by the flip-flop remains unchanged, otherwise it is inverted. This value is fed to the up/down counter, which is activated to introduce the perturbation and the output of which controls the oscillator bias current. The analog circuits are turned off when not in use and after a long time (4096 clock cycles from the start) the procedure repeats itself.

The MPPT must dissipate very little power in order to have as little influence on the total power loss as possible. This can

be achieved with a low sampling rate, turning the circuits off when not in use. However, it would require a sample and hold circuit that can hold for a very long time (which dissipates power). Instead, we chose to sample the rectifier output power one extra time, within a shorter period (32 clock cycles). The number of cycles between the two power estimations was selected to provide enough settling time to the rectifier output capacitor.

The power estimation itself is based on the equation of the input power of a buck-boost converter in DCM:

$$P_{in} = \frac{V_{in}^2}{R_{in}} = V_{in}^2 \frac{D^2 T}{2L} = V_{in}^2 f_s \frac{T_{ON}^2}{2L}. \quad (4)$$

The switching frequency f_s is proportional to the oscillator bias current I_B, which leads to:

$$P_{in} \propto V_{in}^2 I_B. \quad (5)$$

Knowing that the other factors are constant, we just have to maxime $V_{in}^2 I_B$ to maximize the input power. The same result is obtained if we maximize the square root of this value, which can be easily obtained using a differential pair in strong inversion.

The circuit employed to do the power estimation is presented in Fig. 13(a). The difference between the drain currents in the differential pair is given by:

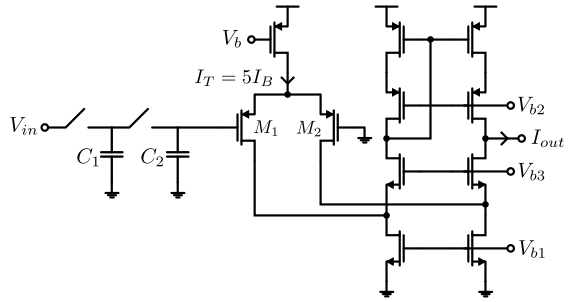
$$I_{D1} - I_{D2} = \sqrt{2K}\sqrt{I_T} V_d, \quad (6)$$

in which $K = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}$, V_d is the differential input, which is a fraction of the input voltage, and I_T is the tail current, which is proportional to I_B. Therefore, the output current of this circuit is proportional to the square root of (5) and maximizing it will maximize the rectifier output power.

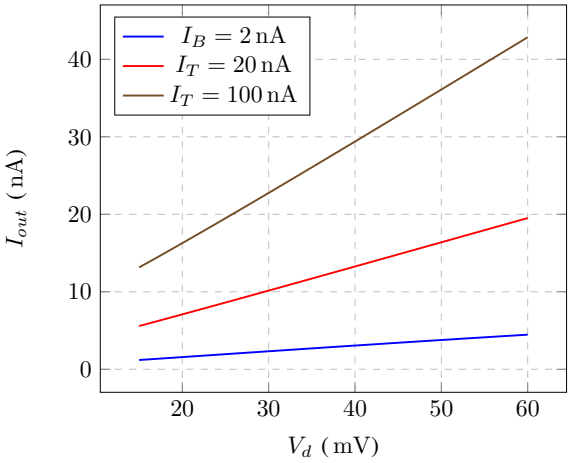
This circuit topology was chosen because of the limited voltage headroom that the differential pair must operate in, recalling that the minimum V_{DD} for which this circuit must operate is 1.2 V (because it shares the same supply as the buck-boost converter presented in the previous subsection) and that the differential pair must be in strong inversion. In the simulation results, we can observe the linear variation with V_d, Fig. 13(b), and the square root variation with I_B, Fig. 13(c), in which the dashed lines are the best fitting square roots.

The current output of the power estimator is fed into a diode connected NMOS, which converts the current into a voltage. The sample and hold circuit consists of a simple switch and capacitor to hold the voltage value. The comparator employed is a StrongARM comparator [16]. The other blocks of the MPPT are all digital: the 12-bit counter provides the input to the sequencer, which enables/disables and generates the clock signal for all the other blocks; the up/down counter sets the oscillator frequency.

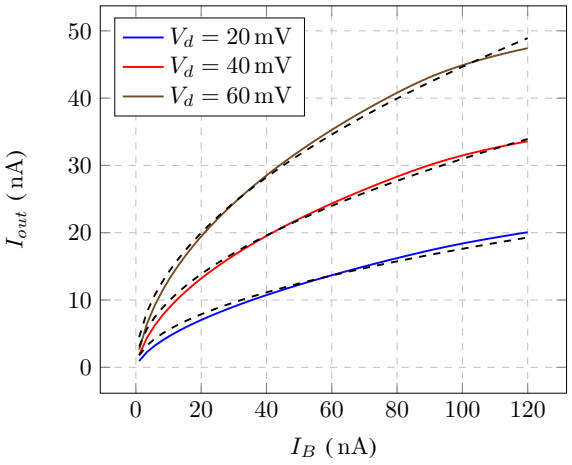
Circuit simulations using AMS 0.18 μm CMOS technology show that the MPPT circuit dissipates 17.4 nW from a 1.8-V supply. This simulation was performed for an operating frequency of 20 kHz (oscillator biased with 2 nA), which is the configuration to achieve 1 μW of input power. If the frequency and hence the oscillator biasing current increase, the power consumption increases as well. At 1 MHz, which is



(a)



(b)



(c)

Fig. 13. Rectifier output power estimator: (a) schematic; (b) output current versus differential input voltage; (c) output current versus I_B (dashed lines represent the best fitting square root curves).

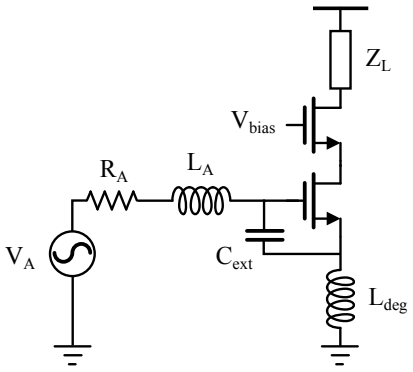


Fig. 14. Interface model of an inductively degenerated CMOS LNA directly connected to an inductive antenna impedance.

the maximum frequency of the system and the one in which it consumes the highest power, the power consumption of the MPPT is $278.5\,\mathrm{nW}$.

The combination of the DC-DC converter, presented previously, with the MPPT allows to boost the rectifier voltage and charge a storage capacitor while presenting the best load to the rectifier, optimizing its efficiency. Moreover, the MPPT circuit power consumption is low, allowing for efficient harvesting down to $1\,\mu\mathrm{W}$ available input power.

Another crucial block that impacts the overall performance of a WSN is the receiver. This challenge is addressed in the next section.

III. Receiver: Co-design of Low-Noise Amplifier and Antenna

As addressed in [8], the co-design principle presented in Section II-A also holds for the interface between an LNA and an antenna. A design example is treated here to demonstrate the NF improvement introduced by the proposed co-design principle.

The co-design of any antenna-electronics interface starts by optimizing the load impedance, which in this example is a narrowband LNA. The well-known inductively degenerated CMOS cascode LNA topology [17] is used as it provides an easy way of adjusting the LNA input impedance. The LNA is directly connected to an inductive antenna as depicted in Fig. 14. The information is sensed with a CMOS gate, meaning that voltage is the preferred signal quantity to maximize.

For this particular LNA implementation, the interface impedance is defined as $Z_{int} = R_A + j\omega(L_A + L_{deg}) = R_A + jX_A$ as the total inductance in the interface is the sum of the antenna and the degeneration inductors. If the interface is conjugate matched, the antenna load voltage can be approximated by (1) for large values of Q. The minimum noise factor for low and medium frequencies can be approximated as:

$$F_{min} \approx 1 + \delta\frac{R_g}{R_A} + \underbrace{\frac{R_A}{X_A^2}}_{co-design}\underbrace{\left(\frac{\gamma}{g_m} + \frac{4}{g_m^2 R_L}\right)}_{LNA} \qquad (7)$$

Here, g_m denotes the transconductance of the MOS transistor, R_g is the transistor gate resistance and R_L is the equivalent thermal noise resistance of the LNA's load and subsequent stages. The coefficient γ is often between 2/3 and 2, depending on the transistor size and the technology. Notice that the 'LNA' term in (7) only depends on the LNA circuit parameters and can be minimized by increasing the MOS transistor's bias current and gate area. The 'co-design' term allows to reduce the noise factor without additional power consumption by using a high-Q impedance interface [8].

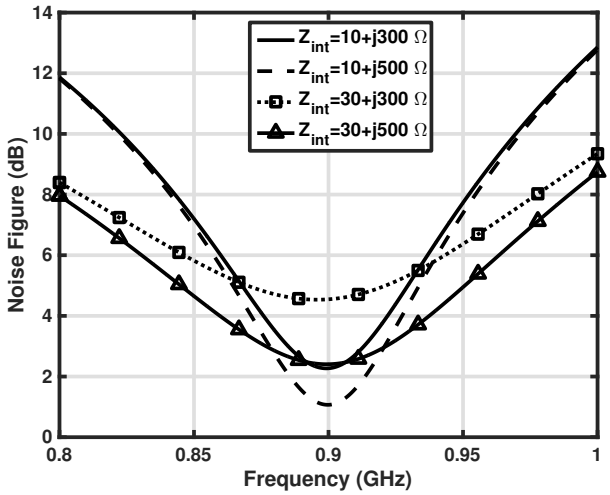


Fig. 15. Simulated narrowband LNA noise figure for various interface impedances.

As a proof of concept, a narrow band LNA with a center frequency of $900MHz$ is designed in AMS 0.18 um technology and its design parameters are kept constant during the circuit simulations ($g_m = 366\,\mu\mathrm{S}$, $C_{gs} = 4\,\mathrm{fF}$, $R_g = 18\,\Omega$, $R_L = 10\,\mathrm{k}\Omega$, $\gamma = 1.1$). The LNA input impedance is varied by tuning L_{deg} and C_{ext} while the antenna impedance is subsequently conjugate matched to the LNA input for each case. The difference in noise factor is thus only determined by the difference in interface impedance, when considering ideal antenna impedance and matching components .

The impact of the 'co-design' term can be confirmed by the simulated noise figure (NF, in dB) for various interface impedances, as shown in Fig. 15. Note that, in order to clearly demonstrate the impact of the interface impedance Z_{int}, some of Z_{int} in Fig. 15 have a big reactance and hence require an impractical value of L_{deg} (e.g., 50 nH). From Eq. 7, it is worth to notice that for a given minimum noise factor, the co-design principle allows to reduce the g_m of the MOS transistor, and therefore the power consumption of the LNA is also reduced. Since this principle can be exploited both at the transmitter and at the receiver side, the power gap depicted in Fig. 1 can be reduced. A limitation of this principle is imposed by the fact that a conjugate matched interface in theory would increase the voltage even further, but in this case would require a purely inductive antenna with infinitely small antenna radiation resistance and conduction loss resistance, which of course is not realizable.

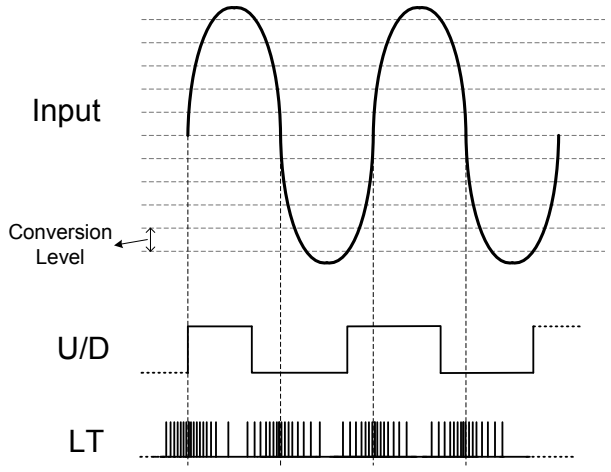


Fig. 16. Input and output signals of the level-crossing ADC.

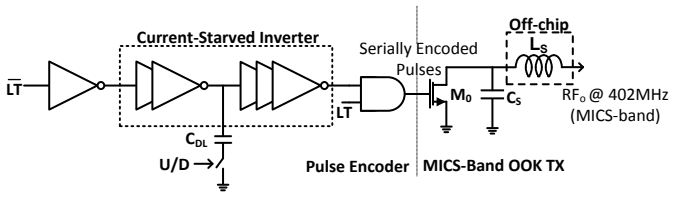


Fig. 17. Circuit diagram of the asynchronous transmitter.

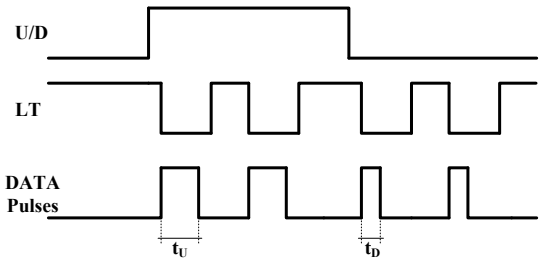


Fig. 18. Waveforms of the asynchronous encoder.

IV. Asynchronous Data conversion and Low-Power Data transmission

Once powered by the RFEH, the system can read data from the sensors and transmit it. In this section, we first briefly discuss a data conversion front-end. Subsection IV-B and Subsection IV-C present passive and active data transmission, respectively.

A. Asynchronous Data Conversion

IoT sensors may be used to sense slowly-varying signals. In this case, a level-crossing analog-to-digital converter (LC-ADC) can be applied in order to reduce power consumption [18]. Unlike uniform sampling, the level-transition (LT) and UP/DOWN (U/D) pulse sequences are generated only when the input signal crosses a predefined threshold level as illustrated in Fig. 16. More details on the asynchronous front-end design are provided in [18].

The two binary outputs (LT and U/D) must then be both fed to the data transmitter. They have to be combined and transmitted simultaneously, otherwise information would be lost. As the transmitter is powered by an RFEH, to minimize power consumption, the data transmission should be only enabled when ADC data conversion is active. The following subsections present two alternative circuits to transmit the data provided by the asynchronous ADC, one passive and one active circuit.

B. Passive Data Transmission

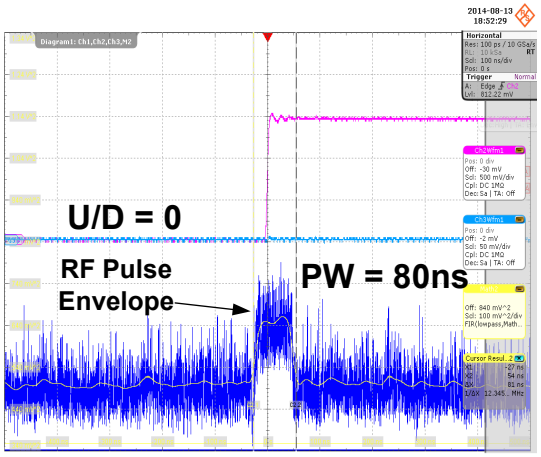
Employing pulse duration modulation (PDM), the 2-bit data stream is combined to generate pulses with different time duration for upward conversion and downward conversion. This means that the transmitter produces a pulse when LT indicates a conversion and U/D defines the duration of this pulse. In this way the 2-bit information can be embedded in a single pulse. Fig. 17 presents the circuit diagram of the transmitter that includes a digital pulse encoder and a backscattering network. The pulses are generated by comparing LT to $\overline{\mathrm{LT}}$, the latter being the complement of LT delayed by six cascaded current starved inverters. The delay time is set by U/D that makes the pulses longer when it is set to 1.

The delay is defined by the current drawn in the inverters and capacitor $\mathrm{C_{DL}}$. For U/D equal to 1 (upward level crossing) $\mathrm{C_{DL}}$ is connected to ground, thus the pulse width is longer. For U/D equal to 0 (downward level crossing) $\mathrm{C_{DL}}$ is disconnected from ground, thus the duration of the pulses is shorter. Fig. 18 shows the waveforms of the low-power pulse encoder: the pulse duration is $\mathrm{t_U}$ for upward conversion and $\mathrm{t_D}$ for downward conversion.

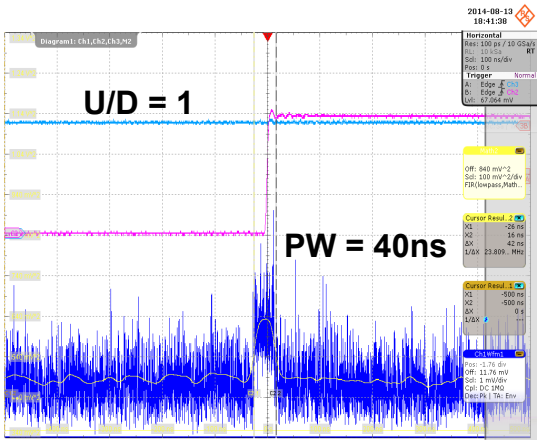
As an example, we present a circuit designed for backscattering data transmission in which the pulsed signal modulates a $402\,\mathrm{MHz}$ RF signal received in the LC network, implementing ON-OFF-Keying modulation through transistor $\mathrm{M_0}$ (see Fig. 17) [19]. The values of $\mathrm{L_S}$ and $\mathrm{C_S}$ are 32 nH and 4.9 pF, respectively. Fig. 19 illustrates the measured waveforms of the asynchronous pulse encoder. In Fig. 19(a) the output of the pulse encoder is presented for an LT transition with U/D = 0. In this condition the pulse width is $80\,\mathrm{ns}$. For a LT transition with U/D = 1, the pulse width equals $40\,\mathrm{ns}$, as shown in Fig. 19(b).

C. Low-Power Sub-GHz UWB Transmitter

Alternatively, active data transmission may be employed to increase the range over which the sensor node can operate, but with the drawback of consuming more power. In this subsection we present a novel low-power sub-GHz UWB transmitter (LPUT) topology based on the circuit principle depicted in Fig. 20. Unlike previously published works, the LPUT core contains a series LC network, comprising R_S, L and C, which is driven by an impulse voltage source Vip^+. R_S is the series equivalent resistance of the LC network plus the output resistance of the voltage source. Voltage VP^+ and current I_P are coupled into the antenna through capacitance C_L. The antenna impedance, Z_A, is modeled as a resistance, R_A, in parallel with the antenna equivalent capacitance C_A and inductance L_A, as shown in Fig. 20. C_A and L_A are



(a)



(b)

Fig. 19. Measured encoder output waveforms: (a) 80 ns or U/D = 0 and (b) 40 ns for U/D = 1.

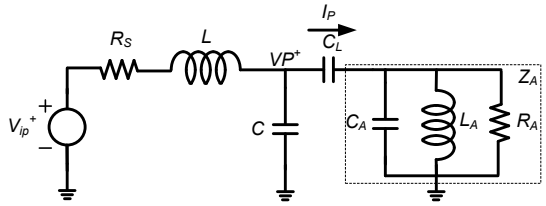


Fig. 20. Circuit diagram of single-ended input low-power sub-GHz UWB transmitter.

included in the antenna model since the antenna has a limited bandwidth, similar to a band-pass filter [20].

Although the circuit from Fig. 20 already generates an UWB pulse, the PSD of VP^+ still contains strong frequency components above 950 MHz that couple into the antenna, violating the FCC regulation mask. To generate a pulse that complies with the FCC spectral mask, previous works perform power spectral density shaping by means of a filter [20], [21]. In addition, some designs rely on standard digital cell delays [22], [23]. These methods introduce losses in the transfer function of the pulse shaping network in the transmitter or require high order filters to realize a steep roll-off near 950 MHz.

Fig. 21 presents an input differential version of the circuit

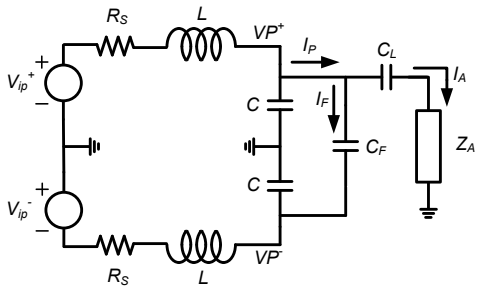


Fig. 21. Circuit diagram of differential input low-power sub-GHz UWB transmitter.

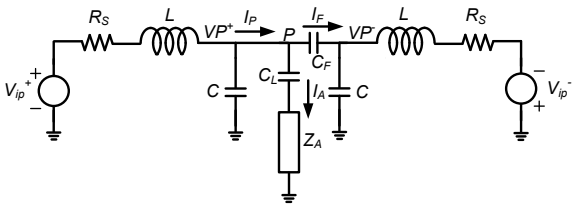


Fig. 22. Circuit diagram of differential input LPUT as a quasi-symmetrical circuit.

shown in Fig. 20. The circuit has been duplicated and is driven by two impulse voltage sources, Vip^+ and Vip^-. The voltages VP^+ and VP^- have opposite signs as the network is driven pseudo-differentially. The voltage and current signals at the antenna are single-ended since the currents I_P and I_F are subtracted in a single node. Hence, the current at the antenna, I_A, is the difference between I_P and I_F. I_P is generated by VP^+ and I_F is generated by the voltage difference $VP^+ - VP^- = VP_{DIF}$.

The impedance $Z_F = 1/(sC_F)$, ideally, is a short only for high frequency components. A simple qualitative analysis can be made to understand the filtering effect of Z_F; (1) at low frequencies, Z_F is very high, therefore $I_F = VP_{DIF}/Z_F$ is very small. Hence, I_A is not affected by I_F. (2) at high frequencies, Z_F is very low. Consequently, at high frequencies, the difference between I_P and I_F, I_A, becomes very small. This analysis leads us to understand that the upper limit of the PSD depends on C_F, the value of which can be selected to generate a pulse with a PSD that falls within the FCC mask.

Fig. 22 shows the LPUT drawn as a quasi-symmetrical circuit, with quasi-symmetry seen from node P. Analyzing Fig. 22, we can derive the currents I_P, I_F and I_A and the voltage at the output antenna (V_A). Each network has an equivalent impedance, seen from node P to ground. The impedances can be described in the complex frequency domain as follows,

$$Z_{pgA} = \frac{(R_S + sL)}{(s^2LC + sR_SC + 1)}, \tag{8}$$

$$Z_{pgB} = Z_{pgA} + Z_F, \tag{9}$$

$$Z_{pgC} = Z_A + \frac{1}{(sC_L)}, \tag{10}$$

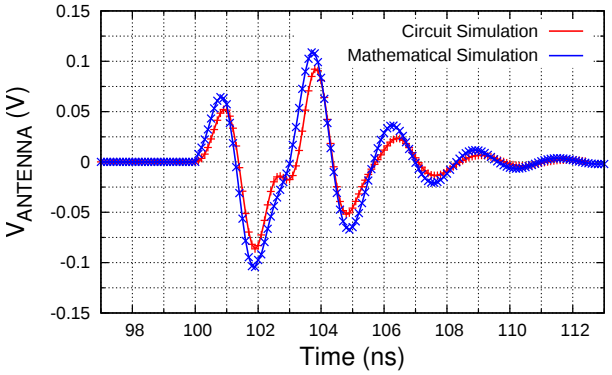


Fig. 23. Time domain result of circuit simulation and mathematical simulation.

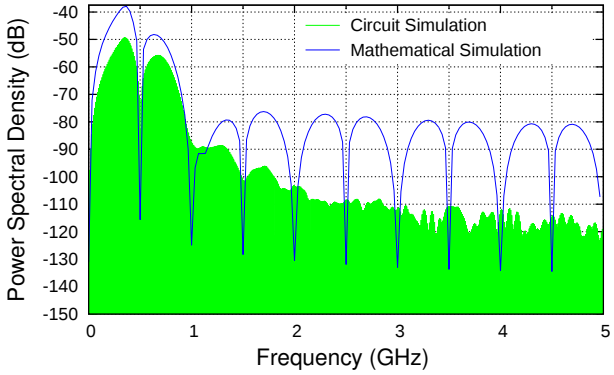


Fig. 24. PSD of circuit simulation and mathematical simulation.

and finally,

$$V_A = \left(\frac{V_{ip}}{(s^2LC + sR_SC + 1)}\right) \cdot \left(\frac{Z_F\ Z_A}{Z_{pgC}Z_F + 2Z_{pgA}Z_{pgC} + Z_{pgA}Z_F + Z_{pgA}^2}\right), \quad (11)$$

which is the voltage across the antenna as a function of the equivalent impedances and the input voltage. From (11), we can conclude that the antenna voltage is roughly zero if Z_F is very low. This analysis makes perfect sense as the network is fully symmetric and the voltage at node P becomes zero when the network is driven by a differential input voltage. Since Z_F is a capacitive reactance, the voltage at node P thus equals zero at high frequencies. In this design, C_F is chosen to set the voltage at node P to zero for frequencies above 1 GHz.

The simulation results that validate the analysis of the previous subsection are presented below. In addition, an experimental implementation is described and measurement results are shown.

1) Simulation Results: Fig. 23 shows the time domain results of the circuit and mathematical simulation. Fig. 24 presents the power spectral density of the simulated signals. The PSD of the signals from both simulations are very much alike and comply with the FCC mask. The difference between the two curves is that the mathematical simulation does not consider all losses that are present in the devices and in the PCB. The circuit simulation already includes losses in the passive devices. In addition, the circuit simulation includes the models of the micro-wave transistors that are used to implement the differential driver. These transistors add more asymmetry since the gate-source voltages of the transistors are different when they drive the differential signal.

2) Experimental Results: The low-power sub-GHz UWB transmitter has been realized using high-speed discrete transistors, discrete (SMD) capacitors and on-PCB inductors in line with the circuit diagram shown in Fig. 25. The drivers are implemented using high-speed discrete transistors with low threshold voltages in a stacked topology that is suitable for low voltage operation ($100\,\mathrm{mV} \leq VDD_{RF} \leq 150\,\mathrm{mV}$) and offers high bandwidth. The transistor that has been chosen for this design is the ATF551M4. The threshold voltage (V_{TH}) of this

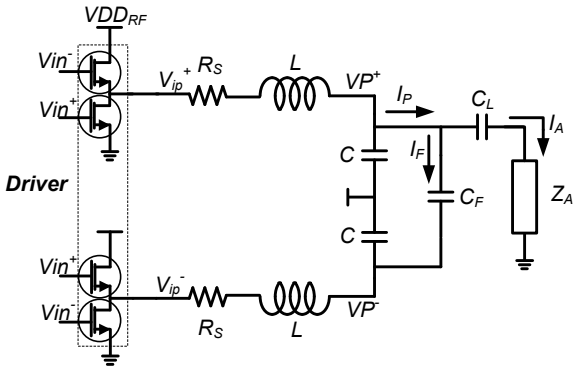


Fig. 25. Circuit diagram of designed LPUT.

device is roughly $0.35\,\mathrm{V}$. The input and output inductances and capacitances of this device are small enough to minimize dynamic power consumption and to keep the amount of high frequency spurs in the transmitted pulse small.

For testing purposes only, a differential input stimulus generator has been implemented. The input stimulus generator comprises a pulse generator, a high pass voltage divider, a balun and a level shifter, as depicted in Fig. 26. The level shifter is supplied by $Vddpulse$ that is $0.65\,\mathrm{V}$ (V_{TH} + VDD_{RF}) and thus large enough to drive both stacked transistors. The photograph of the test bench is shown in Fig. 27. Fig. 28 shows a photograph of the PCB of the transmitter that includes the level shifter.

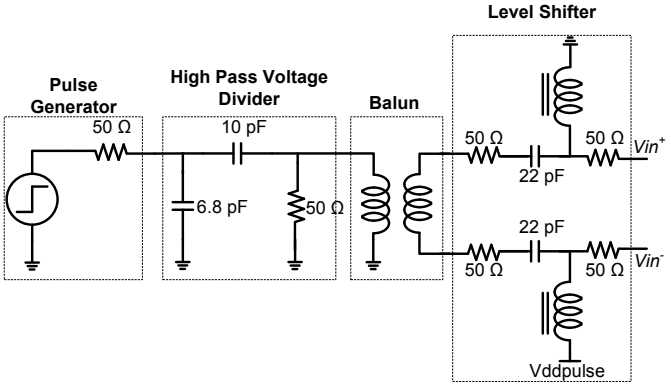


Fig. 26. Circuit diagram of the stimulus generator.

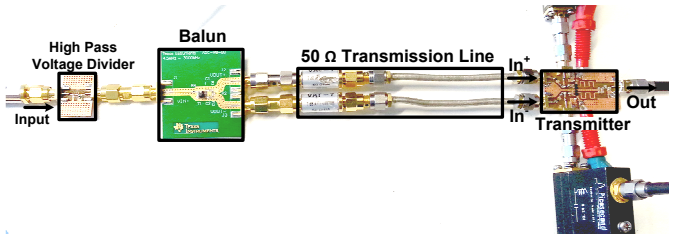


Fig. 27. Test bench photograph of the low energy sub-GHz UWB transmitter.

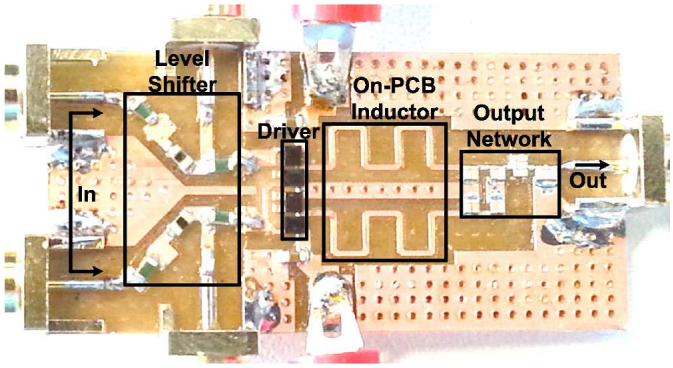


Fig. 28. PCB photograph of the designed transmitter.

The equivalent series resistance and inductance of the on-PCB inductor, extracted by means of electromagnetic simulation, are presented in Fig. 29.

Fig. 30 and Fig. 31 show the measured output voltage waveform of the LPUT and the corresponding power spectral density for $VDD_{RF} = 0.15\,\mathrm{V}$, respectively. In Fig. 31, some high frequency components ($> 1\,\mathrm{GHz}$) can be observed while in Fig. 24 high frequency components are attenuated.

The main difference between the measured and the mathematical results is the symmetry of the circuit. The circuit developed on PCB is not ideally symmetrical, therefore the roll-off is less steep than that of the mathematical model. The PSD of the transmitted signal presents a 25 dB decay between 500 MHz and 1 GHz. This steep decay is a consequence of the differential to single ended conversion of the circuit. It comes from the fact that the neutral point of the differential circuit behaves as a ground for very high frequencies. The

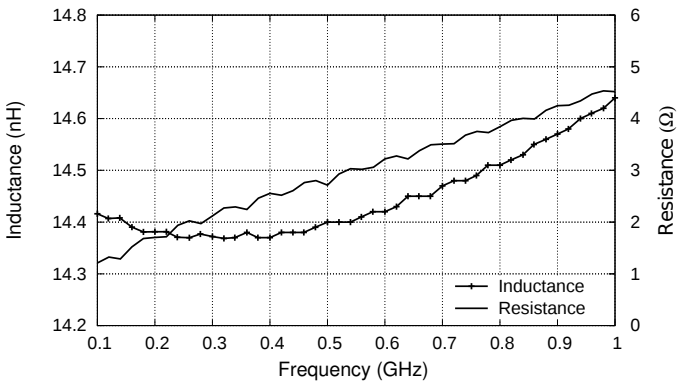


Fig. 29. Equivalent series resistance and inductance of the on-PCB inductor.

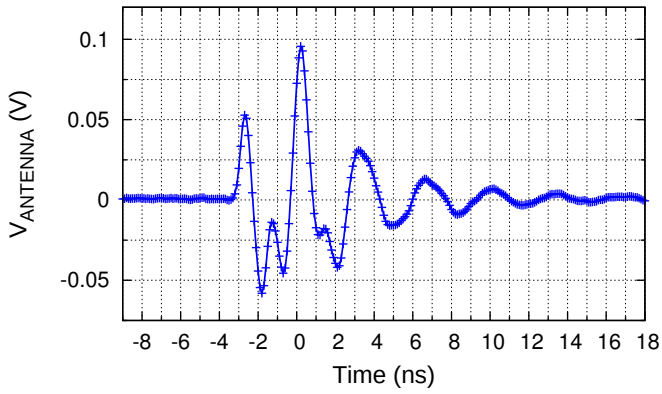


Fig. 30. Measured output voltage waveform of the LPUT.

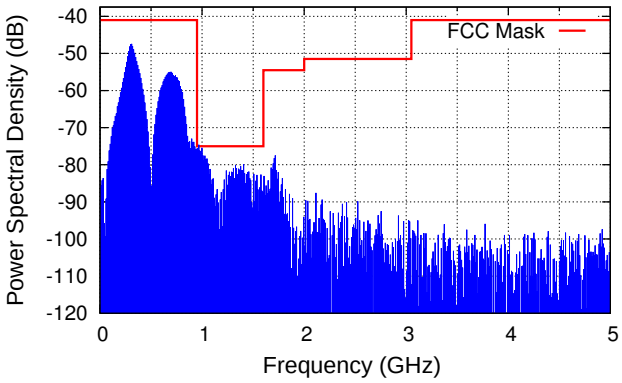


Fig. 31. Measured output power spectral density of the LPUT.

steep decay in the PSD is an important characteristic of the circuit that allows to keep the transmitted signal within the FCC mask [24].

To measure the power consumption of the LPUT, the RMS current consumption of the driver is measured as well as the level shifter power consumption.

Fig. 32 presents the estimated PSD of the transmitted impulse (of Fig. 31) after taking into account path loss, ground reflection and antenna/receiver matching. The path loss and ground reflection are modeled according to [25], [26] and simulated using the measured transmitted impulse as input. The transmitter-receiver separation distances (d) considered in the analysis are $0.1\,\mathrm{m}$, $1\,\mathrm{m}$, and $10\,\mathrm{m}$ with the transmitter and receiver in the same height (h) of $0.1\,\mathrm{m}$ and $10\,\mathrm{m}$; the ground reflection coefficient is -1. Fig. 32 also shows that the PSD peak power decreases with d and increases with h. This behavior can be explained by the fact that at lower height ($h = 0.1\,\mathrm{m}$) the ground reflected signals are stronger at the receiving antenna with $180°$ phase. On the other hand, if the antenna is higher ($10\,\mathrm{m}$) the reflected signal is attenuated and its effects are minimized.

The performance summary of the LPUT is presented in Table IV. The power consumption of the UWB transmitter is only $0.28\,\mathrm{mW}$. This value is much lower than the typical power consumption of the state of the art transmitters discussed in Table I. The transmitter is the most power hungry block in a WSN, therefore with the proposed UWB transmitter the overall power consumption of the WSN is drastically reduced.

TABLE IV
PERFORMANCE SUMMARY OF THE LPUT

Specifications	Value	Specifications	Value
Frequency Band (GHz)	0.25-0.75	$V_{peak-peak}$ (V)	0.14
Power (mW)	0.280	$V_{peak-peak}$/Supply Voltage (%)	93.3
Energy/Pulse (pJ/pulse)	85	PRF (MHz)	3.3
Supply Voltage (V)	0.15/0.65†	Roll-off (dB/octave)	25

† Voltage supply of the level shifter, for testing purposes.

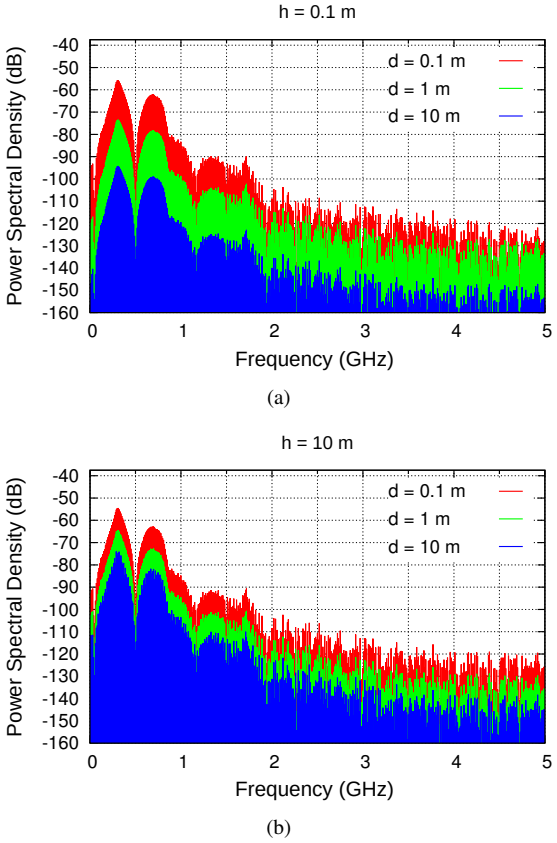


Fig. 32. Estimated PSD of the LPUT including path loss and ground reflection for (a) $h = 0.1\,\mathrm{m}$ and (b) $h = 10\,\mathrm{m}$.

This allows to bring the two curves of Fig. 1 closer each others.

In order to transmit the output data of the asynchronous ADC presented previously, the input of the transmitter can be modulated similarly as in the passive transmitter. In this way, two pulses are transmitted for each output of the LC-ADC and the time between the pulses makes a distinction between an up or down level crossing. Therefore, the UWB transmitter is a simple alternative to the passive transmitter, enabling low-power operation of the sensor node and increasing its maximum distance of operation from a reader device.

V. SUMMARY AND CONCLUSIONS

The circuit techniques presented in this paper allow to have both energy and bidirectional data transfer to a sensor node in a low-power and energy-efficient manner. Regarding the RF to DC conversion, we showed that co-design of the antenna and the RFEH leads to better performance for the overall system. Then, a voltage boosting network combined with a 5 stage on-chip rectifier and its measurement results were presented. A DC-DC converter was presented as an alternative to a multistage on-chip rectifier. The implemented buck-boost DC-DC converter employs an MPPT technique that estimates the input power, and adjusts the equivalent input resistance of the DC-DC converter in order to always show the optimal impedance at the rectifier output, allowing for efficient harvesting across a larger range of available input power. Regarding the receiver side, it was shown that co-design of the antenna and the LNA leads to better performance in terms of NF, power efficiency and sensitivity. An asynchronous front-end that uses an LC-ADC was used to perform data conversion to facilitate data transmission. Moreover, a novel low-power Sub-GHz UWB transmitter was presented. The analytical expression of the voltage across the antenna as a function of the input voltage was derived and compared to the results of circuit simulations. The low-power transmitter has been implemented by using discrete components and the results from the measurement proved the correct operation of the circuit. Throughout the paper a quantified comparison with some relevant works, both in terms of low power UWB transmitter and power-efficient EH, has been carried out, proving that the power gap present in the state of the art WSNs has been drastically reduced.

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Gustavo C. Martins (S'11) was born in Jacupiranga, Brazil, in 1988. He received the B.Eng. degree from Universidade de São Paulo, São Carlos, Brazil, in 2010 and the M.Sc. degree from Universidade Federal de Santa Catarina, Florianópolis, Brazil, in 2013. He is currently a Ph.D. candidate at the Section Bioelectronics of Delft University of Technology, Delft, The Netherlands. His research interests include wireless power transfer and low-power analog IC design.

Alessandro Urso (S'16) was born in Lecce, Italy, in 1991. He received the Bachelors degree and the M.Sc. degree (cum Laude) in Electronic and Telecommunications engineering from the University of Ferrara, Italy in 2013 and 2015, respectively. He is currently a Ph.D. candidate at the Section Bioelectronics of Delft University of Technology, Delft, The Netherlands. His research interests include low-power analog and mixed-signal integrated circuits design and energy harvesting for autonomous wireless sensor nodes.

André L. Mansano (S'11) was born in Jaboticabal, Brazil, in 1982. He received the B.Eng. degree from Universidade Estadual Paulista, São Paulo, Brazil, and the M.Sc. degree from Universidade Estadual de Campinas, São Paulo, Brazil, in 2006 and 2009, respectively. In 2016 he received his PhD degree from Delft University of Technology. In 2007, he joined Freescale Semiconductor as a Analog Mixed-Signal Designer. He designed analog IPs for automotive and general purpose 8 and 32-bit microcontrollers. In addition to the designed IPs for commercial products, he has authored two patents and four papers. In November 2010, he joined Delft University of Technology, Delft, The Netherlands, as a Guest Researcher. Currently he works at Philips Research in Eindhoven as analog mixed signal IC designer. His research interests include wireless energy harvesting, wirelessly powered sensors, very-low-power and low-noise amplifiers and low-power wireless communication.

Yao Liu was born in Hubei, China, in 1987. He received the M.Sc. and B.Sc. degrees in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2011, respectively. He is currently working towards the Ph.D. degree in the Section Bioelectronics of the Department of Microelectronics at the Faculty of Electrical Engineering, Mathematics, and Computer Science, Delft University of Technology. His research interests include low power wireless communication circuits design for biomedical applications.

Wouter A. Serdijn (M'98, SM'08, F'11) was born in Zoetermeer ('Sweet Lake City'), the Netherlands, in 1966. He received the M.Sc. (cum laude) and Ph.D. degrees from Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively. Currently, he is a full professor in bioelectronics at Delft University of Technology, where he heads the Section Bioelectronics, and a visiting honorary professor at University College London, in the Analog and Biomedical Electronics group.

His research interests include integrated biomedical circuits and systems for biosignal conditioning and detection, neuroprosthetics, transcutaneous wireless communication, power management and energy harvesting as applied in, e.g., hearing instruments, cardiac pacemakers, cochlear implants, neurostimulators, portable, wearable, implantable and injectable medical devices and electroceuticals.

He is co-editor and co-author of 10 books, 8 book chapters, 2 patents and more than 300 scientific publications and presentations. He teaches Circuit Theory, Analog Integrated Circuit Design, Analog CMOS Filter Design, Active Implantable Biomedical Microsystems and Bioelectronics. He received the Electrical Engineering Best Teacher Award in 2001, in 2004 and in 2015.

He has served, a.o., as General Co-Chair for IEEE ISCAS 2015 and for IEEE BioCAS 2013, Technical Program Chair for IEEE BioCAS 2010 and for IEEE ISCAS 2010, 2012 and 2014, as a member of the Board of Governors (BoG) of the IEEE Circuits and Systems Society (2006-2011), as chair of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems society, and as Editor-in-Chief for IEEE Transactions on Circuits and Systems-I: Regular Papers (2010-2011). Currently, he is a member of the Steering Committee and an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems (T-BioCAS)

Wouter A. Serdijn is an IEEE Fellow, an IEEE Distinguished Lecturer and a mentor of the IEEE. In 2016, he received the IEEE Circuits and Systems Society Meritorious Service Award.