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A 1-V Class-AB Translinear Integrator for Filter Applications

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Abstract. In this paper, the design and measurements of a 1-volt class-AB instantaneous companding translinear integrator are presented. The use of instantaneous companding and class-AB operation gives an improvement of the dynamic range and a reduction of the power consumption. The proposed circuit uses only bipolar transistors and one capacitor and is, therefore, very well suited for integrated implementation. Its unity-gain frequency can easily be controlled by a current. Simulations and measurements of a semicustom realization, to be applied in a hearing instrument, confirm correct operation of the designed circuit. The translinear integrator operates from a single supply voltage down to 0.95 V. The current consumption is less than 1.9 μA for an input current of 180 nA (p). The dynamic range is better than 73 dB over a bandwidth of 8 kHz.

Key Words: continuous-time filters, companding, translinear circuits, log-domain circuits, hearing instruments

1. Introduction

Today, portable electronic equipment becomes more and more important. Therefore, analog circuits that operate at low supply voltages and consume minimal power, the low-voltage low-power circuits, have gained much interest. An important operation in electronics is the separation of desired signals from undesired signals in the frequency domain: the filtering of signals. Integrators can be considered to be basic building blocks for the realization of filter structures. An integrator that is often used is the well-known transconductance-C (gm-C) integrator. A disadvantage of this integrator for use in low-voltage low-power filters with a controllable transfer function is that resistor values become too large for implementation in integrated circuits [1]. This can be circumvented by using the principle of an instantaneous companding current-mode integrator introduced by Seevinck in [2] and later thoroughly investigated by Frey [3–12], Punzenberger and Enz [13–27], Toumazou et al. [28–47], Roberts et al. [48–53], Tsividis [54–58], Mulder and Serdijn [59–80] and others [81,82]. The integrator introduced by Seevinck uses both the current-mode approach [83] and an instantaneous companding technique [84] to improve the dynamic range in a low-voltage environment. The instantaneous companding is realized by using non-linear transfer functions in the signal path. The circuit proposed here is a 1-volt class-AB companding current-mode integrator. The advantages of class-AB implementation, over class-A implementation, are the further improvement of the dynamic range and reduction of the power consumption.

In the next section, we discuss the principle behind the companding current-mode integrators (CCI's). The designed integrator is discussed in Section 3. Section 4 deals with the simulation results and measurements of a semicustom realization of the integrator, which has been optimized for use in a hearing instrument.

2. Principle of Instantaneous Companding Current-Mode Integrators

As a starting point, we consider the block diagram of an instantaneous companding integrator, as introduced by Seevinck [2]. See Fig. 1(a). The circuit comprises four fundamental system blocks: a divider, a linear time integrator, a block with an expanding

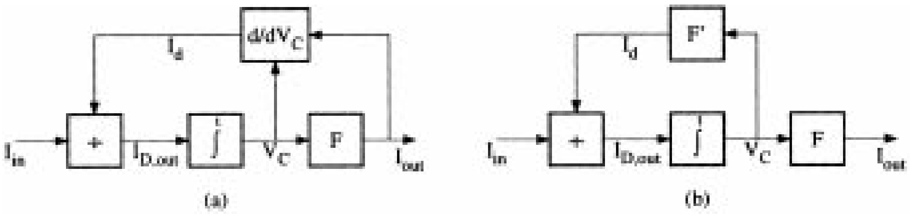

Fig. 1. Principle model (a) and practical realization model (b) of an instantaneous companding integrator.

transfer function F that converts the internal voltage V_C into the output current I_{out}, and a block d/dV_C that differentiates the output current I_{out} with respect to the internal voltage V_C. An expanding transfer function F reduces the voltage swing of the internal voltage V_C, which is beneficial in a low-voltage environment.

Since, in practice, the divider current I_d is unipolar, the divider consists of a two-quadrant divider that divides the bipolar input current I_{in} by I_d and produces $I_{D,\text{out}}$:

$$I_{D,\text{out}} = \frac{I_n I_{\text{in}}}{I_d} \tag{1}$$

with I_n a normalizing current.

The divider current I_d is the output signal of the differentiator, and therefore:

$$I_d = V_n \frac{dI_{\text{out}}}{dV_C} \tag{2}$$

with V_n a normalizing voltage.

Substituting (2) into (1) yields:

$$I_{D,\text{out}} = \frac{I_n I_{\text{in}}}{V_n \frac{dI_{\text{out}}}{dV_C}} \tag{3}$$

The integration is performed by a capacitor and produces the internal voltage V_C. The integration current for the capacitor is the output current $I_{D,\text{out}}$ of the divider and therefore $I_{D,\text{out}}$ must also be equal to:

$$I_{D,\text{out}} = C \frac{dV_C}{dt} \tag{4}$$

with C the integration capacitance.

Combining (3) and (4) and applying the chain rule yields:

$$\frac{dI_{\text{out}}}{dt} = \frac{I_n}{V_n C} I_{\text{in}} \tag{5}$$

Integrating (5) gives the linear result:

$$I_{\text{out}} = \frac{I_n}{V_n C} \int I_{\text{in}} dt \tag{6}$$

Note that the overall input-output relation given by (6) is completely independent of the expanding transfer function F. Deviations of F from the intended transfer function F have thereby no influences on the overall input-output relation. However, in the practical realization, the differentiator (d/dV_C) will not be implemented. Instead, a circuit will be implemented that has a transfer function F', which must be identical to the derivative dF/dV_C. Differences between the implemented transfer function F' and the derivative dF/dV_C will cause the overall input-output relation to be an approximation of (6). The model that represents the practical realization of a companding current-mode integrator is depicted in Fig. 1(b).

3. The 1-Volt Class-AB Companding Current-Mode Integrator

The basic structure of the proposed integrator is given by the model depicted in Fig. 2.

The current splitter, the two one-quadrant dividers and the subtractor form the two-quadrant divider as depicted in Fig. 1. The current splitter splits the input current I_{in} into two positive currents I_1 and I_2. These currents can be now divided individually by the divider current I_d by using one-quadrant dividers. The subtraction of the output currents $I_{D,\text{out}1}$ and $I_{D,\text{out}2}$ of

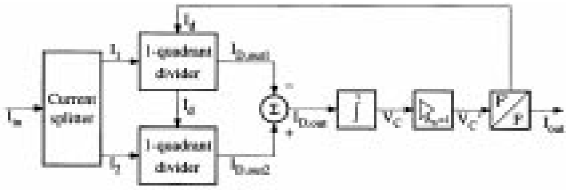

Fig. 2. Structure of the class-AB CCI.

the one-quadrant dividers gives the output current $I_{D,\text{out}}$ of the composed two-quadrant divider. The integration of the current $I_{D,\text{out}}$ is realized by a single capacitor and produces the internal (capacitor) voltage V_C. The advantage of using a single capacitor for integration is that no matching of capacitors is needed, as is the case in the class-AB circuit given by Seevinck in [2]. The voltage buffer minimizes interaction between the F/F' circuit and the capacitor. The expanding transfer function F is a hyperbolic-sine function, because of the very well suited class-AB implementation of this function, and the ease of implementation of the (derivative) transfer function F' (hyperbolic cosine).

The non-linear system blocks depicted in Fig. 2 are very well suited for implementation in translinear circuits. A discussion about translinear circuits can be found in [85,86].

For an implementation with bipolar transistors, the normalizing voltage V_n in (2) will be equal to the thermal voltage V_T $(= kT/q)$ and the overall input-output relation (6) becomes:

$$I_{\text{out}} = \frac{I_n}{V_T C} \int I_{\text{in}} dt \tag{7}$$

Note that the integrator time constant τ $(= V_T C/I_n)$ can be controlled by the current I_n and that it becomes independent of temperature if I_n is made proportional to the absolute temperature (PTAT).

The implementation of the individual system blocks as depicted in Fig. 2 is discussed in the following subsections.

3.1. *The Current Splitter*

For a class-AB two-quadrant divider composed with two one-quadrant dividers, the bipolar input current I_{in} must be decomposed into two positive currents, I_1 and I_2, for separate processing. This can be realized with a current splitter. A current splitter, very well suited to implement in a translinear circuit, is the geometric-mean current splitter, which produces the two positive output currents $I_{1,2}$:

$$I_{1,2} = \pm \frac{I_{\text{in}}}{2} + \sqrt{\left(\frac{I_{\text{in}}}{2}\right)^2 + I_q^2} \tag{8}$$

with I_q the quiescent current of $I_{1,2}$.

This equation can be realized by implementing the following two equations:

$$I_{\text{in}} = I_1 - I_2 \tag{9}$$

$$I_q^2 = I_1 \cdot I_2 \tag{10}$$

The basic implementation of the designed current splitter is depicted in Fig. 3(a).

The translinear loop comprising transistors Q1 through Q4 implements a multiplier to realize the operation given by (10). The output current of the

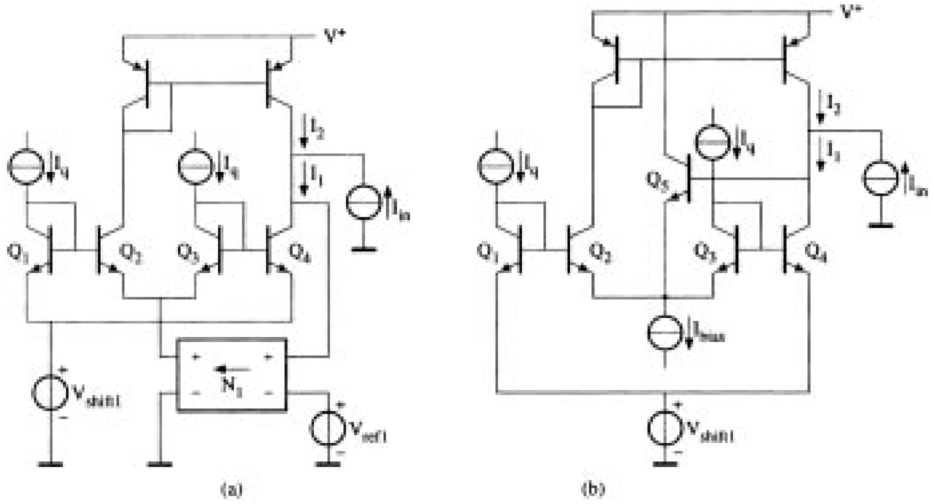

Fig. 3. Basic (a) and practical implementation (b) of the current splitter.

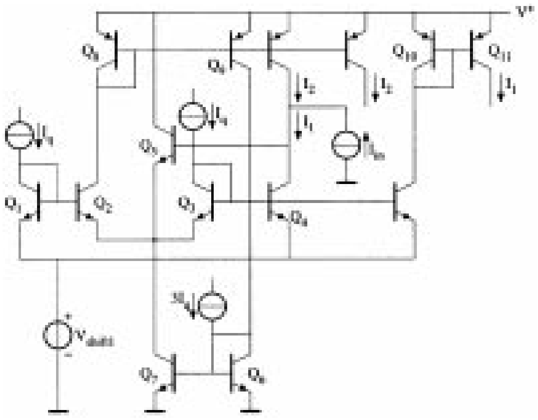

Fig. 4. The final implementation of the current splitter.

multiplier (I_2) is fed back to the input by a current mirror, to produce the difference of currents as given by (9). The voltage source V_{shift1} is necessary to ensure that the emitter voltages of Q2,3 are always positive. Note that this voltage source has no effect on the translinear loop. A convenient value for V_{shift1} is 200 mV. The nullor N1 enables the current I_1 to flow into the collector of Q4 and make it an input transistor of the multiplier. A practical implementation of the nullor N1 and the voltage source V_{ref1} is the emitter follower Q5, as depicted in Fig. 3(b).

A disadvantage of the circuit depicted in Fig. 3(b) is that bias current I_{bias}, if set to a fixed value, must be relatively large $(I_{\text{bias}} > I_q + I_{C,Q2})$ and, as a consequence, will largely contribute to the quiescent supply current consumption. A solution for this problem is the replacement of the current source I_{bias} by the circuit comprising transistors Q6,7,9 and the current source $3I_q$ in the final implementation of the current splitter as depicted in Fig. 4. The current mirror comprising transistors Q8,9 feeds the collector current of Q2 to the input of the current mirror comprising transistors Q6,7, and therefore the current through Q5 will be equal to $2I_q$, which can be much smaller than I_{bias}.

3.2. The Dividers

Once the bipolar input current I_{in} is decomposed into two positive currents $I_{1,2}$, such that the difference of these currents equals the input current, the two-quadrant dividing of the (bipolar) input current I_{in} can now be performed by the individual dividing of the currents $I_{1,2}$ by the (unipolar) divider current I_d, by means of two one-quadrant dividers. The divider output current $I_{D,\text{out}}$ is formed by a simple subtraction of the output currents $I_{D,\text{out1}}$ and $I_{D,\text{out2}}$ of the one-quadrant dividers according to:

$$I_{D,\text{out}} = \frac{-I_{\text{in}} I_n}{I_d} = \frac{I_2 I_n}{I_d} - \frac{I_1 I_n}{I_d} = I_{D,\text{out2}} - I_{D,\text{out1}} \tag{11}$$

The divider output currents $I_{D,\text{out1,2}}$ equal

$$I_{D,\text{out1,2}} = \frac{I_n I_{1,2}}{I_d} \tag{12}$$

and can be simply realized by a translinear divider.

The basic implementation of the realized one-quadrant divider is depicted in Fig. 5(a). The translinear loop comprising transistors Q12–Q15 implements a divider to realize the operation given by (12). The voltage source V_{shift2} is necessary to ensure that the base voltages of Q13,14 are always positive. Again, 200 mV is a convenient value. The nullor N2 enables the current I_n to flow into the collector of Q12 and make it an input transistor of the divider. A practical implementation of the nullor N2 and the voltage source V_{ref2} is the emitter follower Q16, as depicted in Fig. 5(b).

The implementation of the differential two-quadrant divider is depicted in Fig. 6. Note that in (11) the output currents $I_{D,\text{out1,2}}$ are exchanged. The reason for this is to have a PNP current mirror (Q10,11 and Q17,18) in both signal paths, from splitter output to divider output, instead of two current mirrors in one path and none in the other path. This improves the linearity of the composed two-quadrant divider. The polarity will be corrected in the implementation of *F*.

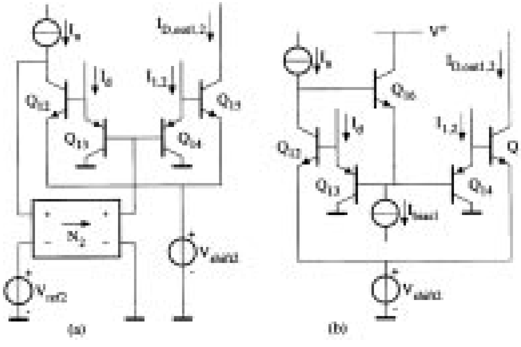

Fig. 5. Basic (a) and practical (b) implementation of the one-quadrant divider.

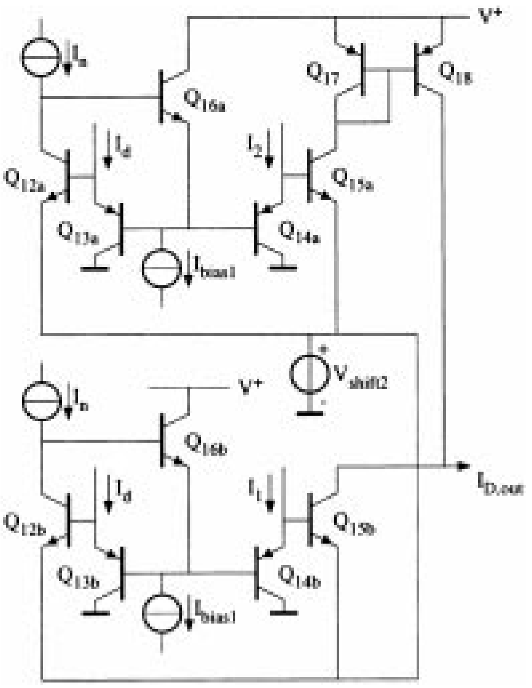

Fig. 6. The implementation of the differential two-quadrant divider.

3.3. *The Integrator/Buffer*

The current $I_{D,\text{out}}$ is integrated over time to produce the internal voltage V_C. The integration is performed by a single capacitor C. To minimize the interaction between the F/F' circuit and the capacitor, a voltage buffer is implemented. The principle of the integrator/buffer is depicted in Fig. 7(a). Ideally, the buffering is performed by the nullor N3. The level-shifting between the input and the output of the buffer, represented by the voltage source V_{shift3}, is necessary to avoid saturation of transistor Q15b of the divider circuit given in Fig. 6.

The practical implementation of the nullor N3 and the voltage source V_{shift3} is depicted in Fig. 7(b). The nullor is implemented by the transistors Q19,20 in common-emitter configuration. The output transistor Q20 must be able to sink the input current of the F/F' circuitry. The level-shift voltage source V_{shift3} is realized by the base-emitter voltage of transistor Q19.

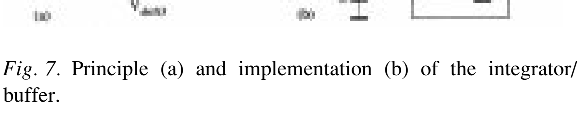

Fig. 7. Principle (a) and implementation (b) of the integrator/buffer.

3.4. *The* F/F′ *Circuitry*

The transfer function F must be an expanding function, to provide the companding in the circuit. Compared with a linear transfer function, expanding results in a reduced swing of the capacitor voltage V_C for the same swing of the output current I_{out}. This is beneficial in a low-voltage environment. Which function F is suitable depends on the operation mode (class A or class AB), and on the ease of implementation of F and its derivative F'. An easy-to-implement transfer function in electronics is the exponentional function describing the behavior of a bipolar transistor or a MOSFET in weak inversion. An advantage of the exponentional function is that the derivative is also an exponentional function and, therefore, it is also easy to implement. For this reason, this function is at the base of most of the bipolar or weak-inversion log-domain (translinear) filters. In the class-AB operated circuit presented here, bipolar transistors are used. In class-AB operation, the expanding function F must be a bipolar function. A natural choice for the function F is the hyperbolic-sine function, see, e.g., [8], and, as a consequence, the (derivative) function F' becomes the hyperbolic-cosine function. Therefore, I_{out} and I_d become:

$$\begin{aligned} I_{\text{out}} &= -2I_r \sinh\left(\frac{V_{\text{in}}}{V_T}\right) \\ &= I_r\left[\exp\left(-\frac{V_{\text{in}}}{V_T}\right) - \exp\left(\frac{V_{\text{in}}}{V_T}\right)\right] \\ &= (I-) - (I+) \end{aligned} \tag{13}$$

$$\begin{aligned} I_d &= 2I_r \cosh\left(\frac{V_{\text{in}}}{V_T}\right) \\ &= I_r\left[\exp\left(-\frac{V_{\text{in}}}{V_T}\right) + \exp\left(\frac{V_{\text{in}}}{V_T}\right)\right] \\ &= (I-) + (I+) \end{aligned} \tag{14}$$

with $V_{\text{in}} = V_C' - V_{\text{shift4}}$ and I_r a reference current.

Note that I_{out} is equal to the negative, instead of the positive, hyperbolic-sine function. This corrects the exchanging of $I_{D,\text{out}1,2}$, as mentioned before. The implementations of the hyperbolic-sine function (F) and the hyperbolic-cosine function (F') are combined in one circuit, as depicted in Fig. 8. This combination is also beneficial for the matching of the transfer function F' and the derivative dF/dV'_C, because now the same currents $I+$ and $I-$ are used for realizing the current I_{out} as well as the current I_d.

The two loops comprising the transistors Q21,22 and Q23,24 convert the input voltage V_{in} V_{in} $(= V'_C - V_{\text{shift4}})$ into the currents $I-$ and $I+$, respectively:

$$(I+) = I_r \exp\left(\frac{V_{\text{in}}}{V_T}\right) \tag{15}$$

$$(I-) = I_r \exp\left(-\frac{V_{\text{in}}}{V_T}\right) \tag{16}$$

The hyperbolic-sine function (F), which produces the output current I_{out}, is realized by a simple subtraction of the currents $I+$ and $I-$ as given in (13). The hyperbolic-cosine function (F'), which produces the divider current I_d, is realized by a simple summation of the currents $I+$ and $I-$ as given in (14). The voltage source V_{shift4} is necessary to ensure that the emitter voltages of Q22,23 are always positive. Once again, 200 mV is a convenient value.

The output current $-I_{\text{out}}$ is added to easily enclose the integrator in a unity-feedback configuration by connecting the $-I_{\text{out}}$ output to the input of the integrator, which results in a first-order low-pass filter.

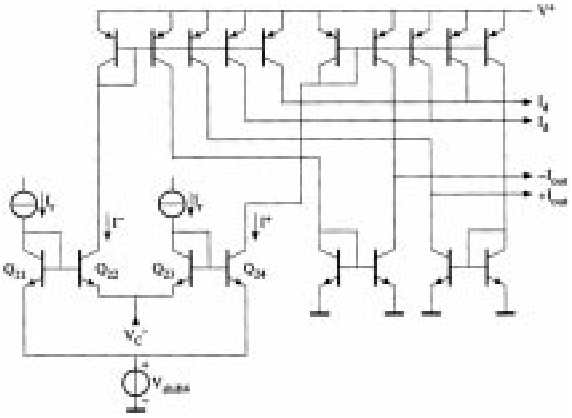

Fig. 8. The implementation of the F/F' transfer functions.

3.5. *Overall Design*

Now that all the system blocks have been designed at circuit level, the subcircuits can be linked together to form the integrator as depicted in Fig. 2. The biasing of the integrator is ensured by enclosing it in a feedback configuration, as mentioned before. This results in a first-order low-pass filter that must, for use in a hearing instrument, fulfill the following requirements [1] (Table 1):

For simulation and measurement purposes, the biasing current sources I_q, I_r, $I_{\text{bias}1}$ and $I_{\text{bias}2}$ are realized by simple current mirrors and high-valued resistors. The control current I_n is realized with a PTAT current source.

4. Simulation and Measurement Results

4.1. *Simulation Results*

The integrator has been simulated using PSPICE and transistor models of the Philips BIMOS L00422 process. Typical (bipolar) transistor parameters are: $I_{S,\text{NPN}} \approx 50\,\text{aA}$, $h_{\text{fe,NPN}} \approx 180$, $f_{T,\text{NPN}} \approx 3\,\text{GHz}$, $I_{S,\text{LPNP}} \approx 60\,\text{aA}$, $h_{\text{fe,LPNP}} \approx 90$ and $f_{T,\text{LPNP}} \approx 16\,\text{MHz}$. Simulations of the designed circuit confirm correct operation, according to the above-listed requirements, for sinusoidal input signals, with $V+ = 1\,\text{V}$, $I_q = I_r = I_{\text{bias}1,2} = 45\,\text{nA}$, $V_{\text{shift}1,2,4} = 200\,\text{mV}$ and $C = 100\,\text{pF}$. The results of the simulations are given in Table 2.

4.2. *Measurement Results*

To verify the integrator operation in practice, a semi-custom version of the active circuitry of the complete filter has been integrated in our in-house 2-μm, 7-GHz process, fabricated at the Delft Institute of Microelectronics and Submicron Technology. Typical transistor parameters are: $I_{S,\text{NPN}} \approx 14\,\text{aA}$, $h_{\text{fe,NPN}} \approx 100$, $f_{T,\text{NPN}} \approx 7\,\text{GHz}$, $I_{S,\text{LPNP}} \approx 8\,\text{aA}$, $h_{\text{fe,LPNP}} \approx 80$ and $f_{T,\text{LPNP}} \approx 40\,\text{MHz}$. I_q, I_r and $I_{\text{bias}2}$ are set to the value of 45 nA. $I_{\text{bias}1}$ is set to 135 nA, instead of 45 nA, to avoid instability. The capacitor C $(= 100\,\text{pF})$ is connected externally. The voltage sources $V_{\text{shift}1,2,4}$ are implemented by a resistive voltage divider set to 200 mV. The measurement results are given in Table 3 and are in good agreement

Table 1. Required specifications of the translinear integrator.

Quantity	Value	Comment
Supply voltage ($V+$)	V	
Current consumption	$< 5\,\mu$A	$I_{\text{in,max}} = 180$ nA (p)
Cutoff frequency (f_c) range	1.6 kHz–8 kHz	controllable
Dynamic range	> 68 dB	Hz–8 kHz
Total harmonic distortion	$< 2\%$	$f = 1$ kHz, $f_c = 1.6$ kHz, $I_{\text{in}} < 130$ nA (p)
	$< 7\%$	$f = 1$ kHz, $f_c = 1.6$ kHz, $I_{\text{in}} > 130$ nA (p)

Table 2. Simulation results of the class-AB translinear integrator.

Quantity	Value	Comment
Minimal supply voltage	0.94 V	
Supply current	$1.7\,\mu$A	$I_{\text{in}} = 180$ nA (p)
Quiescent supply current	$1.4\,\mu$A	
Cutoff frequency range	1 kHz– > 8 kHz	
Total harmonic distortion	1.1%	$f = 1$ kHz, $f_c = 1.6$ kHz, $I_{\text{in}} = 180$ nA (p)
Dynamic range	77 dB	100 Hz–8 kHz

Table 3. Measurement results of the class-AB translinear integrator.

Quantity	Value	Comment
Minimal supply voltage	0.95 V	
Supply current	$1.9\,\mu$A	$I_{\text{in}} = 180$ nA (p)
Quiescent supply current	$1.6\,\mu$A	
Cutoff frequency range	1 kHz– > 8 kHz	
Total harmonic distortion	1.2%	$f =$ kHz, $f_c = 1.6$ kHz, $I_{\text{in}} = 100$ nA (p)
	2.8%	$I_{\text{in}} = 200$ nA (p)
	4.1%	$I_{\text{in}} = 300$ nA (p)
	5.5%	$I_{\text{in}} = 400$ nA (p)
	7.0%	$I_{\text{in}} = 500$ nA (p)
Dynamic range	73 dB	100 Hz–8 kHz

Table 4. Class-AB translinear filters.

	[27]	[26]	[this work]	[65]	[79]
Process	$2\,\mu$ BiCMOS	$1\,\mu$ BiCMOS	Bipolar	Bipolar	Bread-board
Filter	LPF, 3	LPF, 3	LPF, 1	APF, 2	LPF, 1
f_c [Hz]	10 k–100 k	10 k–15 M	1 k–8 k	155 k	1.6 k
DR [dB]	—	65	73	62	76
Total C [pF]	500	59	100	80	100
Power [W]	$180\,\mu$	$65\,\mu$	$2\,\mu$	$2\,\mu$	$1\,\mu$
Supply [V]	4	1.2	1	1.8	3.3

with the simulations, despite the fact another process is used.

4.3. Comparison with Other Implementations

Many skilfully designed class-AB translinear integrators have been presented in literature. Only few of them have been actually experimentally verified. To the authors' knowledge, to date, this amounts to a total of four different class-AB translinear filter designs [26,27,65,79]. The specifications of these filters and the here presented filter are summarized in Table 4.

The conclusions that can be drawn from this table speak for themselves and are thus left to the reader.

5. Conclusions

In this paper, a new implementation of a class-AB operated translinear integrator has been presented. The integrator operates from a single supply voltage down to 0.95 V. The total current consumption is less than 1.9 μA for an input current of 180 nA (p). The unity-gain frequency of the integrator can easily be controlled by a current. The integrator makes use of a single grounded capacitor and, therefore, matching of capacitors is not needed. The results of simulation and measurements of the integrator meets the required specifications for the application in hearing instruments.

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