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A 3.3 V Current-Controlled $\sqrt{}$-Domain Oscillator

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Abstract. In this paper, the strong inversion MOS analog of the recently proposed class of log-domain filters, or translinear filters, is proposed.The dynamic $\sqrt{}$ -domain principle, or dynamic voltage-translinear principle, exploits the quadratic law, describing the MOS transistor in the strong inversion region, both to perform an expanding V-I conversion of the capacitor voltages and to implement multiplications and square roots of currents based on the voltage-translinear principle.The presented theory is applied to the design of a current-controlled two-integrator oscillator. Experiment results of a pure CMOS test IC show the feasibility of the $\sqrt{}$ -domain principle. The realized oscillator has a THD of -42 dB and is linearly frequency tunable across 1.3 decades.

Key Words: integrators, oscillators, current-mode, companding

1. Introduction

Filters employing instantaneous or syllabic companding are receiving increasing interest due to the trend to lower supply voltages [1–7]. In conventional filter realizations, e.g. g_m-C filters, the signal voltage swings are limited by the available supply voltage. Since these filters are based on linear elements, the signal current swings are also limited directly by the supply voltage. A possible solution to overcome the limited signal current swings is to employ companding. By exploiting the nonlinear concave voltage-to-current characteristic of the bipolar transistor or the MOS transistor, the voltage swings in a companding filter are much smaller than the current swings. Thus, larger signal swings are possible in a companding filter relative to filters based on linear elements, which is beneficial with respect to the dynamic range.

Despite the local nonlinearities, companding filters can have an overall linear transfer function [2–7]. An interesting example of companding filters are the translinear, or log-domain, filters, which are inherently instantaneously companding [2,8,9]. Translinear filters exploit the exponential law describing the bipolar transistor, or the MOS transistor in weak inversion, to compress the input current of the filter and also to implement multiplications of currents according to the translinear principle [10].

In MOS IC processes, translinear filters can be realized by operating the MOSTs in the subthreshold region [11]. However, subthreshold operation is limited to low frequencies. Fortunately, the companding principle on which translinear filters are based can be generalized to MOSTs operating in strong inversion [6]. A current-mode approach has to be used. A voltage-mode approach results in filters which are not companding [12].

In this paper, the design of a companding $\sqrt{}$-domain current-controlled oscillator is described. In Section 2, the design principles of $\sqrt{}$-domain operation are treated. These principles were used to design an integrator, described in Section 3. Based on the integrator, a current-controlled harmonic oscillator was designed, described in Section 4. An experimental prototype of the oscillator was realized. The measurement results are presented in Section 5.

2. Design Principles

Dynamic $\sqrt{}$-Domain Principle

The $\sqrt{}$-domain principle, the strong inversion MOS analog of the log-domain principle, will be explained

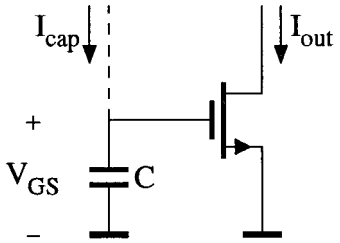

Fig. 1. The dynamic $\sqrt{}$-domain principle.

with the help of the generic subcircuit shown in Fig. 1. Using the simple quadratic law to describe the large signal behavior of the MOS transistor, the drain current I_{out} can be expressed as:

$$I_{out} = \frac{\beta}{2}(V_{GS} - V_{th})^2 \tag{1}$$

where β, V_{GS} and V_{th} are the transconductance factor, the gate-source voltage and the threshold voltage, respectively.

Due to the nonlinear large signal behavior of the MOST, the swing of the capacitance voltage V_{cap}, which equals V_{GS}, is smaller than the MOST's drain current swing. This is illustrated in Fig. 2, which is based on the ideal mathematical relations. In this figure, the drain current consists of the superposition of a DC current of 5 μA and a sine wave with an amplitude of 4.75 μA and a frequency of 100 kHz. The MOST's threshold voltage and the transconductance factor are 0.75 V and 40 $\mu A/V^2$, respectively. The capacitance is 20 pF. Of course, the instantaneous compression of the capacitance voltages in a $\sqrt{}$-domain filter will be less than in a log-domain filter, since the exponential function is far steeper than the quadratic law.

The capacitance voltage swing is only of interest with respect to the available supply voltage. The capacitance current I_{cap} is actually much more interesting, since we are pursuing a current-mode approach. Due to the square law, I_{cap} is nonlinearly related to I_{out}. In contrast with V_{cap}, the shape of I_{cap} is also dependent on the frequency of the AC component in I_{out}. In the situation depicted in Fig. 2, the current swings of I_{cap} and I_{out} are in the same order of magnitude. Consequently, at current level there is no companding.

An expression for I_{cap} can be found from the constitutive law. To this end, we need to know the derivative with respect to time of $V_{GS} = V_{cap}$, which can be found from eqn (1). This yields:

$$I_{cap} = \frac{C}{\sqrt{2\beta I_{out}}}\dot{I}_{out} \tag{2}$$

where the dot represents differentiation with respect to time.

A better insight into the dynamic $\sqrt{}$-domain principle is obtained by slightly rewriting this equation:

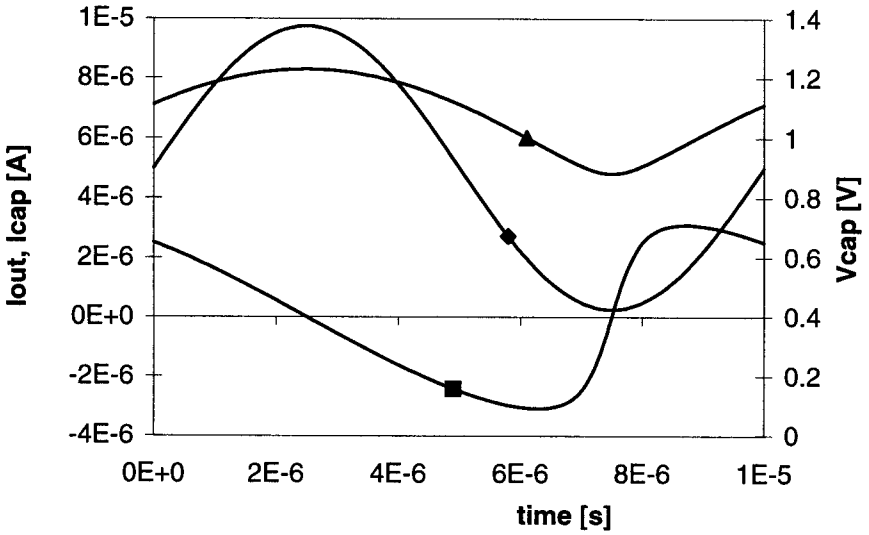

Fig. 2. Drain current (◆) and capacitance current (■) and voltage (▲) in the companding subcircuit shown in Fig. 1.

$$\frac{C_{out}}{\sqrt{2\beta^i}} = \sqrt{I_{out}} I_{cap} \tag{3}$$

The dynamic √-domain principle thus reads: *A derivative of a current can be replaced by the product of the square root of that current and a capacitance current*. This implies that instead of realizing the derivative on the left-hand side of equation (3), we can implement the current-mode algebraic equation on the right-hand side of (3). As the right-hand side is part of the implementation, the left-hand side is part of the differential equation realized. Consequently, this differential equation will be process and temperature dependent through β.

Voltage-Translinear Principle

In strong inversion, products and square roots of currents can be realized by means of the voltage-translinear principle [13–15] (a term coined by Gilbert [16]). Voltage-translinear circuits are based on the linear (affine, to be exact) relation between the transconductance g_m and the gate-source voltage of an MOST operating in strong inversion, which follows from equation (1).

A four-transistor voltage-translinear loop, in up-down topology, is shown in Fig. 3, comprising two MOSTs connected clockwise and two connected counterclockwise. According to Kirchhoff's voltage law, the gate-source voltages add up to zero. Assuming the threshold voltages and the transconductance factors are equal, a current-mode expression describing the voltage-translinear loop can be found [14,15]:

$$\sqrt{I_1} + \sqrt{I_3} = \sqrt{I_2} + \sqrt{I_4} \tag{1}$$

This equation, and generalized forms, can be used to realize current-mode algebraic operations like multiplication and the square root, which is exactly what is needed to implement the dynamic √-domain principle.

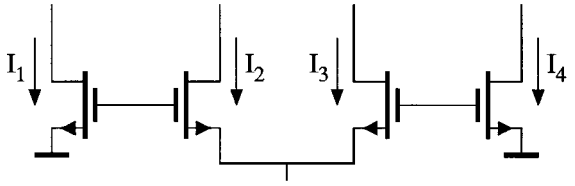

Fig. 3. Voltage-translinear loop.

Square Law Conformity

Both the dynamic √-domain principle and the voltage-translinear principle rely on the quadratic behavior of the MOST operating in strong inversion. However, the square law is quite a coarse simplification of the MOST's behavior [17]. The square law model is only valid across approximately 1.5 decades of current [15]. At the low end, the square law is limited by the moderate inversion region. At the high end, it is limited by carrier mobility reduction. The square law is far less exact than the exponential law, describing the bipolar transistor, on which the translinear principle is based. Therefore, it is advisable to check the range of validity of the square law model.

Some measurements were performed on a 1.6 μm, n-well CMOS process, which was used to implement the √-domain oscillator described in Section 4. In Fig. 4, a measurement is shown of a MOST having dimensions $W = L = 20$ μm. The drain current was measured for gate voltages from 0.7 V to 3 V; higher gate voltages are not very interesting for low-voltage operation. The measured drain current was fitted on the ideal square law (1). To emphasize the difference between the measured and the fitted curve in the moderate inversion region, the drain current is plotted on a logarithmic scale. The fitted parameters are $V_{th} = 0.815$ V and $\beta = 56.8$ μA/V^2. The plotted error curve shows that the fit is accurate to within 1% for drain currents ranging from 5.6 μA to more than 135 μA, which corresponds to more than 1.4 decades of drain current. Although this range is much smaller than the validity of the exponential law for the bipolar transistor, which is valid across approximately eight decades, it is sufficient to justify the application of the simple square law model.

3. Voltage-Translinear Integrator

Any integrator can be described by the dimensionless differential equation:

$$\dot{z} = x \tag{5}$$

where the dot represent differentiation with respect to

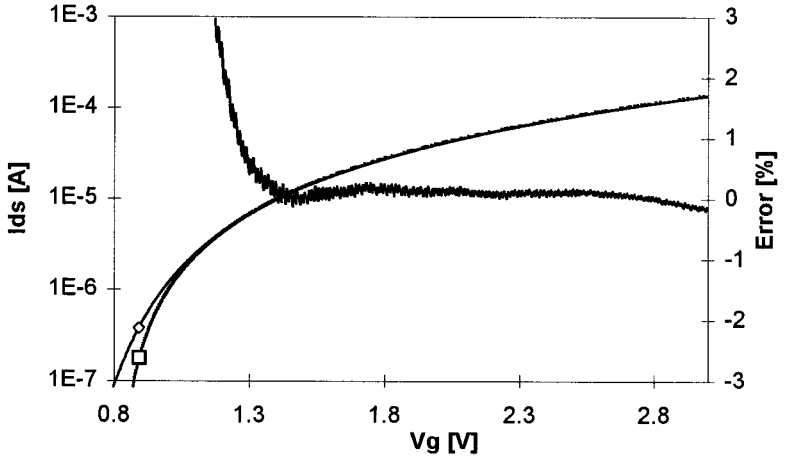

Fig. 4. Measured ◇ and fitted □ drain current and the error between measurement and square law.

the dimensionless time τ and x and z represent the input and output signal, respectively.

In order to implement an integrator using the design principles discussed in the previous section, equation (5) has to be transformed into a differential equation with the proper dimensions. As both the $\sqrt{}$-domain principle and the voltage-translinear principle are basically current-mode, it is obvious that x and z have to be transformed into currents. This is accomplished by defining the equivalence relations:

$$x = \frac{I_{in}}{I_o} \qquad z = \frac{I_{out}}{I_o} \tag{6}$$

where I_{in} and I_{out} are the input and output current of the integrator, respectively, and I_o is an arbitrary DC current.

The dimensionless time τ implicitly presented in equation (5) has to be transformed into the usual time t with dimension $[s]$. This can be done by applying the transformation:

$$\frac{\partial}{\partial \tau} = \frac{C\sqrt{I_{o1}}}{\sqrt{2\beta} I_{o2}} \frac{\partial}{\partial t} \tag{7}$$

where I_{o1} and I_{o2} are DC bias currents. From this equation, it follows directly that frequency, the inverse of time t, is linearly controllable through I_{o2}.

Applying the above transformations, a differential equation is obtained having the proper dimensions for a $\sqrt{}$-domain implementation to be possible:

$$\frac{C\sqrt{I_{o1}}}{\sqrt{2\beta}} \dot{I}_{out} = I_{o2} I_{in} \tag{8}$$

The derivative $\dot{I}_{out}$ in equation (8) can be eliminated if we introduce a capacitance current I_{cap} according to equation (2) corresponding to Fig. 1. Using equation (2) to eliminate the derivative $\dot{I}_{out}$ from (5) an algebraic equation is obtained:

$$\sqrt{I_{out} I_{o1}} I_{cap} = I_{o2} I_{in} \tag{9}$$

If we are able to implement this equation, we have actually implemented the integrator described by equation (8).

To implement equation (9), the voltage-translinear principle can be used. Equation (9) has to be mapped onto one or more voltage-translinear loop equations (4). Unfortunately, no analytical synthesis method for mapping algebraic equations on voltage-translinear loop equations exists [15]. The numerical method described in [15] cannot be used either, since it is limited to single-loop four-transistor circuits, having one input, one output and one bias current. In equation (9), an input current, and output current, two bias currents I_{o1} and I_{o2}, and a capacitance current are present.

The only alternative is to split equation (9) into several simpler parts, which can be realized by existing voltage-translinear circuits. The term $\sqrt{I_{out} I_{o1}}$ can be realized by a square root circuit [14]. Next, a multiplier/divider can be used to realize the product $I_{o2} I_{in}$ and divide it by the output of the

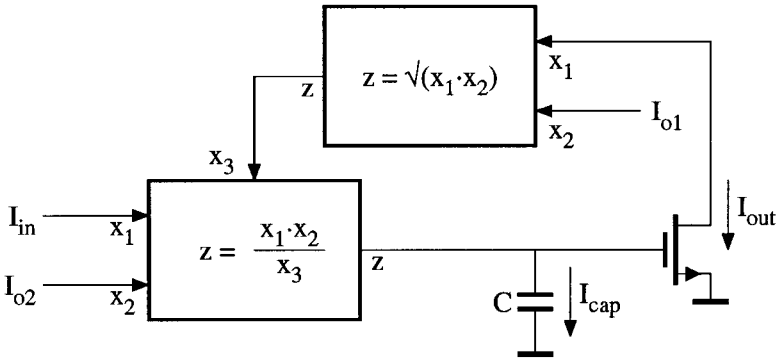

Fig. 5. Block schematic of a voltage-translinear integrator.

square root circuit [15,18]. Then, the output of the multiplier is the capacitance current I_{cap}. The subcircuit shown in Fig. 1 defines the relation between I_{cap} and I_{out}. A block schematic of the solution thus obtained is shown in Fig. 5.

Square Root Circuit

A voltage-translinear square root circuit was published in [14,15]. The circuit is depicted in Fig. 6.

Its loop equation is given by:

$$\sqrt{I_{x_1}} + \sqrt{I_{x_2}} = 2\sqrt{\frac{I_{x_1} + I_{x_2}}{4} + I_z} \qquad (10)$$

where I_{x_1} and I_{x_2} are two input currents and $I_z = \frac{1}{2}\sqrt{I_{x_1} I_{x_2}}$ is the output current of the square root circuit. The relation between these currents and Fig. 5 is given by: $I_{x_1} = I_{out}$, $I_{x_2} = I_{o1}$ and $I_z = \frac{1}{2}\sqrt{I_{o1} I_{out}}$.

A disadvantage of the circuit shown in Fig. 6 is that it is based on a stacked translinear loop, which is sensitive to body effect [15]. Due to the body effect, the threshold voltages of the MOSTs in a stacked loop differ, and as a consequence, errors are introduced in the general equation (4) unless all MOSTs have individual wells connected to their sources, which is disadvantageous with respect to bandwidth.

In up-down topologies, the influence of the body-effect is much smaller. Therefore, a new square root circuit is designed by mapping equation (10) onto a voltage-translinear loop in up-down topology, shown in Fig. 3. The resulting circuit is shown in Fig. 7. Transistors $M_1 - M_4$ make up the translinear core. The dimensions chosen for $M_1 - M_4$ are $W = 10$ μm and $L = 12$ μm. The current-mirror $M_5 - M_6$ is used to supply both M_2 and M_3 with the output current I_z

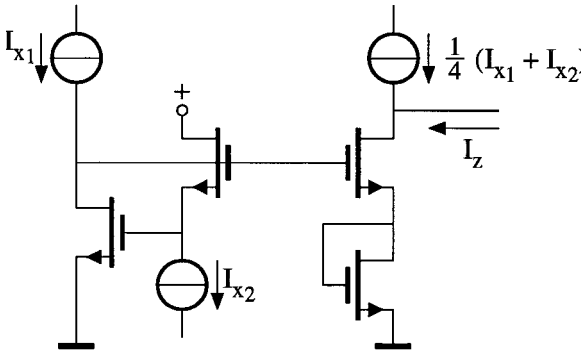

Fig. 6. Square root circuit, stacked topology.

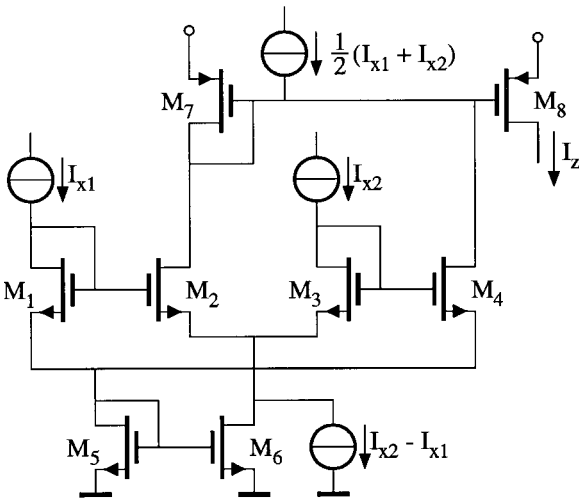

Fig. 7. Square root circuit, up-down topology.

according to equation (10) [15]. The aspect ratio of the current mirror transistors is chosen to be quite large, to gain some voltage room for the transistors of the translinear core at low supply voltages. The dimensions of M_5 and M_6 are $W = 200$ μm and $L = 8$ μm.

Multiplier

Multiplier circuits are often based on the well-known quarter-square principle: $(a+b)^2 - (a-b)^2 = 4ab$. Using this expression, a multiplier can be constructed from two square circuits. In [15,18], four-quadrant voltage-translinear multipliers are presented, which are based on the quarter-square principle.The resulting circuits have a kind of differential difference input structure.

The multiplier described in [15] is based on translinear loops in up-down topology, which are insensitive to the body effect. This circuit is shown in Fig. 8. The voltage-translinear cores of the two square circuits is formed by $M_1 - M_4$ and $M_{11} - M_{14}$, respectively. The output currents of the square circuits are subtracted by means of a PMOS current mirror, yielding the output current I_z of the four-quadrant multiplier, which is given by $I_z = I_{x_1} I_{x_2}/(2I_{x_3})$. This current is supplied to the capacitance shown in Fig. 5. The relations between the input currents I_{x_1}, I_{x_2} and I_{x_3} and the output current I_z of the multiplier shown in Fig. 8, and the currents in the block schematic shown in Fig. 5 are given by: $I_{x_1} = I_{in}$, $I_{x_2} = I_{o2}$, $I_{x_3} = \frac{1}{2}\sqrt{I_{o1} I_{out}}$ and $I_z = I_{cap}$.

For reasons of voltage compatibility between the PMOS current mirror load of the multiplier and the integrator output transistor, a PMOS output transistor is used for the integrator. By choosing equal dimensions for the output PMOST as for the PMOSTs comprising the current mirror, the two output voltages of the square circuits, comprising the multiplier, are identical, thus reducing the even-order distortion of the multiplier.

Complete Voltage-Translinear Integrator

Employing the square-root circuit, shown in Fig. 7, and the multiplier, shown in Fig. 8, in the block schematic, shown in Fig. 5, the complete voltage-translinear integrator thus obtained is depicted in Fig. 9. Note that the output structure, shown in Fig. 1, of the integrator is not part of any translinear loop. In most published log-domain filters/integrators, this output structure is part of the translinear loop. However, this is not a necessary condition, which is illustrated by the log-domain integrator described in [19].

The output of the integrator has to be class A biased. Therefore, a DC bias current source is connected from the drain of the output transistor of the integrator to ground.

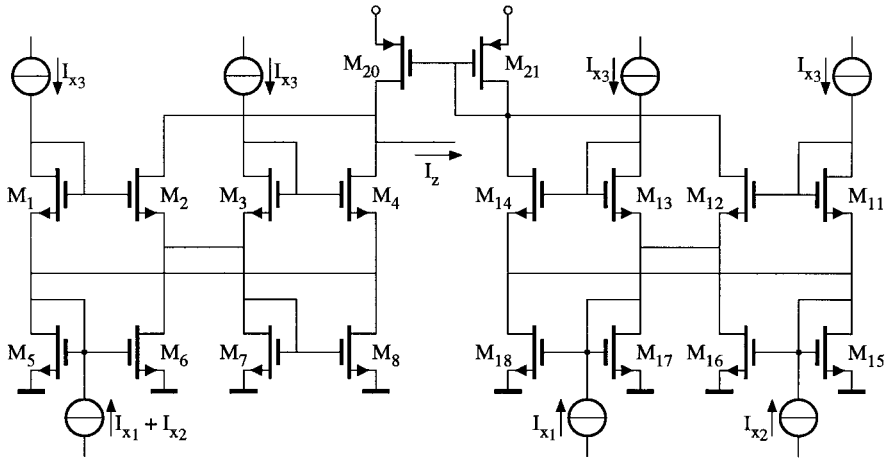

Fig. 8. Four-quadrant multiplier/divider.

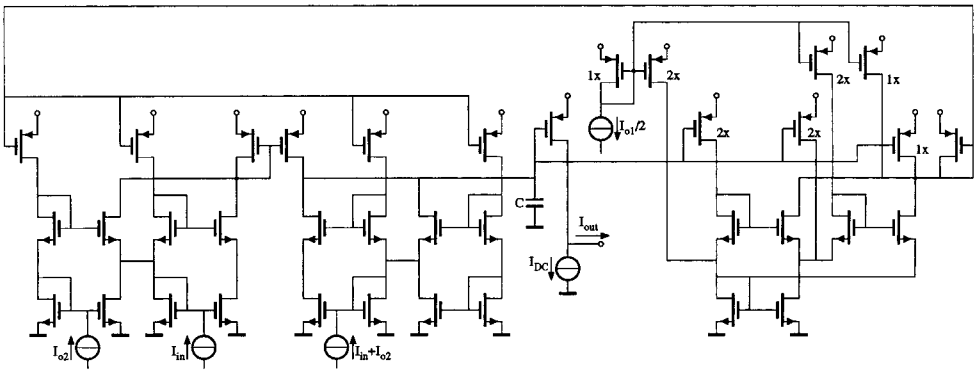

Fig. 9. √-domain integrator.

4. CCO Design

The integrator described in the previous section was used to design a current-controlled harmonic oscillator. By applying negative feedback to a cascade of two integrators, a two-integrator oscillator is obtained. The block schematic of the realized two-integrator oscillator is shown in Fig. 10. The oscillation frequency of the loop equals the unity-gain frequency of the integrators, which is given by:

$$\omega_c = \frac{\sqrt{2\beta}I_{o2}}{C\sqrt{I_{o1}}} \tag{11}$$

The oscillation frequency can be tuned linearly by means of I_{o2}.

A loop of two integrators and an inverter is described by a linear differential equation, which cannot posses a unique limit cycle. In other words, an amplitude control circuit is required, which is also depicted in Fig. 10. A fixed amplitude is maintained by controlling the amount of local feedback of the integrators. Negative feedback causes a decrease of the oscillation amplitude, and positive feedback causes an increase. To be able to apply both positive and negative feedback to the integrators, a four-quadrant multiplier is required in the local feedback paths. The voltage-translinear multiplier shown in Fig. 8 is used to this end.

The integrator, shown in Fig. 9, has a differential input structure. Therefore, it is not necessary to convert the output of the multiplier to a single output current by means of the PMOS current mirror shown in Fig. 8. Since the output voltage levels of M_4 and M_{14}, shown in Fig. 8, are not compatible with the input voltage levels of the integrator, it is necessary to load the two square circuits, comprising the multiplier, with two PMOS current mirrors. The differential output current of these two current mirrors is supplied to the differential input of the integrator.

The amplitude is measured by adding the squares of the two quadrature outputs of the oscillator, yielding the square of the amplitude [20]. Two voltage-translinear square circuits, which were also

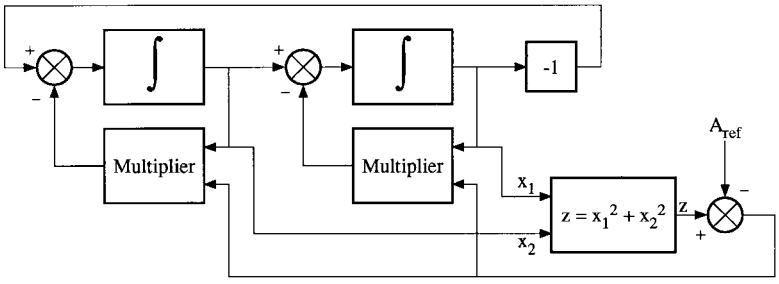

Fig. 10. Two-integrator oscillator.

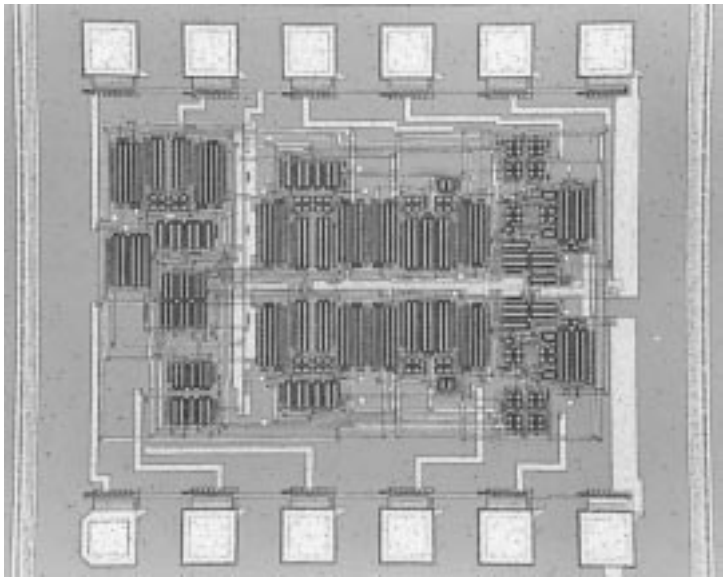

Fig. 11. Photograph of the oscillator.

employed in the multiplier shown in Fig. 8, can be used to this end. The output currents of the square circuits are added by connecting the output terminals. The square of the oscillation amplitude, thus obtained, is compared with a reference current. The difference is applied to the second input of the feedback multipliers, thus controlling the local feedback of the integrators.

In the set-up shown in Fig. 10, the amplitude and the frequency can be tuned independently [20], by means of I_{o2} and A_{ref}, respectively.

5. Measurement Results

To verify the dynamic $\sqrt{}$-domain principle, the

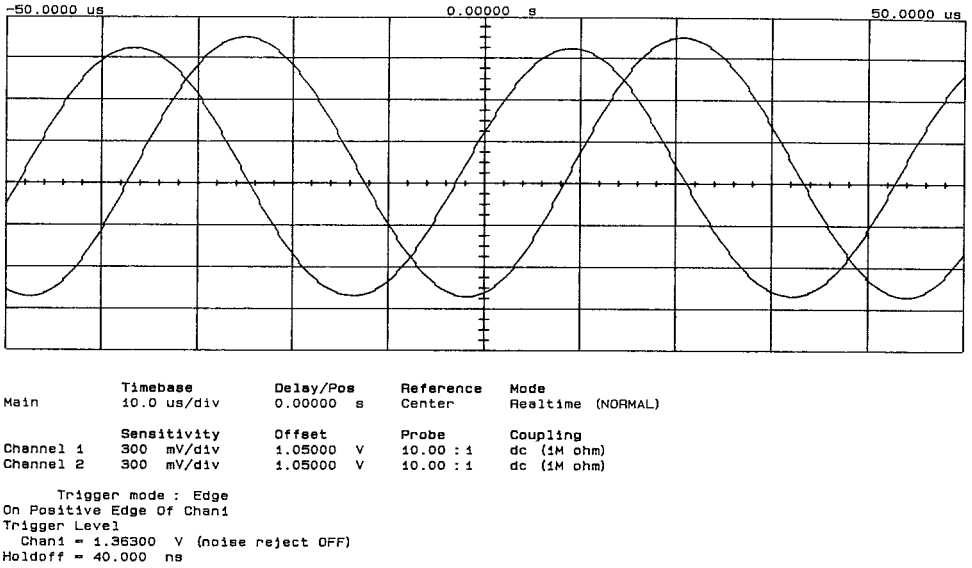

Fig. 12. Output currents of the oscillator.

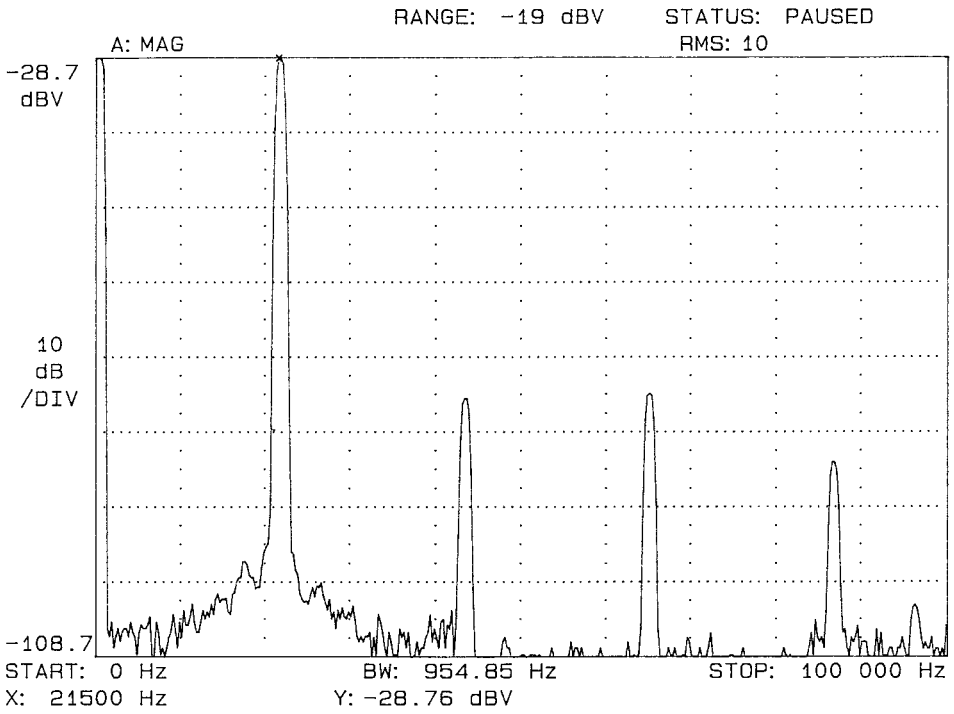

Fig. 13. Frequency spectrum of the oscillator.

current-controlled √-domain oscillator was realized in a 1.6 μm n-well CMOS process. Fig. 11 shows a chip photograph of the prototype oscillator. The two capacitors of the oscillator are external. Also, all DC bias and control currents are supplied externally.

The oscillator occupies a chip area of 0.65 mm^2. Most area is consumed by the current mirrors, which are operated in the moderate inversion region to gain some voltage room. The oscillator is designed for a supply voltage of 3.3 V. An interesting alternative with respect to both low-voltage operation and required chip area is the operation of MOSTs in the triode region [21–24]. The possibilities offered by voltage-translinear loops comprising MOSTs operating in the triode region will be the aim of future research.

Fig. 12 shows the quadrature output currents of the oscillator. The output currents of the two integrators

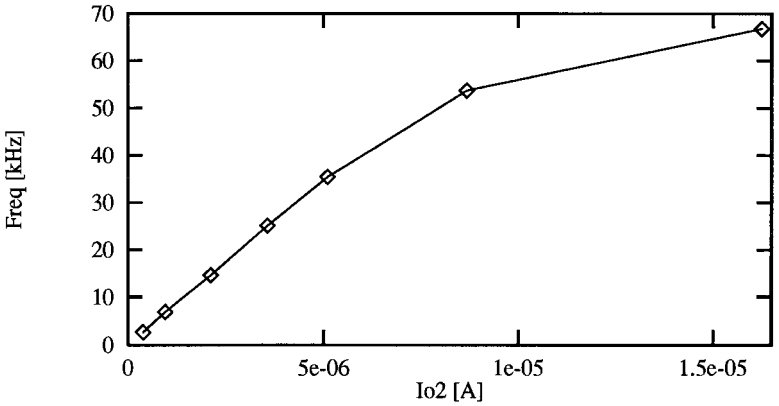

Fig. 14. Frequency control of the oscillator.

are measured across two resistors of 100 kΩ. The DC current used to bias the integrators in class A is 5 μA. The oscillation amplitude is 3.6 μA, which is 72% of the class A bias current.

The capacitors have a value of 82 pF. The control currents I_{o1} and I_{o2} are 5 μA and 3.1 μA, respectively. With equation (11), this amounts to an oscillation frequency of 28 kHz. The measured oscillation frequency is 22 kHz.

Fig. 13 shows the measured output spectrum of the oscillator. To prevent distortion caused by the output voltage swing across the load resistor in relation to the output conductance of the output MOST, an external CB stage is used to buffer the output current. The harmonic distortion is mainly caused by the second and third harmonic at -46 dB and -45 dB, respectively.

The frequency tunability as a function of I_{o2} was measured for the same values of the capacitors and the bias currents.The results are shown in Fig. 14. The figure shows that the oscillator is linearly tunable from about 2.6 kHz to 53 kHz. For large values of the control current I_{o2}, correct operation of the voltage-translinear integrator is prohibited by the limited supply voltage.

6. Conclusions

In this paper, the strong inversion MOS analog of the recently proposed log-domain principle, also called the dynamic translinear principle, has been derived. The $\sqrt{}$-domain principle, or dynamic voltage-translinear principle, is based on the quadratic law describing the MOST in the strong inversion region. Measurements showed an accurate quadratic behavior across at least 1.5 decades of drain current. The $\sqrt{}$-domain principle can be used to substitute algebraic equations for the derivatives in a differential equation. These algebraic equations can be implemented by means of the voltage-translinear principle.

The $\sqrt{}$-domain principle has been illustrated by the design of a current-controlled two-integrator oscillator. The oscillator has been implemented in a 1.6 μm n-well CMOS process. The measured oscillator has a THD of -42 dB and is linearly frequency tunable from 2.6 to 53 kHz.

Future research aims at the application of MOSTs operating in the triode region, which might be advantageous with respect to required chip area and supply voltage.

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