Analog Integrated Circuits and Signal Processing, 9, 207–214 (1996)

Design Rules for an Integratable Low-Power Amplifier/Filter Combination

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Abstract. In this paper design rules for a circuit topology in which there is an inseparable combination of an amplifier and a filter characteristic, are presented. By intentionally using the capacitance of an *already present* input sensor for the filtering, the total required integrated capacitance is *much less* than that in circuits, which have a separately designed amplifier and filter function. Consequently, it is possible to have the advantage of a better integratability. Moreover, less complexity in the design is achieved. The presented circuit shows a current-to-voltage conversion and an inherently controllable second-order low-pass filter characteristic. A discrete realization has been designed to test the circuit. This circuit operates down to a 1 V supply voltage and the transfer shows a 1.8 MΩ current-to-voltage conversion with a bandwidth of 6 kHz. Measurement results of this circuit show that a 63 dB dynamic range can be achieved with a total required integrated capacitance of only 31 pF.

1. Introduction

Normally, if both building blocks are required, amplifiers and filters are designed separately: a circuit is designed to realize the amplification and an additional circuit to realize the filter function. In this paper, a circuit where both operations are inseparably combined, an amplifier/filter combination, is presented. This circuit is a transimpedance amplifier. When an input sensor, that is *already present*, has a capacitive character and the capacitance is much larger than the parasitic capacitances of the transistors used to realize the circuit (in the order of > 10 pF), it is possible to advantageously use this capacitance. This means a decrease in the total required integrated capacitance and, consequently, in the required chip area. Examples of input sensors with sufficiently large capacitance are piezo-electrical elements, photodiodes and electret microphones. By using this capacitance (this means that the amplifier/filter combination must be located at the input of a total system) and the *presence* of the parasitic feedback capacitance of a transistor, it appears that the circuit shows an inherently *controllable* second-order low-pass filter characteristic. The advantages of this amplifier/filter combination in comparison with circuits with separately realized amplifiers and filters are then as follows. For the same dynamic range, the use of amplifier/filter combinations can under certain conditions yield a better integratability of the circuit and simultaneously lead to a reduction of the circuit's complexity. Moreover, a lower power consumption can be achieved.

A circuit that uses a photodiode as an input sensor is discussed here. The circuit is designed to realize an amplification and filter characteristic to be used in an infra-red receiver for hearing aids [1]. An example of another application is an anti-aliasing filter, combined with a preamplifier.

Design rules are presented for the amplifier/filter combination. These rules only apply to a fixed topology, namely of a transimpedance amplifier. The easiest designs appear to be those for low-power applications. An example of such a design is discussed here. Measurement results of the performance of this design are given.

2. Fundamental Aspects

Figure 1 depicts a generic block diagram of the amplifier/filter combination. I_s represents the current of the input sensor and C_1 its capacitance. g_{m1} and g_{m2} are the transconductances of the first and second stage, respectively.

In the transfer of this circuit, two dominant complex poles arise. The positions of these poles can be controlled very effectively by several parameters. For the input-output relation applies [2]

$$A_f = A_{f\infty}\frac{-A\beta}{1-A\beta} \tag{1}$$

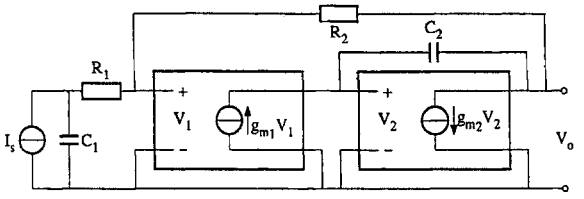

Fig. 1.

where $A_{f\infty}$ is the idealized transfer and $A\beta$ is the loop gain. If we choose g_{m2} the reference variable ($A = g_{m2}$), $A\beta$ shows two dominant complex phantom zeros [2]. In most cases, the positions of the zeros approximately fit the ends of the root locus and are then approximately in the same positions as that of the dominant poles in the transfer function. With this knowledge and with the aid of equation (1), we can find an expression for the dominant poles in the transfer:

$$p(s) = \left(\frac{R_1C_1C_2}{R_2} + C_1C_2\right)s^2 + \left(\frac{C_2}{R_2} + \frac{g_{m_1}R_1C_1}{R_2}\right)s + \frac{g_{m_1}}{R_2} \quad (2)$$

The validity of this polynomial $p(s)$ depends on the situation that the positions of the zeros in the loop gain approximately fit the ends of the root locus. The designer should always check whether this is true with the aid of a simulation program.

If $C_2/(g_{m1}C_1) \ll R_1 \ll R_2$, equation (2) can be reduced to a simplified quadratic equation. From this equation, manageable expressions can be derived for a specified design. If the assumption is made that a Butterworth (or maximally-flat magnitude) filter characteristic is to be realized, C_2 must satisfy

$$C_2 = \frac{g_{m_1}R_1^2C_1}{2R_2} \quad (3)$$

The bandwidth then amounts to

$$B = \frac{1}{\sqrt{2}\pi R_1C_1} \quad (4)$$

3. Practical Realization

Figure 2 depicts a realization of the generic block diagram shown in figure 1. The capacitor C_{ext} is the extra added capacitance, which together with the internal feedback capacitance of transistor Q_3 forms the capacitance C_2 in figure 1.

The first stage is realized by a differential pair. The second stage is realized by a CE-stage with an internal feedback capacitance. In this situation $p(s)$ changes into

$$p(s) = R_1C_1C_2\left(c_{\mu_1} + \frac{c_\pi}{2}\right)s^3 + \left(C_2\left(c_{\mu_1} + \frac{c_\pi}{2}\right) + \frac{R_1C_1C_2}{2r_\pi} + \frac{R_1C_1C_2}{R_2} + C_1C_2\right)s^2 + \left(\frac{C_2}{2r_\pi} + \frac{C_2}{R_2} + \frac{g_mR_1C_1}{2R_2}\right)s + \frac{g_m}{2R_2} \quad (5)$$

where $c_{\mu 1}$ is the feedback capacitance of Q_1 and g_m, r_π and c_π are the transconductance (in this case $g_{m1} = g_m/2$), the input resistance and the input capacitance, respectively, of Q_1 as well as Q_2.

Equation (5) can be reduced to the quadratic equation so that the equations (3) and (4) hold again. For this the following restrictions must hold

$$\frac{R_1C_1C_2}{2r_\pi} + \frac{R_1C_1C_2}{R_2} \ll C_1C_2 \quad (6)$$

$$\frac{C_2}{2r_\pi} + \frac{C_2}{R_2} \ll \frac{g_mR_1C_1}{2R_2} \quad (7)$$

$$C_2\left(c_{\mu_1} + \frac{c_\pi}{2}\right) \ll C_1C_2 \quad (8)$$

$$R_1C_1C_2\left(c_{\mu_1} + \frac{c_\pi}{2}\right)\omega^3 \ll \frac{g_mR_1C_1}{2R_2}\omega \quad (9)$$

We will now introduce a 10% deviation norm for the restrictions. A 10% deviation norm means that $a \ll b$ becomes $a < (1/10)b$, where 10% is a practical value based on the tolerances of components within a standard IC process.

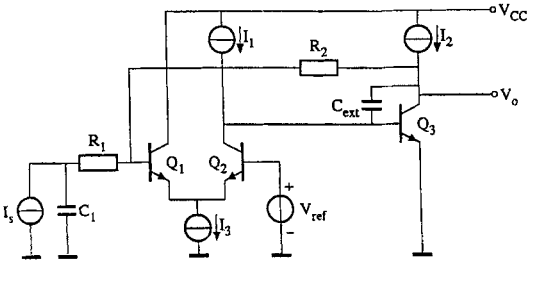

Fig. 2.

Using this norm and the proper substitutions of (3) and (4) in the restrictions, yields a simplification of these restrictions. Accordingly, from (6) and (7) a dominant restriction follows and yields

$$g_m < \frac{R_2 - 10R_1}{5R_1R_2}\beta_F \tag{10}$$

where β_F is the small-signal current gain factor of Q_1 and Q_2. This restriction minimally affects the design freedom. Both (8) and (9) give

$$c_{\mu_1} + \frac{c_\pi}{2} < \frac{1}{10}C_1 \tag{11}$$

if it is kept in mind that (9) must hold in the low-pass frequency band. Some calculation yields that in practice (11) is fulfilled in nearly all cases.

We will now discuss the noise performance of the combination. In low-power applications only the contributions of the base shot noise and the collector shot noise of a transistor are relevant [3]. Further, with the use of transformation techniques, such as described in [2], the mean output noise power can be calculated and yields (see also appendix)

$$\overline{v_{t,o}^2} = \left[4\left(1+\frac{2}{3}\left(\frac{R_1+R_2}{R_1}\right)^2\right)\frac{k^2T^2}{qI_C} + \frac{10}{3}\frac{qR_2^2I_C}{B_F} + \frac{20}{3}kTR_2 + \frac{8}{3}\frac{R_2^2kT}{R_1}\right]B \tag{12}$$

where I_C is the collector bias current and B_F the large-signal current gain factor of transistor Q_1 and Q_2. Equation (12) is derived with the aid of equation (4) and applies to the frequency band 0 to B Hz. As a consequence, the dynamic range can be obtained and equals

$$D_{dB} = 10\log\frac{\hat{I}_{s,\max}^2R_2^2}{2\overline{v_{t,o}^2}} \tag{13}$$

where $\hat{I}_{s,\max}$ is the maximum amplitude of the signal current at the input.

Now, we can obtain design rules for the amplifier/filter combination. As the capacitance of the input sensor C_1 (Derivations show that external enhancement of C_1 results in a decrease of dynamic range), the maximum amplitude of the signal current $\hat{I}_{s,\max}$ and the desired bandwidth B are known, the following parameters can be derived. From equation (4) we obtain the value of R_1. If equation (13) is maximized with respect to R_2, R_2 should be infinite. However, the configuration has a maximally possible amplitude of the output voltage $\hat{V}_{o,\max}$, determined by the supply voltage and a saturation voltage. So we choose

$$R_2 = \frac{\hat{V}_{o,\max}}{\hat{I}_{s,\max}} \tag{14}$$

Now equation (13) can be maximized with respect to I_C. The result is

$$I_C = \frac{kT\sqrt{10B_F(5R_1^2+4R_1R_2+2R_2^2)}}{5qR_1R_2} \tag{15}$$

With (15) we know all the parameters to derive C_2 from equation (3) (where $g_{m1} = g_m/2$). One should verify whether equation (10) is fulfilled, otherwise adjustments have to be made. As stated before, the designer should always check if the positions of the zeros in the loop gain approximately fit the ends of the root locus. If not, increasing of the DC-loop gain will be sufficient in most cases.

4. Design Example

For an evaluation of the operation of the combination, a test design has been realized with discrete components, using transistor arrays. The specifications of this design are a Butterworth characteristic (it is also possible to realize a Bessel characteristic by minor adjustments) with a 6 kHz-bandwidth and a power dissipation as small as possible. The supply voltage is delivered by a single 1.3-V battery. The circuit has to operate down to 1 V (battery voltage at the end of its lifetime; in this worst-case situation, the maximally possible amplitude of the output voltage $\hat{V}_{o,\max}$ of this configuration is restricted to about 100 mV, when using a V_{ref} of 0.85 V (see figure 2)). The employed photodiode has an internal capacitance of 300 pF and a maximum current amplitude of 55.6 nA. This yields: $R_1 = 125$ kΩ, $R_2 = 1.8$ MΩ, $I_C = 1.2$ μA, $C_2 = 31$ pf and $D_{dB} = 63$ db.

For measuring purposes, a 1-MΩ resistor is chosen for the voltage-to-current conversion at the input. In figure 3, the simulated and measured frequency characteristic of the amplitude and the phase of this realisation are shown. We see that a 6.6 kHz bandwidth

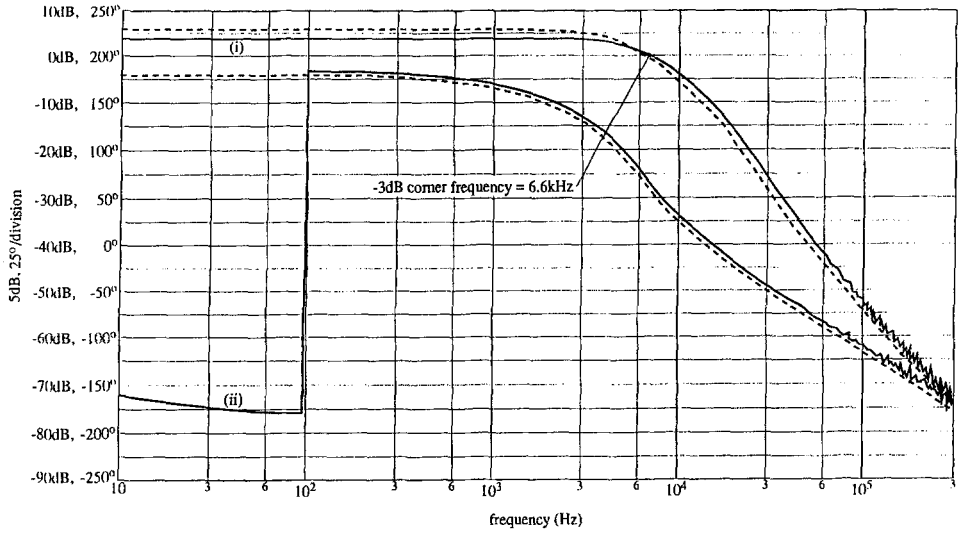

Fig. 3.

is measured and that the measurement results show a very reasonable fit with the simulation results. Further, the simulation results of the test circuit show a good fit with the frequency characteristics as a result of the simplified quadratic equation. In figure 4, the measured noise spectrum at the output (in $V/\sqrt{Hz}$) is depicted. The two peaks appearing at the left side of the figure are a consequence of interference of harmonics of the 50 Hz power frequency. Also in this case, calculated and simulated values show little difference with the measured values.

Finally, it is also feasible to construct design rules, if the basic configuration is a current amplifier instead of a transimpedance amplifier. This has been accomplished by the authors, but for the sake of brevity is not discussed here.

5. Conclusions

Design rules for a circuit which has an inseparable combination of an amplifier and filter characteristic, have been presented. With this circuit it is possible to realize a current-to-voltage conversion with an inherently controllable second-order low-pass filter characteristic. By intentionally using the capacitance of an *already present* input sensor for the filtering, it is possible to have the advantage of a better integratability and less complexity. Moreover, a lower power consumption can be achieved. A discrete realization has been designed to test the circuit. At a worst-case supply voltage of 1 V and a bandwidth of 6 kHz, the circuit shows a 63 dB dynamic range. This is achieved with only a total required integrated capacitance of 31 pF.

6. Appendix: Noise Calculations

In order to find the noise behaviour of the input stage we represent v_1 and i_1 as the total noise voltage and current noise at the input of transistor Q_1, respectively. The same holds for v_2 and i_2 of transistor Q_2 (see figure 5). According to [3], the following spectra hold in low-power circuits:

$$S(v_1) = S(v_2) \approx \frac{2qI_C}{g_m^2} \tag{16}$$

where I_C is the collector current of a transistor of the differential pair and

$$S(i_1) = S(i_2) \approx 2qI_B \tag{17}$$

where I_B is the base current of a transistor of the differential pair. In this case (base of transistor Q_2 grounded), the total noise spectra at the input of the differential pair (see figure 6a) are $S(v) = 2S(v_1)$ and $S(i) = S(i_1)$ [4].

In order to calculate the noise parallel with the signal source, we can use the representation in figure 6a. The feedback resistance R_2 influences the noise performance as if it were in parallel with the input of the

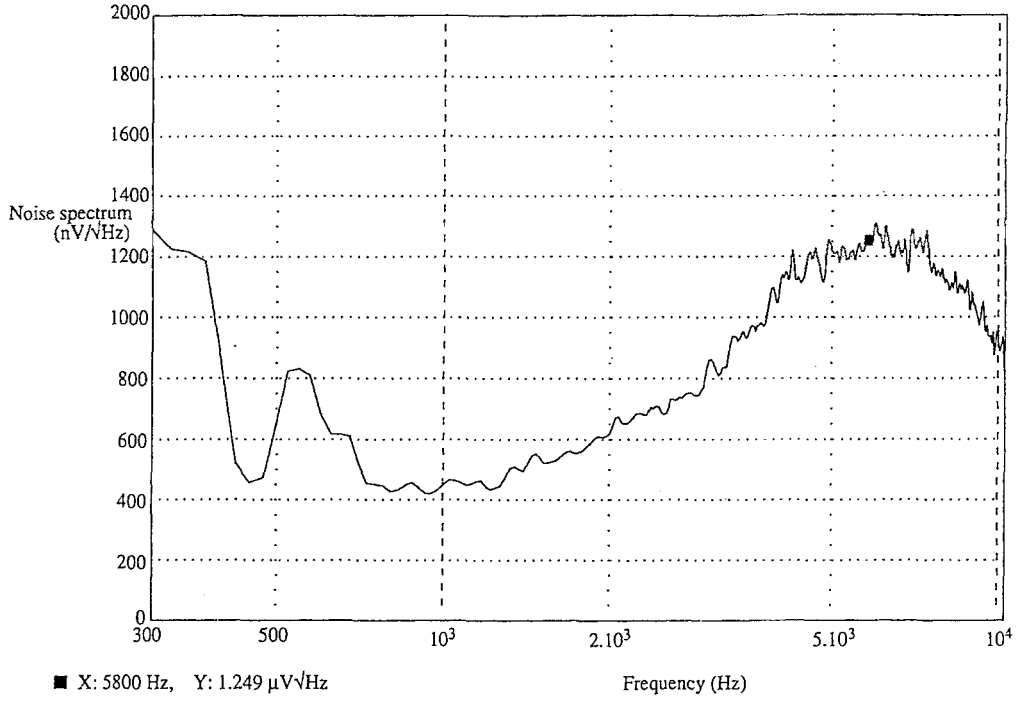

Fig. 4.

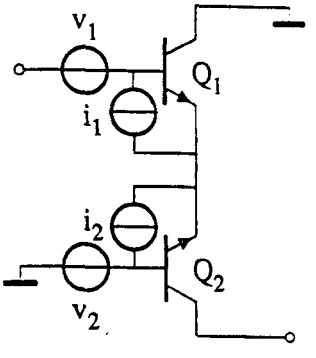

Fig. 5.

"nullor" [2], where the nullor approximation holds for frequencies within the bandwidth. The following spectra hold:

$$S(v_{R_1}) = 4kTR_1 \tag{18}$$

$$S(v_{R_2}) = 4kTR_2 \tag{19}$$

With the aid of the Norton equivalent, figure 6b results, where $i' = i + v_{R2}/R_2$.

If we consider the influence of the voltage source v, the transformations in figure 7 are applicable, using the Blakesley transformation and the Norton equivalent.

If we consider the influence of the current source i'', where $i'' = i' + v/R_2$, the transformations in figure 8 are applicable, using the equivalent of the Blakesley transformation for current sources and using the Thévenin and Norton equivalent.

Using the transformations in figures 6–8, the total noise current parallel with the input signal current source can be calculated:

$$\begin{aligned} i_{t,i} = {} & \left(\frac{1}{R_2} + \frac{R_1}{R_2}\omega C_1 j + \omega C_1 j\right) v \\ & + (1 + R_1\omega C_1 j) i \\ & + \left(\frac{1}{R_2} + \frac{R_1}{R_2}\omega C_1 j\right) v_{R_2} \\ & + j\omega C_1 v_{R_1} \end{aligned} \tag{20}$$

From this equation the noise spectrum $S(i_{t,i})$ can be determined, using the spectra (16)–(19). For frequencies within the bandwidth

$$S(v_{t,o}) = R_2^2 S(i_{t,i}) \tag{21}$$

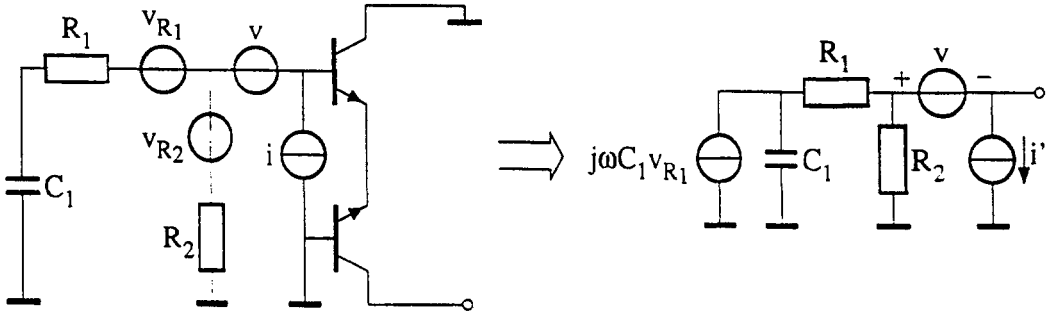

Fig. 6.

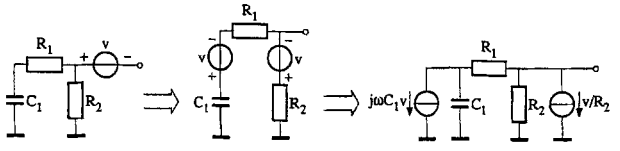

Fig. 7.

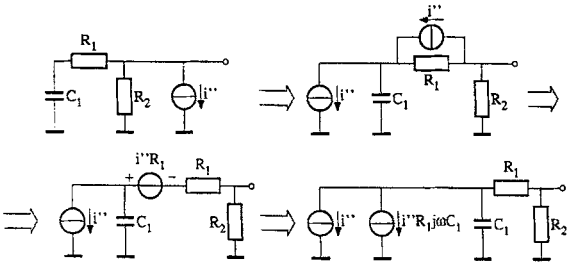

Fig. 8.

holds. This output noise spectrum can be integrated from 0 to B Hz and by using (4) this results in the mean output noise power

$$\overline{v_{t,o}^2} = \left[4\left(1+\frac{2}{3}\left(\frac{R_1+R_2}{R_1}\right)^2\right)\frac{k^2T^2}{qI_C} + \frac{10}{3}\frac{qR_2^2I_C}{B_F} + \frac{20}{3}kTR_2 + \frac{8}{3}\frac{R_2^2kT}{R_1}\right]B \quad (22)$$

where B_F is the large-signal current gain factor of transistor Q_1 and Q_2.

References

1. A. C. van der Woerd, "Analog circuits for a single-chip infrared controlled hearing aid." *Analog integrated Circuits and Signal Processing* 3, pp. 91–103, 1993.
2. E. H. Nordholt, *Design of High-Performance Negative-Feedback Amplifiers.* Elsevier: Amsterdam, 1983.
3. W. A. Serdijn, *The Design ofLow-Voltage Low-Power Analog Integrated Circuits and Their Applications in Hearing Instruments.* Delft University Press: Delft, 1994.
4. A. C. van der Woerd and A. C. Pluygers, "Biasing a differential pair in low-voltage analog circuits: A systematic approach." *Analog Integrated Circuits and Signal Processing* 3, pp. 119–125, 1993.

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1990 to 1992 of a Multi-Window Television project. Since 1992 he has been a full professor at the Electrical Engineering Department of Delft University of Technology, where he heads the Electronics Department. The research activities of his group are accomodated in DIMES: the Delft Institute of Micro Electronics and Submicron technology, where he heads the Circuits and Systems Section.