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Low-Voltage Low-Power Fully-Integratable Automatic Gain Controls

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Abstract. This paper discusses the design of low-voltage low-power fully-integratable automatic gain controls. Four different AGCs are presented, all consisting of three elementary building blocks: a controlled amplifier, a comparator and a voltage follower. Their design is treated separately. As an example, the final section describes an automatic gain control for hearing instruments, realized in a bipolar process.

Keywords: low-voltage, low-power, current-mode, automatic gain controls, battery-operated

1. Introduction

Low-voltage low-power circuit techniques are applied in the area of battery-operated systems. In particular, they are of crucial importance for implantable devices, such as pacemakers, blood flowmeters and auditory stimulators [1], [2], [3], [4], [5], [6], [7]. Also, as more and more complex systems are being integrated on the same chip, area minimization is becoming of primary importance. Typical examples are portable radios, hand-carried radiotelephones, pagers and hearing instruments [8], [9], [10], [11], [12], [13]. As the size of batteries is now becoming the limiting factor, it is not sufficient to reduce the size of bulky components by integrating them; the reduction of the power dissipation is also very important. As a consequence, the key point is to develop, simultaneously, both low-voltage and low-power operating integrated circuits in order to reduce the battery size and chip area.

Automatic gain controls (AGCs) are widely used in communication systems to modify the dynamic range of a signal. They can be found in, e.g., radio receivers and transmitters, audio amplifiers and hearing instruments.

An AGC is a circuit that automatically controls its gain in such a way that variations in the input signal result in smaller variations in the output signal. This control action is usually performed by means of a loop that contains a large time constant (e.g. several tens of milliseconds).

In the past, this large time constant was realized by means of a large (external) capacitor [12], [14]. However, in integrated circuit implementations, external components should be avoided as much as possible.

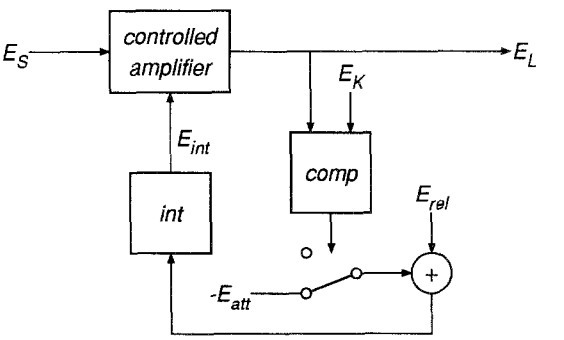

Fig. 1. Block diagram of an automatic gain control ($C.R. = \infty$).

A typical AGC circuit is shown in Figure 1. The output signal E_L is compared with a reference level E_K (the knee level) by a comparator that determines whether the integrating circuit—in practice often nothing more than an RC network—is charged (by $E_{\text{att}} - E_{\text{rel}}$) or discharged (by E_{rel}). The output signal of the integrator, E_{int}, forms the control signal of the controlled amplifier. The operation is as follows: When E_{att} is larger than E_{rel}, the output signal E_L is controlled toward the knee level E_K. Variations in the input signal therefore always result in smaller or equal variations in the output signal. The control action requires some time. This can be described by the expressions *attack time* and *release time*. The attack time is defined as the time needed for the AGC to respond to a sudden 25 dB increase in the input signal until the output signal is

within 2 dB from its final value [15]. Vice versa, the release time is defined as the time required to respond to a sudden 25 dB decrease in the input signal until the output signal is within 2 dB from its final value.

Another important parameter is the *compression ratio* ($C.R.$), defined as the ratio of the variation in the input signal and the variation in the output signal (both in dBs), or

$$C.R. = \frac{\Delta E_{S,\mathrm{dB}}}{\Delta E_{L,\mathrm{dB}}} \tag{1}$$

From this expression it can be seen that for $C.R. > 1$ the operation is that of a compressor and for $C.R. < 1$ of an expander.

The circuit given in Figure 1 realizes an infinite compression ratio. In the following section, realizations with different compression ratios are discussed.

2. AGCs with Finite Compression Ratios

For AGCs with finite compression ratios, the output signal E_L cannot directly be compared with the reference level E_K. We thus need at least one additional amplifier to generate an additional signal out of E_L, E_S or E_K.

2.1. Controlled Amplifiers in Cascade

One way of obtaining a finite compression ratio is to pass the output signal of the AGC, E_L, through another controlled amplifier, which is controlled by the same control signal E_{int}. The output of this second amplifier can then be compared with E_K and thus kept constant. This situation is depicted in Figure 2.

If the controlled amplifier consists of a simple multiplier three equations can be extracted.

$$E'_L = E_K \tag{2}$$

$$E_L = E_S E_{\mathrm{int}} \tag{3}$$

$$E'_L = E_L E_{\mathrm{int}} \tag{4}$$

with E_L the output signal of the AGC, E'_L the output signal of the second controlled amplifier, which is kept equal to E_K. These equations can be rewritten as follows:

$$E'_L = E_S E_{\mathrm{int}}^2 \tag{5}$$

$$E_{\mathrm{int}} = \sqrt{E_K / E_S} \tag{6}$$

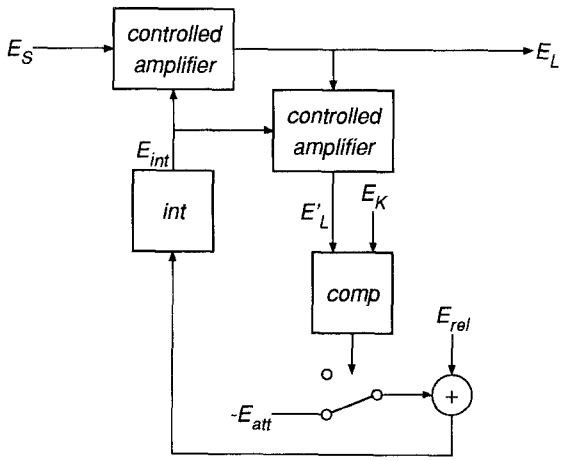

Fig. 2. AGC with $C.R. = 2$ using two controlled amplifiers in cascade.

$$E_L = \sqrt{E_K E_S} \tag{7}$$

For the compression ratio of the AGC we thus can write

$$C.R. = \frac{\Delta E_{S,\mathrm{dB}}}{\Delta E_{L,\mathrm{dB}}} = \frac{20 \log E_S}{20 \log \sqrt{E_K E_S}} = 2 \tag{8}$$

because E_K is a constant level.

Realizing compression ratios other than two is done by using additional controlled amplifiers in cascade. However, because of the greater complexity, this is believed to be of little practical value.

2.2. Differently Controlled Amplifiers

Another possibility is making use of two controlled amplifiers that both have the same input signal E_S, but are controlled by different control signals. This is depicted in Figure 3. The output signal of the integrator, E_{int}, is passed to the controlled amplifier that generates the output signal and to a multiplier that multiplies E_{int} by a constant factor m. This multiplied version of E_{int} is then passed to the second controlled amplifier that generates the signal that is to be compared with E_K.

In order for it to operate properly, the input-output relation of the controlled amplifiers cannot be that of a multiplier for this would result in an infinite compression ratio. We therefore assume that both amplifiers realize an exponentially controlled transfer function, or

$$E_{\mathrm{out}} = E_{\mathrm{in}} \exp E_{\mathrm{control}} \tag{9}$$

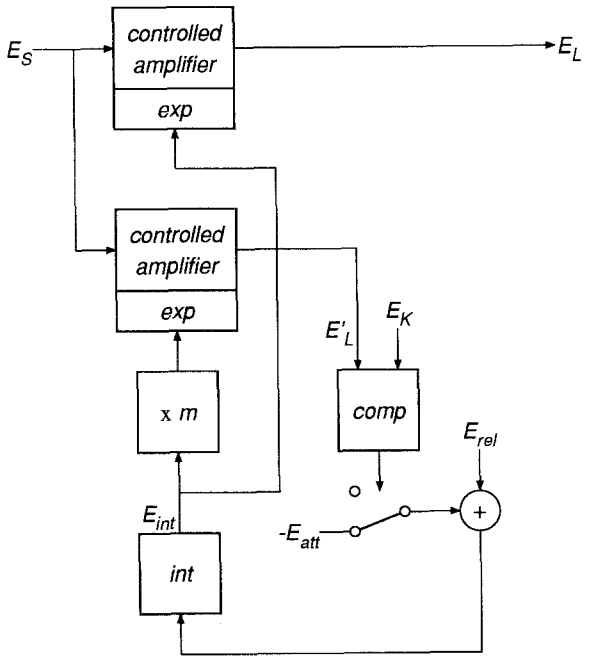

Fig. 3. AGC with $C.R. = \frac{m}{m-1}$ using differently controlled amplifiers.

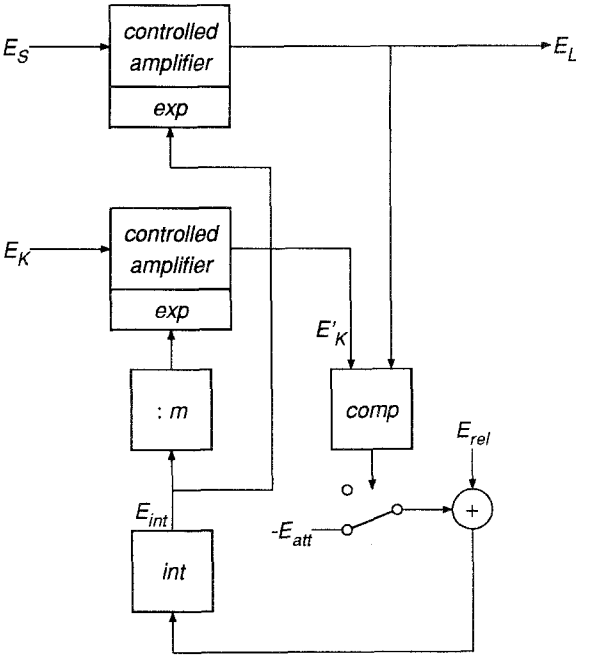

Fig. 4. AGC with $C.R. = 1 - m$ using a controlled knee level.

This transfer function can easily be realized, as is shown in Section 4. For the circuit shown in Figure 3 again three expressions can be found.

$$E'_L = E_K \tag{10}$$

$$E_L = E_S \exp E_{\text{int}} \tag{11}$$

$$E'_L = E_S \exp m E_{\text{int}} \tag{12}$$

These can be rewritten as

$$E'_L = E_K \tag{13}$$

$$E_{\text{int}} = \frac{\ln E_K/E_S}{m} \tag{14}$$

$$E_L = E_S \exp \frac{\ln E_K/E_S}{m} \tag{15}$$

$$= E_S^{1-1/m} E_K^{1/m} \tag{16}$$

For the compression ratio we then find

$$C.R. = \frac{\Delta E_{S,\text{dB}}}{\Delta E_{L,\text{dB}}} = \frac{1}{1-1/m} = \frac{m}{m-1} \tag{17}$$

Using this technique, all compression factors between zero and infinity can be realized. A compression ratio of two, for example, is thus obtained by choosing $m = 2$.

2.3. *Controlled Knee Level*

Finally there is also the possibility of passing the reference level E_K through another controlled amplifier and comparing its output signal to the output signal of the AGC. This is depicted in Figure 4. As E_K contains no signal information (i.e. is a constant level) the demands that are made upon the second controlled amplifier can be much less, thereby reducing the circuit complexity.

Again both amplifiers are exponentially controlled. The output signal of the integrator, E_{int}, is passed to the controlled amplifier that generates the output signal of the AGC and to a divider that divides E_{int} by a constant factor m. This divided version of E_{int} is then passed to the second controlled amplifier that generates the signal that is to be compared with the output signal E_L from the reference level E_K. Again three expressions can be found.

$$E'_K = E_L \tag{18}$$

$$E_L = E_S \exp E_{\text{int}} \tag{19}$$

$$E'_K = E_K \exp E_{\text{int}}/m \tag{20}$$

These can be rewritten as

$$E'_K = E_L \tag{21}$$

$$E_{\text{int}} = m \ln E'_K/E_K \tag{22}$$

$$= m \ln E_L/E_K \tag{23}$$

$$E_L = \frac{E_S^{1/(1-m)}}{E_K^{m/(1-m)}} \tag{24}$$

For the compression ratio this results in

$$C.R. = \frac{\Delta E_{S,\text{dB}}}{\Delta E_{L,\text{dB}}} = \frac{1}{1/(1-m)} = 1 - m \tag{25}$$

A compression ratio of two, for example, is obtained by choosing $m = -1$. Hence, in this situation the divider is an inverter.

3. AGCs in the Current Domain

Low-voltage low-power integrated circuits for preference operate in the current domain [16]. However, we see in the next section that the exponentially controlled amplifiers proposed here are controlled by means of a voltage. As the only integratable integrating element is a capacitor, and its input signal is a current, whereas its output signal is a voltage, the integrator will thus consist of a capacitor followed by a voltage follower. This voltage follower generates a low-impedance version of the voltage across the capacitor to prevent interaction between the capacitor and the controlled amplifier.

4. Controlled Current Amplifiers

Controlled amplifiers can be divided into two different types. First there is the class of controlled amplifiers of which the output signal shows no significant variation, but of which the input signal varies over a wide range. As an example, we mention an AGC with infinite compression; its input signal varies significantly but the output signal is almost unchanged. Second, there are controlled amplifiers of which the input signal shows no significant variation, but of which the output signal varies over a wide range. For example, in an ordinary audio amplifier; the output signal is controlled so that the sound pressure level corresponds to the need of the listener.

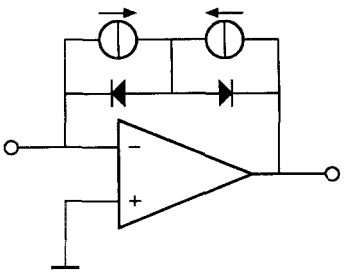

Fig. 5. Transimpedance amplifier with two diodes in anti-series in the feedback path.

A well-known and commonly used controlled amplifier is the *differential pair* of which the transconductance is controlled by varying its tail current. However, as the input signal is limited to some tens of millivolts, while the output signal can be made to vary over a wide range by simply adjusting the tail current, it falls into the category of the second type and therefore it is clearly not the best type of controlled amplifier to use in an AGC. Apart from the above disadvantages, its input signal is a voltage which makes the differential pair less suitable for our purposes.

Another example of a controlled amplifier is given in Figure 5: a transimpedance amplifier of which the feedback network consists of two diodes in anti-series. The transfer function equals the sum of the dynamic resistances of both the diodes, which can be varied by controlling the bias currents through the diodes. Although it is of the first type of controlled amplifiers, the problem with this circuit is that, apart from the bias current, also signal current flows through the diodes, thereby varying the dynamic resistances and distortion occurs. To reduce this distortion, the biasing currents must be much larger than the signal current which degrades the power efficiency. Further, its output signal is a voltage which additionally makes this type of amplifier less suitable for our purposes.

4.1. *Four Fundamental Ways of Controlling the Gain*

A suitable solution is a current amplifier of which the gain equals the ratio of two transconductances: the scaling current amplifier (Figure 6) [16]. As the transconductance of bipolar transistors and CMOS transistors in weak inversion is proportional to their bias current, we can vary the gain by varying the bias

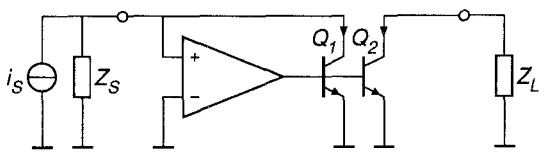

Fig. 6. Controlling the gain of a scaling current amplifier by controlling the ratio of the collector currents of Q_1 and Q_2.

current of either Q_1, $I_{C.Q_1}$, or Q_2, $I_{C.Q_2}$. We can say that the controlled amplifier is of the first type if $I_{C.Q_1}$ is controlled ($I_{C.Q_2}$ remains constant, thus limiting the output current swing) and to the second type if $I_{C.Q_2}$ is controlled ($I_{C.Q_1}$ remains constant, thus limiting the input current swing). A theoretical possibility is that both the bias currents are controlled. However, this option is believed to be of little use in practice.

Another way of controlling the ratio of the transconductances, and thus the gain of the amplifier, is by means of a controlling voltage V_C connected between the emitter of Q_1 and the emitter of Q_2. We now obtain a gain A_i that is proportional to the anti-log of V_C, or

$$\begin{aligned} A_i &= -g_{m.Q_2}/g_{m.Q_1} \\ &= -e^{V_C/V_T} \approx 335 V_C \text{ dB}, \; V_C \text{ in volt} \end{aligned} \tag{26}$$

in which V_T equals the thermal voltage kT/q, approximately 26 mV at 300 K.

The exponential relationship between the gain A_i and the control voltage V_C of the voltage-controlled amplifiers enables us to control the gain over a wide range.

As the controlled current amplifiers are either current- or voltage-controlled and are of either the first or second type, we can distinguish four different kinds:

- a current-controlled type 1 scaling current amplifier,
- a current-controlled type 2 scaling current amplifier,
- a voltage-controlled type 1 scaling current amplifier, and
- a voltage-controlled type 2 scaling current amplifier.

These four are the subject of the next four subsections. Unless there is the possibility of on-chip filtering, the biasing of a circuit is by preference done by setting the common-mode quantities [16]. In order to do so, the signal path has to be symmetrical. As current- or voltage-controlled and type 1 or type 2 has nothing to do with the signal behavior of the amplifier, we assume that the design of the symmetrical signal path has been completed in an earlier stage and start our considerations from here.

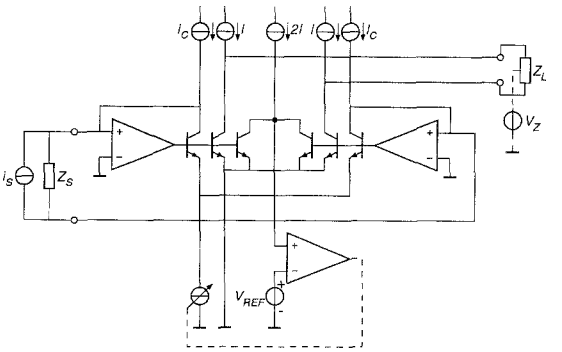

Fig. 7. Current-controlled type 1 symmetrical scaling current amplifier.

It also is tacitly assumed that the source is floating and the load is tied to a certain reference level (e.g. a base-emitter voltage of the following circuit). In other situations, similar solutions can be found.

4.2. *The Current-Controlled Type 1 Symmetrical Scaling Current Amplifier*

The general biasing solution for a current-controlled type 1 symmetrical scaling current amplifier is depicted in Figure 7. The transfer function is controlled by means of two current sources I_C. In order to make the DC collector currents of the output transistors equal to I, a common-mode output is generated by two extra output transistors. The sum of their collector currents is compared with $2I$, thus producing an error signal. The error signal is amplified by the op amp and fed back to both emitters of the input transistors, thereby setting the correct emitter current. As the absolute value of the loop gain of the common-mode loop is much larger than one, the error signal is nullified and the output transistors are biased correctly.

4.3. *The Current-Controlled Type 2 Symmetrical Scaling Current Amplifier*

This situation does not differ much from the preceding one. Only now the transfer function is controlled by varying the current through the *output transistors*. The

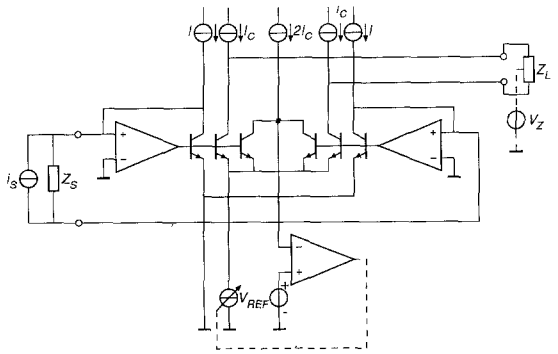

Fig. 8. Current-controlled type 2 symmetrical scaling current amplifier.

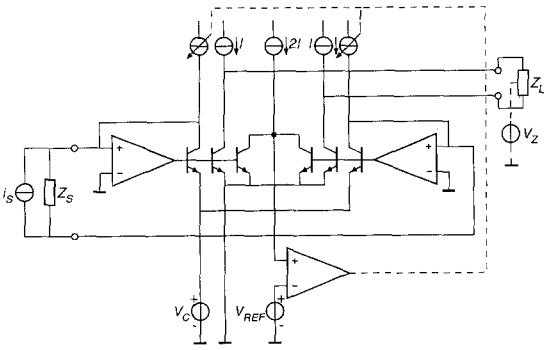

Fig. 9. Voltage-controlled type 1 symmetrical scaling current amplifier.

general solution for a current-controlled type 2 symmetrical scaling current amplifier is depicted in Figure 8. In order to set the output collector currents, again a common-mode output is generated by two extra transistors, their collectors tied together. The common-mode current is compared with $2I_C$, producing an error signal. The error signal is amplified by the op amp and fed back to both emitters of the *output transistors*, thereby setting the correct emitter current. As the absolute value of the loop gain of the common-mode loop is much larger than one, the error signal is nullified and the output transistors are biased correctly.

4.4. *The Voltage-Controlled Type 1 Symmetrical Scaling Current Amplifier*

The transfer function of this type of amplifier is controlled by the control voltage V_C (see Figure 9). Again a common-mode replica of the common-mode collector currents through the output transistors is compared with $2I$, producing an error signal. The error signal is amplified by the op amp and controls the collector current of the input stages.

An example of the voltage-controlled type 1 symmetrical scaling current amplifier is described in [17]. This circuit is part of a hearing instrument and serves to attenuate the signal coming from the preamplifier [18], that can vary between 40 nA and 10 μA (peak value), and drive a highpass filter [19] at maximal 25 nA.

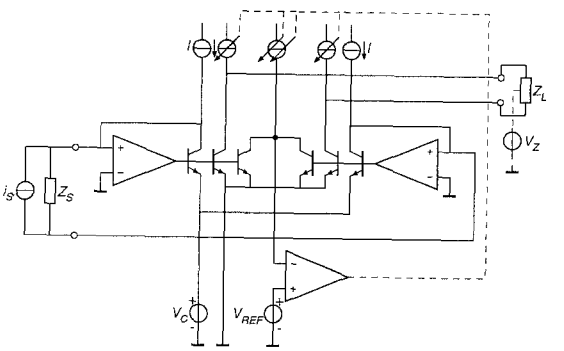

Fig. 10. Voltage-controlled type 2 symmetrical scaling current amplifier.

4.5. *The Voltage-Controlled Type 2 Symmetrical Scaling Current Amplifier*

Finally, the voltage-controlled type 2 symmetrical scaling current amplifier, see Figure 10. V_C controls the gain. The common-mode loop controls the collector currents of the output transistors (including the common-mode output transistors) in such a way that they match the collector currents of the input stages.

Two examples of the voltage-controlled type 2 symmetrical scaling current amplifier can be found in [20] and [21]. The first circuit (though not strictly symmetrical) has been designed for the same hearing instrument and loads a highpass filter [19] at maximal 25 nA and drives the power amplifier. Its gain can be controlled from 0 to 60 dB. The second circuit, a controllable preamplifier, was originally designed for a different hearing instrument using the conventional electret microphone with built-in JFET [22]. It adapts

input signals varying between 120 nA and 30 μA (peak value) to the maximal filter input level of 1 μA.

5. Comparators

The comparator is the circuit that compares the output current of the controlled amplifier with the reference level I_K by means of a highly non-linear input-output relation. Thus the comparator can be viewed as a one-bit A/D converter. Its response to a signal level higher than the reference level is a fixed output level, representing the '0' or the '1' state. Its response to a signal lower than the reference level is another fixed output level, representing the complementary state. The gain when the input equals the reference level ideally is infinite. However, it is no use making the gain much larger than the ratio of the desired output swing and the smallest input swing. In practice, there is also some common-mode-to-differential-mode conversion in the controlled amplifier, so that for large values of the comparator gain the common-mode control loop might become instable.

For a comparator which has a current-current input-output relation we can choose either a cascade connection of a non-linear one-port and a linear two-port, or an amplifier with a saturating input-output relation.

5.1. *Cascade of a Non-linear One-Port and a Linear Two-Port*

Examples of (bipolar) non-linear one-ports are diodes and pinch resistors. An example of a (current) comparator consisting of a cascade of a non-linear one-port and a linear two-port is given in Figure 11. Both the output current of the controlled amplifier and the reference current can be supplied, with opposite signs, to the same input, and thus subtracted from eachother. If the result is positive, diode D_1 will conduct. The resulting anode-cathode voltage will vary only slightly with respect to the current and thus represent one state of the comparator. If the result is negative, diode D_2 will conduct, resulting in a complementary voltage, representing the complementary state. The resistor R transforms the voltage into a current that is sensed by the (low-impedance input of the) next circuit. Although this is a relatively simple comparator, it is not suited to use in low-power integrated circuits. If, for example, the output current of the comparator is to be as small as 25 nA, and the diode voltages are about .5 V, R must

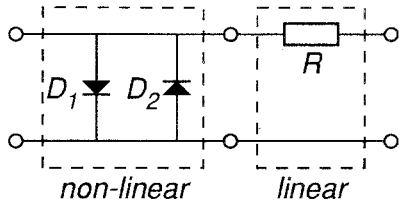

Fig. 11. Example of a comparator consisting of a cascade connection of a non-linear one-port and a linear two-port.

equal 20 MΩ. This value is not easily realized in an integrated circuit.

5.2. *Amplifiers with a Saturated Input-Output Relation*

It is not difficult to design an amplifier with a saturated input-output relation. Every practical amplifier will come into saturation if its input signal exceeds a certain level. Three examples are given in Figure 12. During saturation, often one or more transistors will be pinched off or be in saturation. In negative-feedback amplifiers, this might introduce extra dominant poles in the feedback loop, giving rise to instability, or lead to latch-up (see e.g. [23]). The designer must be aware of this and try to avoid both instabily and latch up under all circumstances. Often good results can be obtained from simple circuitry.

6. Voltage Followers

The last stage in the design of low-voltage low-power automatic gain controls is the design of the voltage follower. The voltage follower forms a buffer between the capacitance C and the controlled amplifier. Since the input current of a field effect transistor (JFET or MOST) is far below the other currents that charge and discharge the integrating capacitor, these devices are very well suited for this task. When using bipolar transistors this can only be achieved by using negative-feedback techniques. The basic voltage-follower configuration and three possible implementations, with either one, two or three transistors, are given in Figure 13. Although the output voltage differs a base-emitter voltage from the input voltage, this is no problem here; the voltage follower is part of a loop; the effect of the base-emitter voltage will be nullified.

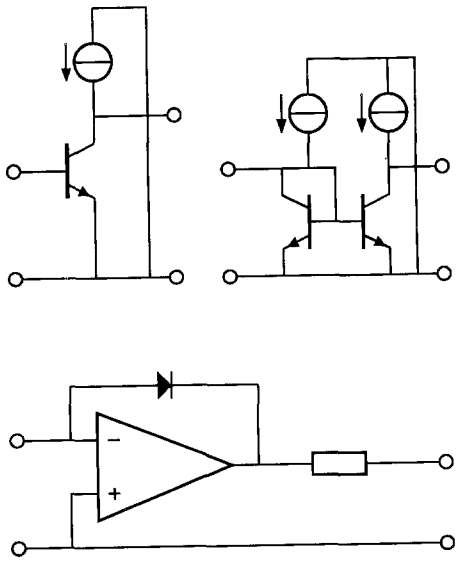

Fig. 12. Three possible implementations of amplifiers with a saturated input-output relation.

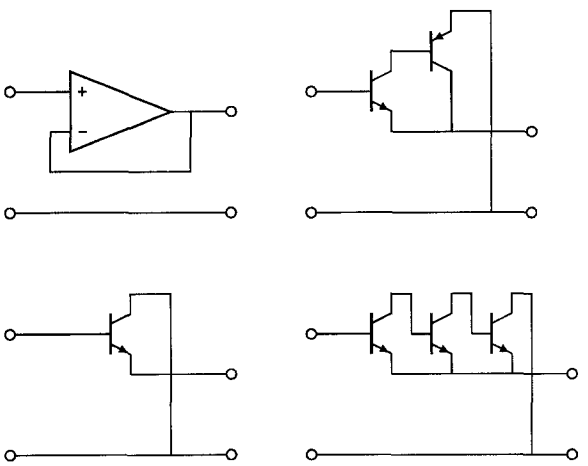

Fig. 13. Basic voltage-follower configuration and three possible implementations.

An example of a three-transistor voltage follower can be found in [17].

7. An Example: An Automatic Gain Control for Hearing Instruments

In this section, the design and realization of a low-voltage low-power fully-integratable automatic gain control for hearing instruments is presented.

Apart from pitch, loudness and timbre, information in the world of sound is characterized also by more or less sudden temporary changes. These variations and changes often do not fall within the dynamic range of those with a hearing impairment: certain parts of the information are not perceived and/or the pain limit is frequently exceeded. In this situation, an automatic gain control can offer certain improvement of the (speech) intelligibility [24], [25]. It must be noted that AGCs are only technically approximate solutions to the dynamic range problems of the hearing impaired. This also explains why optimal, generally applicable values for the AGC characteristics are not easily found.

In practice, two kinds of AGCs are found [26]: an AGC-I and an AGC-O. The AGC-I obtains its control signal from a signal in front of the volume control. Thus, the control action depends on the sound pressure level at the input of the hearing instrument. The control signal of the AGC-O is derived from the signal behind the volume control. The control action then depends on the sound pressure level that is offered to the ear.

The AGCs differ from each other insofar as that the control range of the AGC-I is always larger (for example 60 dB) while for the AGC-O often 20 dB is enough. The compression ratio often is also different: e.g. between 1.5 and 10 for the AGC-I and infinite for the AGC-O.

The circuit that is described here is an AGC-O with an infinite compression ratio, of which the block diagram is shown in Figure 1. Its *current-domain* realization is given in Figure 14. Apart from the integrator signal E_{int} all signals are represented by currents. The AGC amplifier obtains its input signal from a controllable attenuator [17] and drives a highpass filter [19]. The nominal signal level at both input and output amounts to 25 nA (peak value). The purpose of the AGC is to attenuate larger input signals to avoid clipping and hearing damage. The attack time and the release time must be < 5 ms and 50 ms, respectively.

To here the design has been discussed at system level. We now take a closer look at the design of its components: the controlled amplifier, the comparator (including the switch and current source I_{att}) and the voltage follower.

7.1. Design of the Controlled Amplifier

From the considerations presented in Section 4, it should be clear that the best choice of amplifier is a

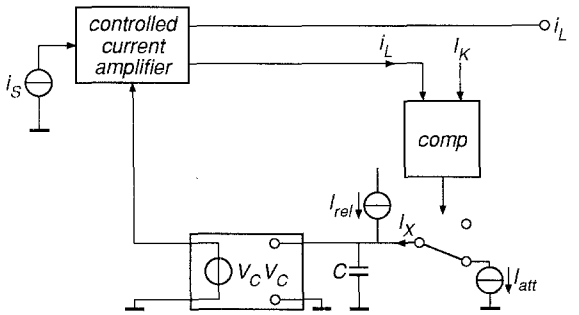

Fig. 14. Block diagram of an AGC-O operating in the current domain.

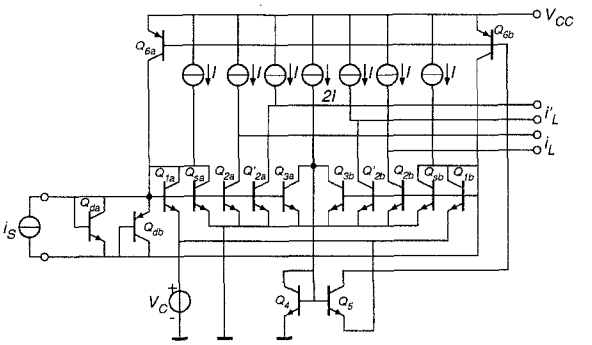

Fig. 15. The voltage-controlled type 1 symmetrical current mirror.

type 1 symmetrical scaling current amplifier. From the two variants, we choose the voltage-controlled one as this gives a control action in dBs, which is perceptibly the most comfortable. A possible implementation of a voltage-controlled symmetrical scaling current amplifier is given in Figure 15. As the absolute value of the (differential) loop gain is always larger than $B_F/4$, there is no need for additional loop gain; the op amps thus can be replaced by short circuits. We call this a voltage-controlled type 1 symmetrical current mirror. Transistors Q_{1a} and Q_{1b} are the input transistors. Q_{2a} and Q_{2b} deliver the output current i_L. Q'_{2a} and Q'_{2b} are the output transistors for i'_L. The common-mode loop is formed by Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a} and Q_{6b}. The collector currents of Q_{3a} and Q_{3b}, which equal the collector currents of Q_{2a} and Q_{2b}, are added and compared with a current $2I$. The error signal controls via Q_4, Q_5, Q_{6a} and Q_{6b} the collector currents of Q_{1a} and Q_{1b}. Because the gain in this loop, the common-mode loop gain, equals the current gain factor B_F of Q_{6a} and Q_{6b}, which is much larger than one, the error signal is nullified and the symmetrical current mirror is biased correctly. Q_{sa} and Q_{sb} limit the maximum gain of the amplifier to one. Q_{da} and Q_{db} shunt the input and prevent the amplifier from saturating.

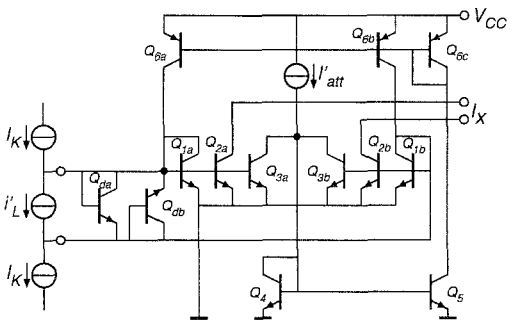

Fig. 16. A type 1 symmetrical current mirror used as a comparator. The common-mode loop gain equals 2 to prevent instability.

7.2. *Design of the Comparator*

The comparator is the subcircuit that decides whether the output current i'_L of the controlled amplifier is larger or smaller than the reference level I_K. For this purpose we can again use a symmetrical current mirror now acting as an amplifier with a saturated input-output relation. Its implementation is given in Figure 16. Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a}, Q_{6b} and Q_{6c} form the common-mode biasing circuitry. In this case, the common-mode loop gain is kept sufficiently small (i.e. equals 2) to prevent instability in the comparator. The output current I_X therefore switches between 0 and $\frac{2}{3}I$. The two diode-connected transistors Q_{da} and Q_{db} prevent the output transistors Q_{2a} and Q_{2b} from saturating; the comparator switches faster.

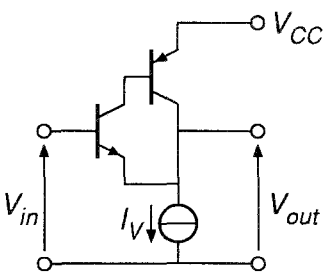

Fig. 17. The two-transistor voltage follower.

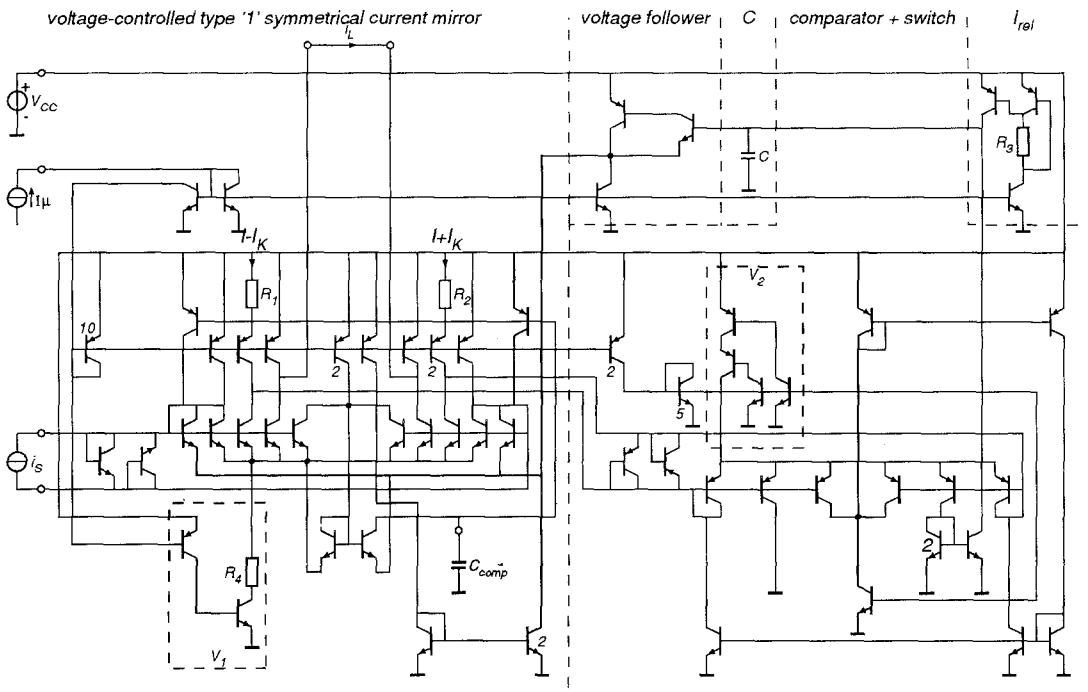

Fig. 18. The total automatic gain control. Instability may be counteracted by C_{comp}.

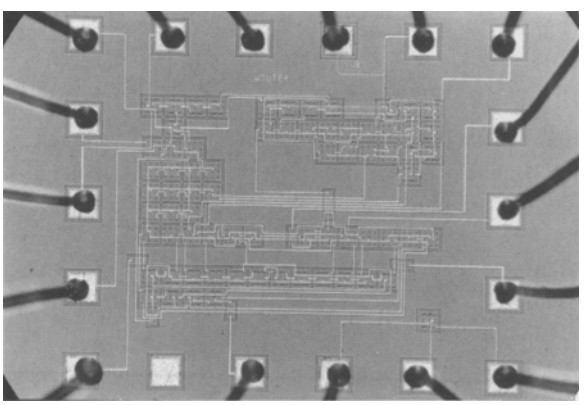

Fig. 19. Photograph of the integrated circuit.

7.3. *Design of the Voltage Follower*

The chosen voltage follower is depicted in Figure 17. The input (offset) current equals $I_V/B_{\text{F,PNP}}B_{\text{F,NPN}}$ and must lie well below the release current I_{rel}. Its influence will then be small.

7.4. *Overall Design*

Now that all the different parts of the AGC have been designed at circuit level, they can be linked together and we take a look at the numerical values and the remaining bias circuitry.

As the output signal is to be maximally 25 nA (peak value), the reference current I_K equals 25 nA. The current sources I as depicted in Figure 15 have been chosen well above this 25 nA and equal 100 nA. The values of I_{att} and I_{rel} can be derived from the attack time and the release time. Some calculation yields

$$I_{\text{att}} = \frac{5.2V_T C}{t_{\text{att}}} + I_{\text{rel}} \tag{27}$$

and

$$I_{\text{rel}} = \frac{2.6V_T C}{t_{\text{rel}}} \tag{28}$$

For I'_{att} (Figure 16) it follows

$$I'_{\text{att}} = \frac{3}{2}I_{\text{att}} = \frac{7.8V_T C}{t_{\text{att}}} + \frac{3}{2}I_{\text{rel}} \tag{29}$$

With t_{att}, t_{rel} and C equal to 4 ms, 50 ms and 400 pF, respectively, this results in 20 nA and 540 pA for I'_{att}

Table 1. Measurement results of the AGC.

Parameter	Value	Unit
Compression range	38	dB
Attack time, i_s=1 μA_p, 1 kHz	4.2	ms
Release time, i_s=10 nA_p, 1 kHz	58	ms
Total harmonic distortion, G=1, 1 kHz	<0.3	%
Dynamic Range, G=1, B=10 kHz, THD=5%	62	dB
Bandwidth	>100	kHz
Min. supply voltage	1	V
Supply current, G=1	4	μA

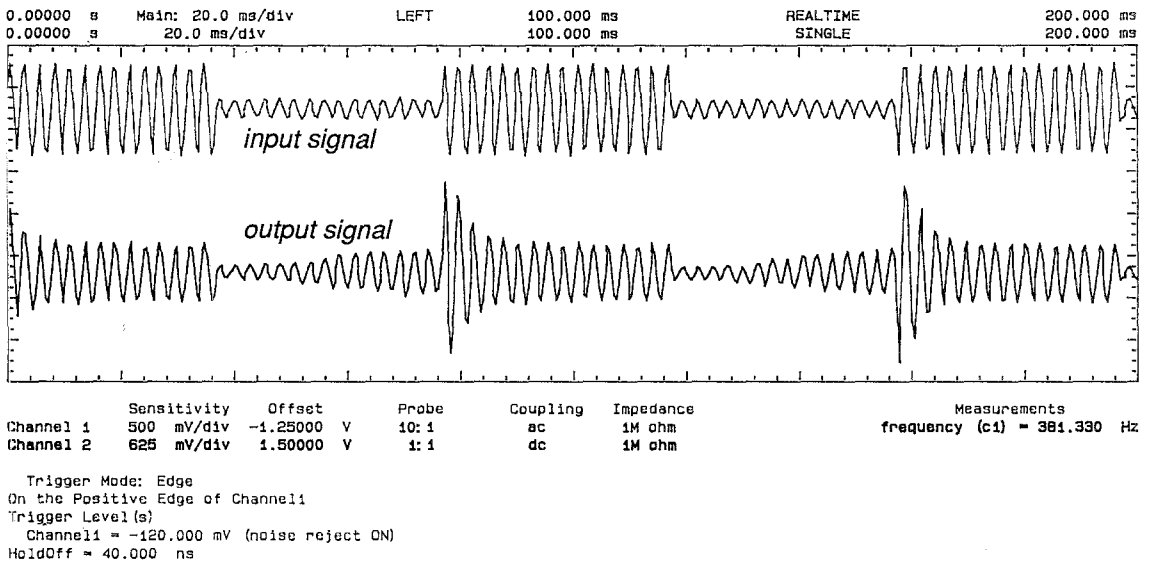

Fig. 20. Response of the AGC to a typical input (test) signal.

and I_{rel}. The current source I_V (Figure 17) supplies the current of the PNP transistor in the voltage follower and is chosen to be equal to 1 μA. All these currents can be derived by means of current mirrors with multiple outputs and convenient scaling factors. The scaling factor can be obtained by choosing either a proper emitter area ratio or by means of resistors. The latter solution yields either a *Widlar mirror* or a *gm-compensated mirror* [27].

The total circuit diagram of the AGC is depicted in Figure 18. The transistor polarities in the comparator have been changed for biasing purposes. Two voltage sources (V_1 and V_2) have been added to prevent the current sources I_V and I_K from saturating. V_1 has been realized by means of a saturating NPN transistor and a resistor. V_2 contains two saturating PNP transistors in series. Thus, their voltages are well above the saturation voltages of I_V and I_K. To avoid (common-mode) instability, an integratable capacitance C_{comp} can be added.

7.5. *Experiment Results*

The active circuitry of the circuit shown in Figure 18 has been integrated in the DIMES01 process [28], fabricated at the Delft Institute of Microelectronics and Submicron Technology. Figure 19 shows a photomicrograph of the chip. Experiments proved the correct operation of the AGC. Figure 20 shows the response of the AGC to a typical input (test) signal. Table 1 gives

the measurement results. No instability occurred. The relatively large value of the release time is caused by the base current of the first stage of the voltage follower. However, this did not pose a problem in our application.

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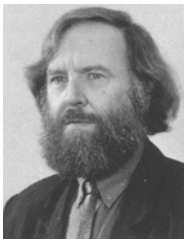

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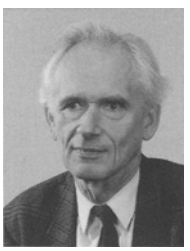

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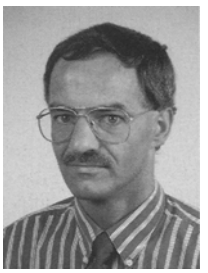

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