

A Novel Microphone Preamplifier for Use in Hearing Aids

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Abstract. A novel design for a microphone preamplifier for application in hearing aids is presented. The amplifier operates at a supply voltage of 1–1.3 V, the current drain is 70 μA . The maximum sound level allowed is more than 105 dB SPL, with a typical noise level of 28 dB SPL. Instead of the usual voltage sensing, current sensing of the microphone is used. The amplifier consists of a fully balanced charge-to-current amplifier with no external components required. A semicustom version of the design has been integrated in a standard BIMOS process.

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1. Introduction

Current hearing aids use an electret design for the microphone [1, 2]. Electret microphones represent a capacitive source for the preamplifier. Due to the low frequencies involved and the low value of the source capacitance of typically 5 pF, the amplifier must show a very low noise current in order to realize an acceptable signal-to-noise ratio. In traditional designs, a junction FET circuited as a source follower is combined with the electret microphone to realize this low noise current.

Due to the gate leakage current of the JFET and the relatively low value of the bias resistor, the noise is still at a level of typically 27 dB SPL [3]. This means that the total amount of noise is equivalent to a speech level of 27 dB above the threshold of audibility. Improvement of the signal-to-noise ratio with a JFET is difficult because the gate leakage current imposes an upper limit to the value of the bias resistor. To lower the noise current of the preamplifier, MOSFETs which show a negligible gate leakage current can be used. Until now, their use has been restricted because little or no BIMOS processes were available. Also the threshold voltage of typical devices is too high for application in circuits operating at 1–1.3 V.

Furthermore, due to the low value of the PSRR of the source follower, an extra voltage source is needed to prevent feedback through the power supply. This is especially important when a class B output stage is used. Therefore, we have to look for other configurations for the preamplifier. Preferably the amplifier must be fully integrated. Another requirement concerns the nature of the output signal. Novel designs of correc-

tion filters, controlled amplifiers, etc., commonly operate at current level. As a consequence, voltage swing and, therefore, distortion caused by modulation of parasitic capacitances is restricted as much as possible. Therefore, the output of the preamplifier must operate at current level too.

This paper presents a balanced charge-to-current amplifier operating at supply voltages of 1–1.3 V. It uses direct current sensing at the input and indirect sensing at the output. In Section 2, we will choose the amplifier configuration most suited for use at low supply voltages. In Section 3, the noise performance is discussed. Since no large capacitors are acceptable common mode (CM) feedback is used for the biasing, which is discussed in Section 4. In Section 5, the complete design is discussed and some measuring results of a semicustom version of the amplifier are presented.

2. Amplifier Configuration

The electret microphone can be represented by the equivalent circuit of figure 1. It consists of a capacitor which is charged by a permanent electric field. This

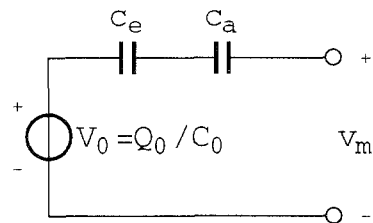


Fig. 1. Circuit representation of an electret microphone.

field is generated by the electret element inside the microphone. This is represented by the constant voltage V_0 . One of the capacitor plates acts as a diaphragm which deforms as a function of the air pressure difference across it. The capacitance of the microphone can be modeled by a constant capacitance formed by the electret capacitance c_e in series with a variable part formed by the air capacitance c_a . An output voltage $v_m(t)$ is generated by the variation of the capacitance c_a as a function of air pressure variations. This voltage equals

$$v_m(t) = \frac{V_0}{C_m} \cdot dc \quad (1)$$

where dc equals the capacitance variations due to air pressure variations. The total microphone capacitance C_m (the series connection of c_e and c_a) is $C_0 + dc$, which depends on the air pressure variations. For a more comprehensive discussion of the principles of electret based sensors see [4].

For the signal quantity of the microphone, we can take both the open-voltage and the short-circuit current. The linearity of the transfer of the microphone is not essentially different in both cases. In this design we have used the short-circuit current of the microphone. The amplifier delivers a current at the output. Furthermore, a balanced configuration is preferred. Hence, we can use CM feedback for the biasing. This yields a balanced charge-to-current amplifier, the basic configuration is shown in figure 2.

Although it is possible to choose a balanced transadmittance amplifier which uses the microphone volt-

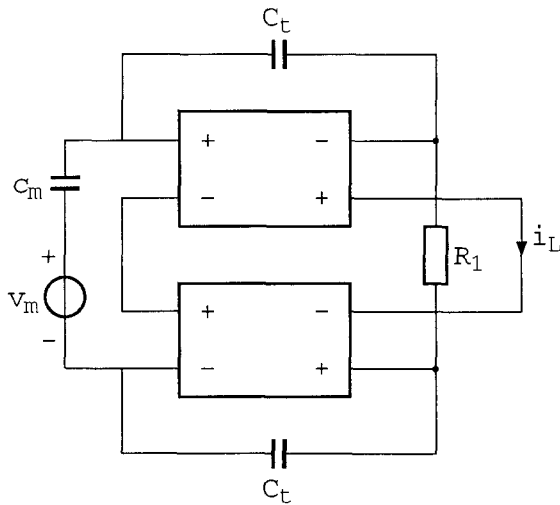


Fig. 2. Basic configuration of the microphone preamplifier.

age as the signal quantity, this choice has a main drawback. For practical reasons, one pin of the nullor is preferably grounded. This is only feasible if current sensing is employed; the transadmittance amplifier needs two fully floating nullors. Therefore, the transadmittance amplifier is rejected.

In the ideal case there is no voltage across the input terminals of the active part of the amplifier and the input current is also zero. For the output current i_L , one easily finds

$$i_L = \frac{2c_m}{R_1 C_t} \left(\frac{1 + j\omega R_1 C_t}{2} \right) v_m \quad (2)$$

The “small-signal” capacitance c_m is the microphone capacitance at zero sound pressure which is equal to C_0 . As we can see, the transfer contains a zero. In practice ($1 \text{ pF} < C_t < 5 \text{ pF}$, $10 \text{ k}\Omega < R_1 < 50 \text{ k}\Omega$) this zero is well above 50 kHz, so the influence will not be noticeable.

3. Noise Performance

In order to achieve an acceptable signal-to-noise ratio, the amplifier must show a very low noise current. Therefore, we take a MOSFET for the input transistor. First we will look at the noise performance of the input stage and the feedback network. We will assume that the noise contribution from other stages of the amplifier and of the bias circuit can be kept sufficiently low. Because of the indirect current sensing used at the output the noise contribution of the output must be taken into account too. We will deal with the noise performance of the output stage separately.

The equivalent input noise resistance of a single MOSFET is given by

$$R_{gn} = c/g_m \quad (3)$$

If the transistor operates in strong inversion, then [5]

$$R_{gn} = 2/3g_m \quad (4)$$

In the weak inversion region it is shown in [6] that for good quality devices the equivalent noise resistance is given by $R_{gn} = 1/g_m$. For transistors operating in moderate inversion, measurements have shown that $R_{gn} \approx 1/g_m$ [7]. Therefore, we will assume that in all operating regions $c = 1$.

The special density of the equivalent input noise voltage can now be written as

$$S(u_{neq}) = S(u_{n,eq}) + S(u_{n,eq}) \quad (5)$$

where

$$S(u_{n,eq}) = \frac{4kT}{g_m/2} \left(1 + \frac{f_i}{f^a} \right) \frac{(c_m + (C_t + c_{iss})/2)^2}{c_m^2} \quad (6)$$

where the term f_i/f^a gives the contribution of $1/f$ noise (f_i is the frequency where the contribution of the white noise is equal to the contribution of the $1/f$ noise) and

$$S(u_{n,eq}) = kTR_1 \frac{C_t^2}{c_m^2} + \frac{gI_g}{\omega^2 c_m^2} \quad (7)$$

where

$$c_{iss} = c_{gs} + c_{gd} \quad (8)$$

The first term of (5) gives the contribution of the noise of the drain current. The second terms gives the contribution of the feedback resistor R_1 and of the gate leakage current and possibly other leakage currents from the bias circuit. Although p -channel MOSFETs generate less $1/f$ noise n -channel MOSFETs are used because the threshold voltage of the p -channel MOSFETs of the employed BICMOS process was too high for our application.

As we can see from (6) and (7), a small value of the feedback capacitor C_t gives the best noise performance. However, if we take a value for C_t that is too small, the maximum output signal is limited by the voltage swing across R_1 , which equals

$$V_{R_1} = \frac{2c_m}{C_t} v_m \quad (9)$$

The maximum output voltage of the microphone is about 50 mV. With $c_m = 5$ pF and $C_t = 4$ pF this means that the maximum peak voltage swing across R_1 is about 180 mV. This is acceptable in this design. With this value for C_t , the noise performance is only slightly deteriorated. Furthermore, the leakage currents at the input must be kept very small. The contribution to the equivalent input noise voltage is given by the second term of (7). If we want to keep the contribution below 10 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, the leakage current must be less than 0.6 pA. This corresponds to a noise resistance of 85 G Ω . This means that the use of resistors for the biasing of the input transistor is not feasible. We will deal with the biasing of the input transistors in Section 4.

Because of the indirect current sensing at the output, the noise contribution of the output stage cannot be neglected. The schematic diagram of one output stage is depicted in figure 3. The noise sources u_n and i_n represent the equivalent input noise voltage and current of the output transistors. If the transfer parameters γ

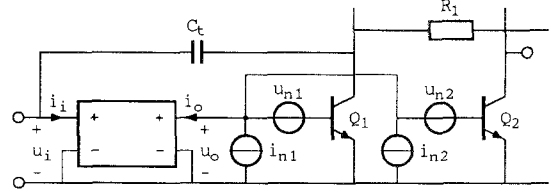


Fig. 3. Schematic diagram of one output stage with noise sources.

and α of the first stages of the amplifier, defined as (see figure 3)

$$\gamma = \left. \frac{i_o}{u_i} \right|_{u_o=0}, \quad \alpha = \left. \frac{i_o}{i_i} \right|_{u_o=0} \quad (10)$$

are sufficiently large, the contribution of the noise sources i_{n1} and i_{n2} can be neglected. The noise sources u_{n1} and u_{n2} however cannot be neglected. For the low-frequency value of the transfer $A_{r\infty}$, we can write (see equation (2) and [8])

$$A_{r\infty f} = \frac{2c_m g_{m2}}{R_1 C_t g_{m1}} \quad (11)$$

The extra term g_{m2}/g_{m1} is caused by the indirect current sensing at the output.

For low frequencies, the equivalent input noise voltage of the output stage (balanced configuration) equals

$$S(u_{neq}) = \frac{2kTC_t^2 R_1^2 g_{m1}^2}{4c_m^2} \left(\frac{r_{b1}}{2} + \frac{1}{2g_{m1}} + \frac{r_{b2}}{2} + \frac{1}{2g_{m2}} \right) \quad (12)$$

The spectral density of the equivalent input noise voltage is halved with respect to the unbalanced configuration. From (12) it follows that it is possible to exchange noise performance with power efficiency. If we have chosen a value for the maximum input voltage and a bias current for the output transistor, it is possible to vary the scaling factor n of the transistors in the output stage which is given by

$$n = g_{m2}/g_{m1} \quad (13)$$

It can be shown that the noise contribution of the output stage is minimized for $n = 1$.

4. The Biasing of the Amplifier

Since the amplifier must be fully integrated we cannot use coupling capacitors in the bias circuitry. Furthermore, the use of voltage sources must be prevented because they are difficult to realize at low supply voltages. Therefore, CM feedback is used for the biasing of the

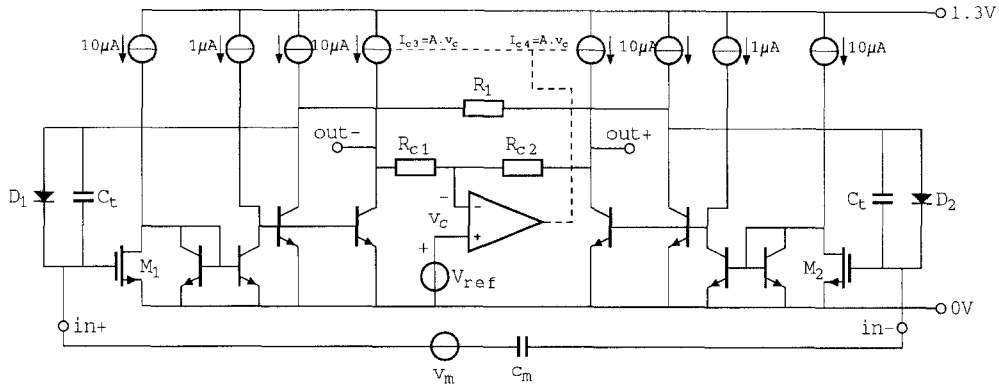


Fig. 4. Schematic diagram with ideal bias circuitry.

preamplifier. The schematic diagram of the amplifier with ideal bias circuitry is shown in figure 4. The signal path contains no PNP transistors.

Both nullors consist of three stages. The first stage is an n -channel MOSFET with dimensions $W/L = 800 \mu/3 \mu$, to achieve high transconductance and to reduce the $1/f$ noise. This stage operates in weak inversion. The bias current is $9 \mu\text{A}$. The second stage is a current mirror. This stage has been added to realize an extra phase shift of 180° without adding a dominant pole to the loop gain. The noise contribution of this stage has been kept low by choosing a low bias current. The output stage consists of two identical NPN transistors for indirect current sensing at the output. Each transistor of the output stage operates at a current of $10 \mu\text{A}$.

The amplifier contains two CM loops for the biasing. The first one is for the biasing of the input transistors and is realized with the two diodes D_1 and D_2 . The current through these diodes is determined by the MOSFETs and is equal to the leakage currents from the MOSFETs and the gate protection circuitry. Hence, the noise performance is influenced as little as possible. The small-signal resistance of the diodes is very high so that the transfer of the amplifier is not influenced.

The second CM loop determines the dc voltage at the output terminals. The two controlled current sources I_{c3} and I_{c4} are controlled by the CM voltage at the output terminals, which is determined by the reference voltage V_{ref} . This voltage source can be realized by the base-emitter voltage of a bipolar transistor. Two resistors R_{c1} and R_{c2} are added in order not to influence the output current of the amplifier.

5. Overall Design

The overall circuit of the amplifier with bias circuitry is shown in figure 5. The scaling of the transistors of the current mirrors is indicated between brackets. The CM loop at the output is realized with transistors Q_{c1}, \dots, Q_{c6} . The reference voltage V_{ref} equals the base emitter voltage of Q_{c1} . The DM loop gain has two dominant poles determined by the last stage (Q_1, \dots, Q_4) and by the feedback elements, the source capacitance and the input stage. Because the pole of the second stage cannot be neglected, some form of compensation must be added. It is possible to add a phantom zero by putting a resistor in series with the microphone, but this would deteriorate the noise performance. Therefore, two capacitors C_{c1} and C_{c2} have been added to enlarge the pole of the last stage. Another advantage is that the stability of the CM loop can also be ensured by these capacitors.

The amplifier must be able to handle a sound level of at least 105 dB SPL, which is equivalent to an output voltage of the microphone of 50 mV. If we choose the maximum peak output current to be $10 \mu\text{A}$ (the output transistors are biased at a current of $10 \mu\text{A}$), the transfer of the amplifier is found to be $A_t = 0.135 \text{ mA/V}$. With $C_t = 4 \text{ pF}$ and $c_m = 5 \text{ pF}$, it follows from (2) that $R_1 = 18.5 \text{ k}\Omega$. From (5) and (7), it follows that the contribution to the equivalent input noise spectrum equals

$$S(U_{eqR_1}) = 4kT \cdot 2960 \quad (14)$$

which is acceptable. The maximum input level the amplifier can handle can be raised but this would deteriorate the noise performance.

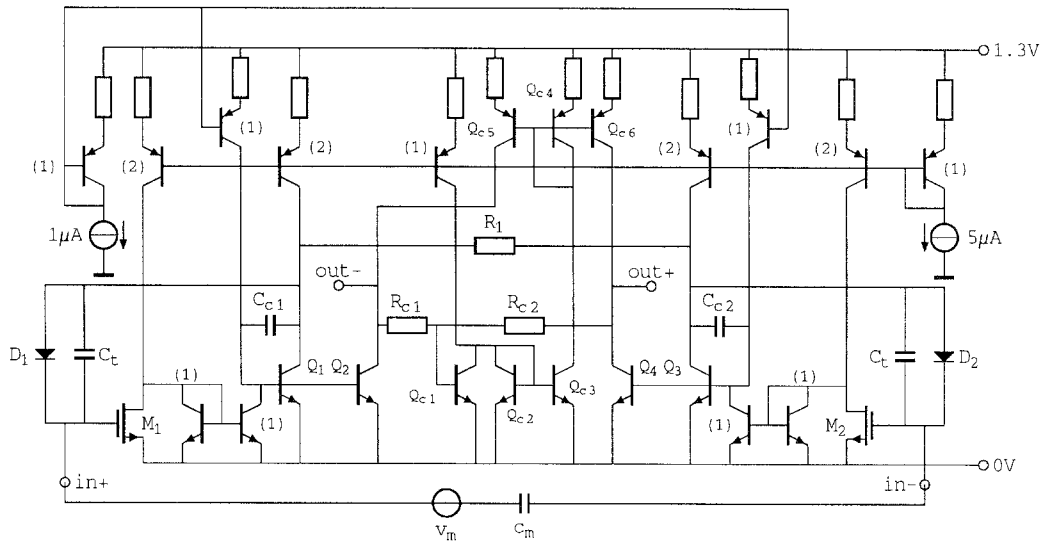


Fig. 5. Complete circuit diagram of the amplifier.

The noise contribution of the output stage now equals (12)

$$S(U_{eqo}) = 4kT \cdot 16425 \quad (15)$$

The contribution of the thermal noise of the MOSFETs to the equivalent input noise spectrum equals (6)

$$S(U_{eqi}) = 4kT \cdot 18000 \quad (16)$$

The total equivalent input noise voltage due to the white noise is $u_{neq} = 25 \text{ nV}/\sqrt{\text{Hz}}$. This equals an input noise voltage of $2.5 \text{ } \mu\text{V}$ over the frequency band (100 Hz–10 kHz), which is equivalent to an unweighted noise level of 20 dB SPL. The contribution of the $1/f$ noise depends on the quality of the MOSFETs and varies with each batch.

A semicustom implementation of the amplifier has been realized in a standard BICMOS process with *NPN* transistors having a maximum transit frequency f_{Tmax} of 3 GHz and *PNP* transistors having an f_{Tmax} of 15 MHz. The f_T of the *NPN* transistors is 200 MHz at a bias current of 10 μA . The typical threshold voltage of the NMOS transistors is 0.75 V, with an f_T of 25 MHz at a bias current of 10 μA .

Figure 6 shows the measured input noise spectrum of the preamplifier. The total noise level is mainly determined by the $1/f$ noise of the MOSFETs. The influence of current noise was not noticeable. The thermal noise level of the amplifier was higher than expected. This was due to the input transistors which showed a higher noise level than was expected. The equivalent input noise voltage over the frequency band (100 Hz–10 kHz)

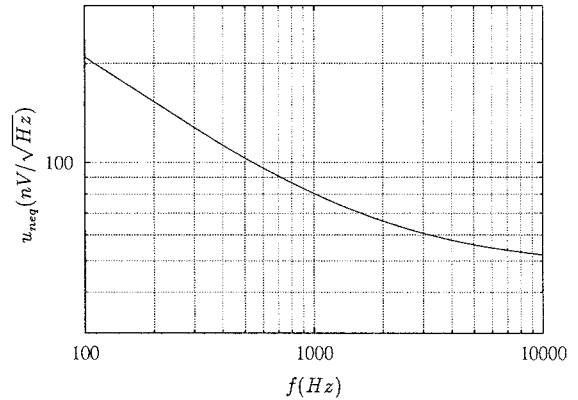


Fig. 6. Measured equivalent input noise of the preamplifier.

equals $6.8 \text{ } \mu\text{V}$. This is equivalent to an unweighted noise level of 28 dB SPL. The transfer of the amplifier is 0.11 mA/V with a bandwidth of 8 Hz–5 MHz.

6. Conclusions

The preamplifier presented in this paper uses current sensing of the electret microphone. At the output indirect current sensing is used. The amplifier is fully balanced. Hence, it is possible to use CM feedback for the biasing of the amplifier and no external components, such as coupling capacitors, are needed. The amplifier has been integrated in a standard BICMOS process.

The total unweighted noise level equals 28 dB SPL, mainly due to $1/f$ noise of the *n*-channel MOSFETs. *P*-channel MOSFETs show less $1/f$ noise than *n*-channel

MOSFETs, so this would improve the SNR. However, p -channel MOSFETs with a sufficiently low threshold voltage were not available in the employed BIMOS process. Due to the balanced configuration, the PSRR can be very high depending mainly on the matching of the transistors.

References

1. D.A. Spring, "On silicon microphones and earphones for hearing aids," *Sensors Actuators*, Vol. 18, pp. 33–44, (1989).
2. M.C. Killion and E.V. Carlson, "A subminiature electret-condenser microphone of new design," *J. Audio Eng. Soc.*, Vol. 22, No. 4, pp. 237–243, 1974.
3. *Broadband EA Series Microphones Data Sheet, EA 1934*, Knowles Electronics Inc., Franklin Park, IL, 1982.
4. J.A. Voorthuyzen, P. Bergveld, and A.J. Sprenkels, "Semiconductor-based electret sensors for sound and pressure," *IEEE Trans. Elect. Insulation*, Vol. 24, No. 2, pp. 267–276, 1989.
5. P.R. Gray and R.G. Meyer, "MOS operational amplifier design—a tutorial overview," *IEEE J. Solid-State Circuits*, Vol. SC-12, No. 3, pp. 224–231, 1977.
6. G. Reimbold and P. Gentil, "White noise of MOS transistors operating in weak inversion," *IEEE Trans. Electron Dev.*, Vol. 29, No. 11, pp. 1722–1725, 1982.
7. François Callias, François H. Salchli, and Dominique Girard, "A set of four ICs in CMOS technology for a programmable hearing aid," *IEEE J. Solid-State Circuits*, Vol. 24, No. 2, pp. 301–312, 1989.
8. E.H. Nordholt. *Design of High Performance Negative Feedback Amplifiers*, Elsevier: New York, 1983.



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