Analog Integrated Circuits and Signal Processing 3, 119–125 (1993)

Biasing a Differential Pair in Low-Voltage Analog Circuits: A Systematic Approach

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Abstract. This paper deals with a systematic approach to the common mode and the differential mode biasing of a differential transistor pair. Four different variants will be shown, two of these variants show practical importance; a practical circuit of one of these variants turns out to be the traditional "long-tailed pair." This variant is mainly suited, if the input signal operates at "voltage level," whereas another variant has great advantages if operation at "current level" occurs. Besides, the latter variant turns out to be very favorable in circuits operating with a single low supply voltage. Two practical circuits based on this variant are given.

Received January 15, 1992; Revised July 10, 1992.

1. Introduction

During the last decade the use of hierarchical methods for the design of analog circuits as negative feedback amplifiers, oscillators, mixers, etc., has gained much interest [1]. Briefly, such methods contain the following design steps: First, an optimal "basic configuration," containing passive components and ideal nullors, is selected. The next step is the design of realistic approximations of those nullors at signal level. At last, the biasing circuits of all active components have to be designed. During each design step first-order calculations are made by hand and exact behavior is predicted with the aid of computer simulations.

In symmetrical nullor approximations for the design of amplifiers, mixers, oscillators, etc., we can make a distinction between differential mode (DM) voltages and currents (signal quantities) and common mode (CM) quantities. Ideally these two quantities do not influence each other so that we can use DM quantities for the desired signal transfer and CM quantities for the biasing. In these symmetrical designs the "differential pair" is the most commonly employed circuit as an individual amplifier stage. In the next section it will be shown that four fundamentally different variants exist for biasing such a stage. One of them turns out to be the traditional "long-tailed pair." However, closer examination reveals that this variant shows some fundamental drawbacks when it is applied in low-voltage circuits, whereas one of the other variants lacks these drawbacks. The small-signal parameters and the noise performance with symmetrical and asymmetrical driving for these two variants are derived. Besides, the reaction on common mode currents and voltages in each case will be given.

2. The Four Basic Methods for Accomplishing Common Mode Feedback in a Differential Pair

In figure 1a a single transistor is depicted as a two-port. Its small-signal behavior can very conveniently be characterized by using a matrix equation with chain parameters, given below.

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_o \\ i_o \end{pmatrix} \tag{1}$$

The chain parameters are defined as

$$A = \left.\frac{v_i}{v_o}\right|_{i_o=0} \tag{2}$$

$$B = \left.\frac{v_i}{i_o}\right|_{v_o=0} \tag{3}$$

$$C = \left.\frac{i_i}{v_o}\right|_{i_o=0} \tag{4}$$

$$D = \left.\frac{i_i}{i_o}\right|_{v_o=0} \tag{5}$$

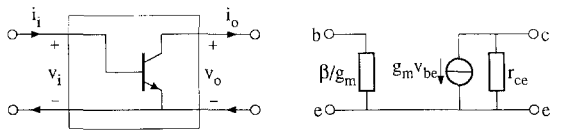

Fig. 1. Transistor depicted as a two-port (a) with equivalent circuit (b).

The use of chain parameters with respect to other parameter sets shows some great advantages. First, they are directly suited for anticausal analysis of negative feedback circuits. Besides, they are closely related to the following important design quantities [1]

$$\text{voltage gain factor} \quad \mu = 1/A \tag{6}$$

$$\text{transadmittance} \quad \gamma = 1/B \tag{7}$$

$$\text{transimpedance} \quad \zeta = 1/C \tag{8}$$

$$\text{current gain factor} \quad \alpha = 1/D \tag{9}$$

In the remainder of this paper the chain parameters of any configuration are related to A, B, C and D. Low-frequency approximations of the quantities μ, γ, ζ, and α can simply be expressed into components of the well-known hyprid-π model of a single bipolar transistor, shown in figure 1b. Some calculation yields

$$\mu = -g_m r_{ce}; \quad \gamma = -g_m; \quad \zeta = -\beta r_{ce}; \quad \alpha = -\beta_{ac} \tag{10}$$

Expressions holding for higher frequences are found in [1].

The conventions used for symmetrical and asymmetrical driving of a differential pair are depicted in figures 2a, b for voltage driving and in figures 2c, d for current driving. Hence, if the circuit is asymmetrically driven, the right-hand sources $v_s/2$ and i_s are made zero. In the case of voltage driving this means that the base of the right-hand transistor is grounded, and in the case of current driving the base of the right-hand transistor is left open. If the circuit is driven asymmetrically the input signal can be considered as the sum of a differential mode and a common mode signal, where

$$E = E_{DM} + E_{CM} \tag{11}$$

and $|E_{DM}| = |E_{CM}|$.

Figures 3a through 3d depict the four possible variants for biasing a differential pair with common mode feedback. i_{cm} and v_{cm} are common mode input sources, whereas i_{dm} and v_{dm} are differential mode input sources. As known, any individual transistor needs fixed values of I_C (or I_E) and V_{CB} (or V_{CE}) for correct biasing. The circuits include the current-biasing, whereas the collector potentials are supposed to be fixed

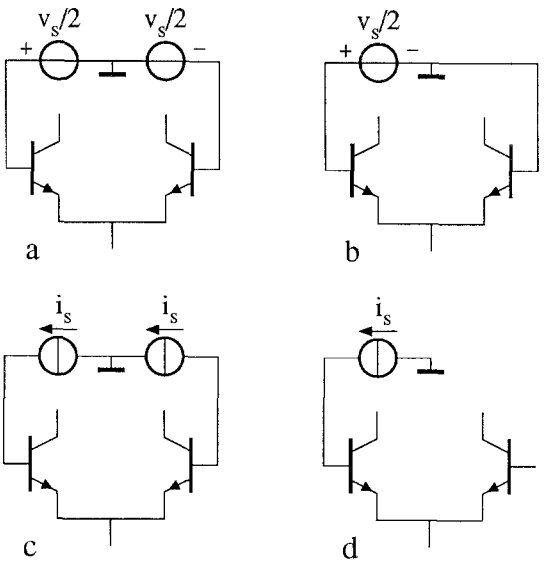

Fig. 2. Symmetrically (a, c) and asymmetrically (b, d) voltage and current driven differential pair.

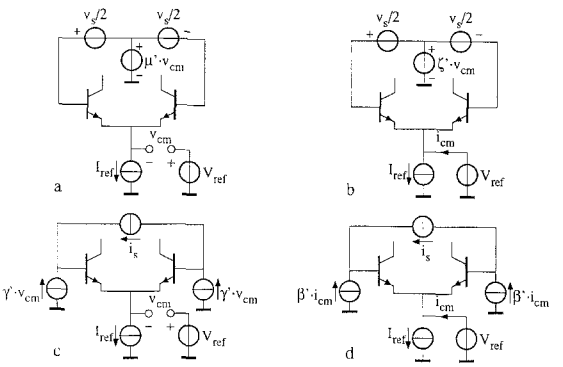

Fig. 3. The four basic configurations.

by the loading circuit(s). Let us now examine the different variants. In all variants common mode biasing is accomplished by two controlled sources. In figures 3a thorugh 3d these are voltage-controlled voltage sources, current-controlled voltage sources, voltage-controlled current sources, and current-controlled current sources, respectively. Their amplification factors are μ', ζ', γ', and β', respectively.

3. Chain Parameters, Common Mode Behavior, and Noise Properties of the Basic Configurations

Now some typical properties of some variants will be derived. First, the chain parameters with symmetrical and asymmetrical driving will be given. Then, the

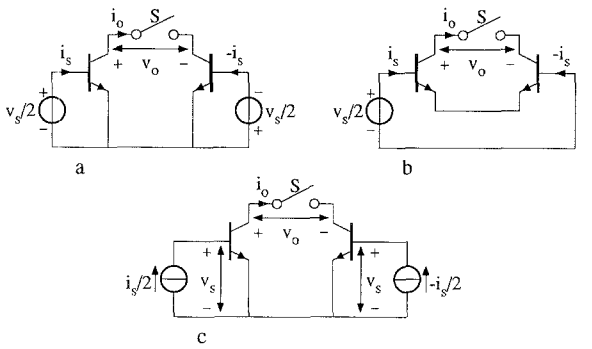

Fig. 4 (a), (b), (c). Simplified circuits for determining the chain parameters. The switches S are closed for the determination of the parameters *B, D* and open for the determination of *A, C.*

discrimination factors for common mode voltages and currents of two variants are examinated. At last, attention will be paid to the noise behavior. With differential mode driving, the controlled sources contain no signal components. Hence, the chain parameters can be derived with the aid of the simplified circuit shown in figure 4a. The transconductance (γ) is halved and the transimpedance (ζ) is doubled compared with a single identical transistor, whereas the current voltage gain factors (β and α) remain unchanged. Hence, the chain matrix of all variants with symmetrical driving is

$$\begin{pmatrix} A & 2B \\ C/2 & D \end{pmatrix} \tag{12}$$

With asymmetrical driving, the chain matrices of the four variants differ from each other. If the amplification factors μ', γ', ζ', and β' are supposed to be infinite and hence perfect common mode feedback occurs, these chain matrices can be derived with the aid of the simplified circuits shown in figure 4b for the configurations of figures 3a, b. As the input voltage is halved compared with the situaiton with symmetrical driving, whereas the input current remains unchanged, the chain parameters A and B are doubled. Hence, the chain matrix of the variants of figures 3a, b is

$$\begin{pmatrix} 2A & 4B \\ C/2 & D \end{pmatrix} \tag{13}$$

If the configurations of figures 3c, d are asymmetrically driven, the input signal currents of the left-hand and the right-hand transistors, are forced to equal $+i_s/2$ and $-i_s/2$, respectively, whereas the input signal voltage remains unchanged. The corresponding chain parameters can easily be found with the simplified circuit shown in figure 4c. Hence, the input currents are halved and the input voltages are doubled with respect to the situation with symmetrical driving, resulting in the following chain matrix:

$$\begin{pmatrix} A/2 & B \\ C & 2D \end{pmatrix} \tag{14}$$

Before the common mode behavior can be considered, suitable definitions are needed. A suitable expression for common mode behavior is the discrimination factor, defined as

$$F_D = G_d/G_c \tag{15}$$

where G_d is the differential mode gain and G_c is the common mode gain. Commonly, voltages are used as input signals for the calculation of those gain factors. However, closer examination yields that distinction must be made between the discrimination factors for voltages and currents. In most cases the output of a differential pair operates at current level. Therefore, the voltage discrimination factor will be defined as follows:

$$F_{DV} = \frac{(i_{o1} - i_{o2})/v_s}{(i_{o1} + i_{o2})/v_{CM}} \quad (v_{o1} = v_{o2} = 0) \tag{16}$$

and the current discrimination factor

$$F_{DC} = \frac{(i_{o1} - i_{o2})/i_s}{(i_{o1} + i_{o2})/i_{CM}} \quad (v_{o1} = v_{o2} = 0) \tag{17}$$

The configuration of figure 3a, which we will call the traditional differential pair, turns out to be a generalized form of the traditional "long-tailed pair," for the inputs operate at voltage level, whereas common mode feedback for input voltages occurs. In the configuration of figure 3c the inputs operate at current level, whereas common mode feedback for voltages occurs. In figure 3b these two operations are just opposite. The inputs operate at voltage level, whereas common mode feedback for currents occurs. The configuration of figure 3d, at last, which we will call the alternative differential pair, the inputs operate at current level, whereas common mode feedback for currents occurs. As a consequence of the properties mentioned above the configurations of figures 3b and 3c are considered as less practical, for the biasing of a single differential pair. In more complex circuits, however, these configurations can be useful. In the next sections it will be shown that the configuration of figure 3d has great importance and leads to many practical circuits that are very suitable for systems, operating at current level with a single, very low supply voltage. Furthermore, the configurations of figures 3a and 3d turn out to be completely dual. Therefore, the following section will only deal with the configurations of figures 3a and 3d.

The discrimination factors of the configurations of figures 3a and 3d will now be calculated, respectively.

3.1. The Traditional Differential Pair

Note that the voltage discrimination factor F_{DV} of the configuration in figure 3a will always be infinite, unless a finite common-emitter impedance Z_{EE} is taken into account. This impedance has been added in figure 5a by dashes.

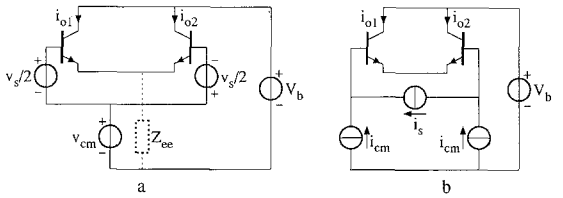

Fig. 5. Configurations for calculating the voltage (a) and current (b) discrimination factor.

Applying equations (3), (5), and (16) to the configuration n figure 3a yields after some calculation

$$F_{DV} = \frac{Z_{EE}(1 - \mu')(D - 1)}{2B} + \frac{1}{4} \tag{18}$$

where B and D are the chain parameters defined in (3) and (5), and μ' is the amplification factor of the voltage-controlled voltage sources in figure 3a. If this configuration is current driven, no common mode feedback occurs, the common mode loop gain becomes zero in this case. For F_{DC} the value 1/2 is found.

If $\mu' = 0$, the configuration degenerates to the traditional "long-tailed pair." A low-frequency approximation of F_{DV} is found if further D is replaced by $-1/\beta_{ac}$ and B by $-2/g_m$ (see equation (10)). The result is

$$F_{DV} = g_m Z_{EE}/2 \tag{19}$$

which is the commonly employed equation for calculating the discrimination factor of the traditional "long-tailed pair" [2]. F_{DV} can be improved by adding extra loop gain. Then the amplification factor of the voltage-controlled voltage sources must have a large value ($\mu' \gg 0$).

3.2. The Alternative Differential Pair

Applying equations (5) and (17) to the configuration in figure 3d yields after some calculation

$$F_{DC} = \frac{-2\alpha'(D - 1)}{2D} + \frac{1}{2} \tag{20}$$

where D is a chain parameter, defined in (5) and α' is the amplification factor of both current-controlled current sources. If this configuration is voltage driven, no common mode feedback occurs. For F_{DV} a value of 1/4 is found. A low-frequency approximation for F_{DC} is found if D is replaced by $-1/\beta_{ac}$ (see (10)). The result is

$$F_{DC} = -\alpha'\beta_{ac} \tag{21}$$

3.3. Noise Performance

The noise properties of the configurations of figures 3a and 3d will be compared with those of a single (identical) transistor. Furthermore the voltage-controlled voltage sources and the emitter impedance Z_{EE} in figure 5a and the current-controlled current sources in figure 3d are supposed to give negligible contributions to the noise behavior. This can be accomplished in most cases by careful design.

Figure 6 depicts a single transistor, all noise sources of which have been transformed to the input. For suitable transformation techniques, see, e.g., [1]. Hence, the transistor is supposed to be noise-free and all noise is concentrated in a noise current with spectrum $S(I)$ and a noise voltage with spectrum $S(V)$.

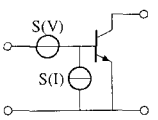

Fig. 6. Single transistor with noise sources.

The resulting equivalent input noise spectra of differential pairs can be found with the aid of figures 7a, b, c. Figure 7a depicts the noise sources of the individual transistors. Application of the Norton-Thévénin theorem to the current spectra and the input impedances of the transistors $Z\pi_1$ and $Z\pi_2$ and summing the resulting voltage spectra (7b) yields a voltage spectrum $S(V')$

$$S(V') = S(I)\{|Z\pi_1|^2 + |Z\pi_2|^2\}. \tag{22}$$

Finally, the spectrum $S(V')$ is transformed back into a current spectrum $S(I')$ with the Norton-Thévénin theorem (7c). The result is

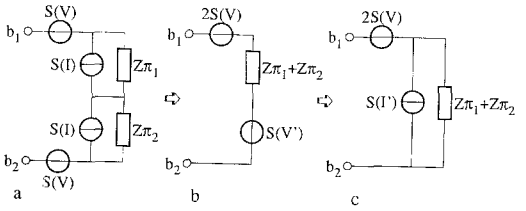

Fig. 7 (a), (b), (c). Determination of the equivalent input noise spectra in differential pairs.

$$S(I') = \frac{S(I)\{|Z\pi_1|^2 + |Z\pi_2|^2\}}{|Z\pi_1 + Z\pi_2|^2} \qquad (23)$$

With (23) the equivalent input spectra of both configurations of figures 3a and 3b with symmetrical driving and the spectra of the configuration of figure 3a with asymmetrical driving can be derived. The spectra of the asymmetrically driven configuration of figure 3b will be explained differently.

3.3.1. Symmetrical driving. Symmetrically driven, in both configurations of figures 3a and 3d, $Z\pi_1$ and $Z\pi_2$ both equal the input impedance of a single common emitter stage. Substituting $Z\pi_1 = Z\pi_2$ in (23) yields $S(I') = S(I)/2$. Hence, the spectrum of the equivalent current noise is halved and that of the equivalent voltage noise is doubled, with respect to the spectra of a single transistor.

3.3.2. The configuration of figure 3a, asymmetrically driven. A strong local feedback in the right-hand transistor (common base behavior) causes that $Z\pi_2 \ll Z\pi_1$. Substitution into (23) yields $S(I') = S(I)$. Hence, the voltage spectrum is doubled compared with a single transistor and the current spectrum remains unchanged.

3.3.3. The configuration of figure 3d, asymmetrically driven. In this case the input signal of the right-hand transistor is obtained indirectly form the signal source. As the base of the right-hand transistor is driven from an infinite impedance, its noise voltage will have no effect. Its noise *current*, however, is added to the input via the common mode loop. Hence, the current spectrum is doubled compared with a single transistor and the voltage spectrum remains unchanged.

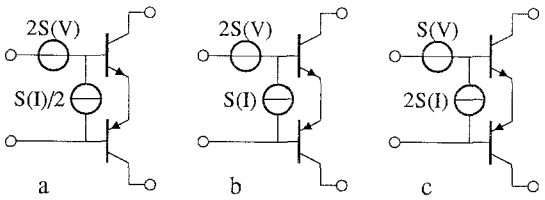

Fig. 8. Equivalent noise sources with symmetrical driving (a), the asymmetrically driven traditional differential pair (b), and the asymmetrically driven alternative differential pair (c).

The resulting noise behavior of both configurations with symmetrical and asymmetrical driving is summarized in figure 8.

It can be concluded, that the configurations of figures 3a and 3d show complete duality with respect to small-signal, common mode, and noise performance. The asymmetrically driven version of figure 3a can be considered as an antiseries connection of two transistors, whereas the asymmetrically driven version of 3d can be considered as an antiparallel connection of two transistors. Furthermore, the configuration of figure 3d completely operates at current level. In the next section it will be shown that this configuration has fundamental features, especially in systems, operating with a single, very low supply voltage (1.0 V or less).

4. Practical Circuits

With the boundary condition mentioned above, the basic configuration, depicted in fiture 3a (generalized long-tailed pair) shows some fundamental drawbacks with respect to that of figure 3d (dual configuration). In practical circuits according to figure 3a, an extra dc voltage reference is inevitable. This source must generally meet very heavy demands. Its value must be quite accurate. Besides, if the source feeds more than one of those stages, it must show a low output impedance for all working frequencies, dc included. (undesired coupling and latching effects). If the stage has to be biased individually, both base connections need a resistive path to ground, in order to make the flow of base current possible. This measure affects the small-signal behavior and the noise properties. The configuration of figure 3d lacks the above-mentioned drawbacks.

A basic difference between both configurations is that both common mode loops of the alternative differential pair always comprise two stages, whereas the common mode loops of the traditional differential pair in its simplest form comprise only one stage (the ampli-

fying transistors themselves). Therefore, the alternative differential pair suffers from two new problems. First, there are two sources of offset, one of the amplifying pairs itself and one caused by the current-controlled sources. Fortunately, the second offset source can be kept very small by exploiting the excellent matching properties of *PNP* transistors in the most I.C. processes [3]. Second, each common mode loop will contain at least two dominant poles. Consequently, frequency compensation in the common mode loops will be needed in some cases.

Many different practical implementations of this configuration are possible. Two examples will be shown. Both circuits can successfully operate with a single supply voltage of 0.8 V. figure 9 depicts a very simple implementation. Q_1 and Q_2 are the basic amplifying transistors. The collectors are loaded with a *PNP* current mirror. If $R_1 = R_2$, the common emitter current approximately equals I_{ref}. A more advanced circuit with accurate symmetrical outputs is shown in figure 10. The CM feedback is applied over two stages in this example. The first stage consist of transistors Q_1 and Q_2, the second stage consists of Q_3 and Q_5. The common mode current is yielded by summing the collector currents of Q_4 and Q_6 and copied by the *PNP* current mirror. As the common mode loop contains three dominant poles, the circuit might show high-frequency instability. However, this can be successfully

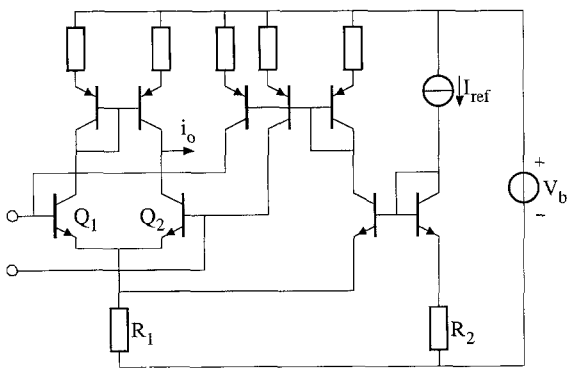

Fig. 9. Simple implementation of figure 3d.

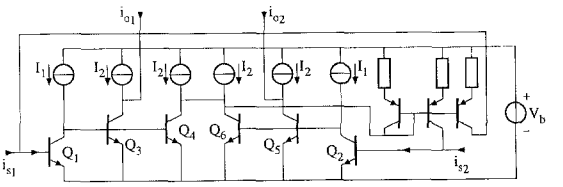

Fig. 10. More advanced implementation of figure 3d.

coped with using a frequency compensation algorithm [3, 4]. An example of a complete low-voltage/low-power amplifier, where the principle of figure 3d is used, can be found in [6].

5. Conclusions

By using CM feedback for the biasing of an amplifier the use of coupling and decoupling capacitors is prevented. It has been shown that four fundamentally different configurations exist for the CM biasing of a single differential CE stage, the "differential pair." One of these configurations, the "alternative differential pair" is very well suited for application in circuits operating at low supply voltages. The small-signal and noise behavior of this configuration is exactly dual to that of the "traditional differential pair." The traditional differential pair suppresses CM voltages, whereas the "alternative differential pair" suppresses CM currents. Although in the basic configurations the CM feedback is restricted to one stage, it can be applied to several stages as well.

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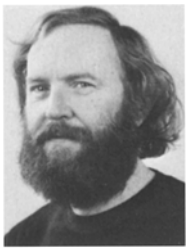

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