A Compact Rail-to-Rail Class-AB CMOS Buffer With Slew-Rate Enhancement

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***Abstract*—Two prior-art transconductance amplifier-based rail-to-rail class-AB analog buffers are examined. Their analysis reveals that the output current drive capability for large input voltages is restricted. To mitigate this drawback, a relatively simple slew-rate enhancement scheme is proposed. The new scheme allows the buffer's speed to be increased by over 200% with only a very small increase in static power consumption (1.25%) and silicon area (3%). The proposed and the two conventional buffers were fabricated in a 0.35-μm CMOS technology for a power supply of 3 V. Measurements verify the superior slew-rate performance of the new buffer for rail-to-rail step responses.**

***Index Terms*—Analog buffer, class AB, CMOS circuits, high speed, rail to rail, slew-rate enhancement.**

I. Introduction

IN ORDER to drive a large capacitive load, an analog buffer (or voltage follower) implemented by a transconductance amplifier g_m connected in negative feedback as shown in Fig. 1(a) is the most fundamental and widely used driving scheme. Examples include liquid crystal display drivers [1], [2], low-dropout regulators [3], [4], and analog testing and signal monitoring [5]. Class-AB buffers are usually preferred for their high power efficiency and low harmonic distortion [6]. In Fig. 1(a), r_o and C_L represent the output resistance of the g_m circuit and the load capacitor, respectively. Before settling, i.e., $t_0 \leq t \leq t_s$ [see Fig. 1(b)], the g_m circuit should have a high output current drive capability to quickly charge (or discharge) C_L. After settling, i.e., at time $t \geq t_s$, the output voltage $V_{\rm out}$ should (ideally) follow the input voltage $V_{\rm in}$. In practice, the common-mode (CM) range (CMR) of the g_m circuit limits the signal range over which $V_{\rm out}$ follows $V_{\rm in}$. Thus, to simultaneously achieve low-power consumption, high slew rate, and high signal-to-noise ratio, a compact class-AB g_m circuit with rail-to-rail CMR is required.

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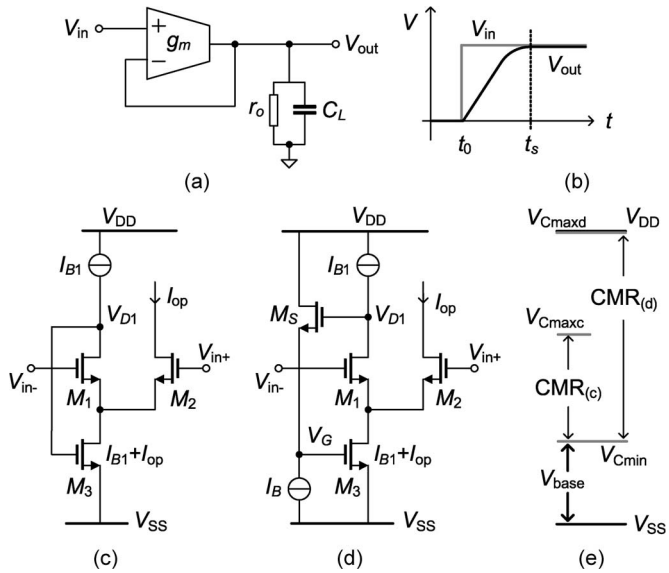

Fig. 1. (a) Transconductance amplifier-based voltage follower. (b) Output settling with slewing. (c) DFVF transconductor. (d) DFVF transconductor with extended CMR. (e) CMR of both circuits.

An analog CMOS buffer that meets these criteria was proposed by Carrillo et al. in [7]. The circuit uses two complementary class-AB differential flipped voltage follower (DFVF) transconductors [8], assisted by a pair of adaptive biasing circuits, which serve to ensure that the two output transistors are correctly biased for almost the entire signal range of the supply rails. The adaptive circuits utilize four simple current mirrors and a couple of extra transistors, making the buffer attractive for low-power applications.

In [9], the authors showed that the adaptive biasing mechanism still remains despite removing the four current mirror circuits from the buffer design in [7]. This modification reduces the static power consumption and transistor count requirements of the buffer by 30% and 35%, respectively.

However, both the buffer designs in [7] and [9] share a common drawback: Their output current drive capability for large input voltages is restricted. This limitation is fundamental to their circuit architecture, and it cannot be avoided if we want to have both class-AB and rail-to-rail operations simultaneously. In this brief, we analyze the origin of this limitation. Based on the analysis, we present a compact scheme to enhance output current drive capability for full rail-to-rail input signal swing, without degrading any other key performance aspect. The proposed modification greatly increases the buffer's slew rate while requiring only a very small increase in static power consumption and silicon area. To verify the concept, the buffer

designs in [7] and [9] and the proposed buffer were designed and fabricated in a 0.35-μm CMOS technology. The measured results are consistent with the analysis.

In the next section, a review of prior-art class-AB analog voltage buffers along with their performance analysis is presented. Section III proposes the slew-rate enhancement technique, while Section IV shows the new buffer. The measured results and comparison of the designs are presented in Section V, followed by concluding remarks in Section VI.

II. Rail-to-Rail Analog Buffers: Prior-Art Design

A. CM Behavior

Fig. 1(c) and (d) shows the DFVF transconductors (which have been used as the basic circuit cell in the buffer designs in [5], [7], and [9]) and their CMR limitations. Referring to Fig. 1(b) after settling, the situation is similar to applying a CM voltage to both input terminals of the g_m circuit. Using the transconductors in Fig. 1(c) and (d) as the g_m circuit, their CM voltage ranges will define the available range for signal swing.

Considering the circuit in Fig. 1(c), the minimum and maximum CM voltages can be derived using the square-law function of the MOS transistor in the strong inversion saturation (SIVS) region. Since transistors M_1 and M_2 have the same gate–source voltages $(V_{\rm GS})$, neglecting channel length modulation (CLM), they conduct the same drain currents I_{B1}. We thus find that

$$V_{\rm CM\,min} = V_{\rm SS} + V_{tn} + \sqrt{\frac{2I_{B1}}{\beta_3}} + \sqrt{\frac{I_{B1}}{\beta_{1,2}}} \tag{1}$$

$$V_{\rm CM\,max(c)} = V_{\rm SS} + 2V_{tn} + \sqrt{\frac{2I_{B1}}{\beta_3}} \tag{2}$$

where V_{tn} and β_i represent the threshold voltage of an nMOS device and the process transconductance of each device, respectively. The CMR of this circuit is $\text{CMR}_{(\rm c)} = V_{tn} - \sqrt{I_{B1}/\beta_3}$. This range is too small, and it is thus not recommended to apply this circuit as a buffer that has to deal with large input signal swings.

To extend the CMR, a level shifter is inserted to shift up voltage V_{D1}, as shown in Fig. 1(d) [7], [9]. V_{D1} should ideally be set to allow the maximum CM input voltage of the circuit (i.e., $V_{\rm CM\,max(}b{\rm)}$) to reach the supply voltage $V_{\rm DD}$, i.e., $V_{D1} = V_{\rm DD} - V_{tn}$. This can be achieved by the appropriate sizing of transistor M_S according to the following relationship:

$$V_{D1} = V_{\rm SS} + V_{tn} + V_{tnS} + \sqrt{\frac{2I_{B1}}{\beta_3}} + \sqrt{\frac{I_B}{\beta_S}}. \tag{3}$$

Note that for an n-well CMOS process, V_{tnS} will be affected by the body effect and $V_{tnS} > V_{tn}$. Also, V_{D1} is a key parameter that limits the drive capability of the buffer (see Section II-D). The CMR lower bound of both circuits in Fig. 1(c) and (d) is identical and defined by (1). For the circuit in Fig. 1(d), the CMR is thus

$$\begin{aligned}\text{CMR}_{(\rm d)} &= V_{\rm DD} - V_{\rm SS} - \left(V_{tn} + \sqrt{\frac{2I_{B1}}{\beta_3}} + \sqrt{\frac{I_{B1}}{\beta_{1,2}}}\right) \\ &= V_{\rm DD} - V_{\rm SS} - V_{\rm base}.\end{aligned} \tag{4}$$

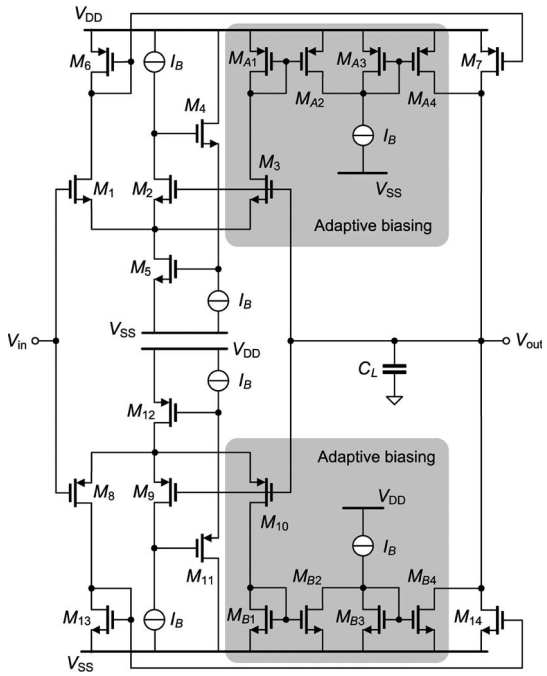

Fig. 2. Class-AB rail-to-rail analog buffer [7].

B. Achieving Rail-to-Rail Signal Swing

The third term in (4) $(V_{\rm base})$ can be avoided when floating gate devices are used [10]. However, it is also possible to extend the CMR using complementary transconductors and adaptive biasing networks. Fig. 2 shows the schematic of the rail-to-rail class-AB buffer in [7]. In the design, all bias currents are set to I_B. The buffer may be divided into upper and lower parts, each of them featuring a DFVF transconductor of the type in Fig. 1(d) (the upper circuit is nMOS type and the lower circuit is pMOS) and an adaptive biasing circuit. The output currents of the upper and lower transconductors are conveyed to the output via current mirrors M_6–M_7 and M_{13}–M_{14}, respectively. To keep transistors M_7 and M_{14} in the SIVS region, the supply voltage needs to provide a minimum voltage drop of $V_{\rm eff7} + V_{\rm eff14}$ for M_7 and M_{14} ($V_{\rm eff7}$ and $V_{\rm eff14}$ are the effective voltages of M_7 and M_{14}, respectively). Hence, ignoring the CMRs of the DFVF transconductors, $V_{\rm out}$ can swing within the following range:

$$V_{\rm SS} + \sqrt{\frac{I_B}{\beta_{14}}} \le V_{\rm out} \le V_{\rm DD} - \sqrt{\frac{I_B}{\beta_7}}. \tag{5}$$

In practice, when the CMRs of the DFVF transconductors are taken into account, the current mirrors M_6–M_7 and M_{13}–M_{14} cannot function properly over the full range of (5) without assistance from the adaptive biasing networks shown in the shaded areas in Fig. 2. Applying the analysis in Section II-A to the buffer in Fig. 2, it follows that the minimum and maximum CM voltages of the upper and lower DFVF transconductors are respectively given by

$$V_{\rm CM\,min\,}{}_U = V_{\rm SS} + V_{tn} + \sqrt{\frac{3I_B}{\beta_5}} + \sqrt{\frac{I_B}{\beta_{1,2,3}}} \tag{6}$$

$$V_{\rm CM\,max\,}{}_L = V_{\rm DD} - \left(|V_{tp}| + \sqrt{\frac{3I_B}{\beta_{12}}} + \sqrt{\frac{I_B}{\beta_{8,9,10}}}\right) \tag{7}$$

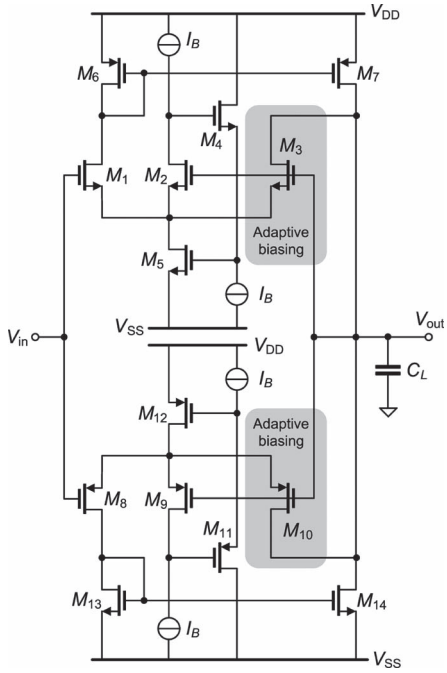

Fig. 3. Class-AB rail-to-rail analog buffer with compact adaptive biasing [9].

where V_{tp} is the threshold voltage of a pMOS device.

If $V_{\rm in}$ goes high, reaching condition (6), M_{14} will stop conducting current, and the lower adaptive biasing circuit will provide I_B to M_7, keeping the feedback loop closed until $V_{\rm out}$ reaches the upper bound of (5). The same mechanism holds for the upper adaptive biasing circuit when $V_{\rm in}$ goes low and meets condition (7).

C. Compact Adaptive Biasing

In [9], the current mirrors $M_{A1}-M_{A4}$ and $M_{B1}-M_{B4}$ in the shaded areas in Fig. 2 are removed, resulting in the buffer circuit in Fig. 3. Instead of supplying current I_B via those current mirrors, the drain terminals of M_3 and M_{10} are connected to the output terminal directly. Now, the adaptive biasing mechanism for each DFVF transconductor is handled by a single transistor. Since the DFVF circuits used in this buffer are still identical to those used in the buffer in Fig. 2, (6) and (7) are still applicable.

When $V_{\rm in}$ goes high and condition (6) is met, all transistors of the lower part will be cut off. At this point, M_3 takes care of $I_{D7} = I_{D3} = I_B$. Also, when $V_{\rm in}$ goes low and condition (7) is met, the upper part is shut down, and M_{10} is responsible for $I_{D14} = I_{D10} = I_B$. This alteration yields a rail-to-rail operation with a more compact design and less power consumption, while similar settling and slewing performances remain.

D. Driving Capability Limitation

Using the square-law function of the MOS transistor in the SIVS region, taking into account that $V_{\rm GS2}$ is constant due to I_B and again neglecting CLM, we find that the output current of the upper part of the buffer (i.e., the drain currents of M_1 and M_7 in Figs. 2 and 3), assuming equal dimensions for M_1-M_3 ($\beta_1 = \beta_2 = \beta_3$), is given by

$$I_{oU} = \begin{cases} \beta_1 \left(V_{\rm id} + \sqrt{\frac{I_{B1}}{\beta_1}} \right)^2 & \text{for } V_{\rm id} \geq -\sqrt{\frac{I_{B1}}{\beta_1}} \\ 0 & \text{for } V_{\rm id} < -\sqrt{\frac{I_{B1}}{\beta_1}} \end{cases} \quad (8)$$

where $V_{\rm id} = V_{\rm in+} - V_{\rm in-} = V_{\rm in} - V_{\rm out}$. It can be seen from (8) that, for $V_{\rm id}$ being less than the effective voltage of M_1, no current will be conveyed to the output. However, when $V_{\rm id}$ exceeds that limit, I_{oU} increases quadratically with $V_{\rm id}$. Unfortunately, this is not entirely true. The quadratic equation of (8) is obtained from the assumption that the feedback loop around $M_1-M_4-M_5$ forces the source terminal of M_1 to act as a virtual ground node that can sink infinite current. In practice, $I_{D1}(= I_{oU})$, I_{D2}, and I_{D3} will all combine through M_5, yielding

$$I_{D5} = 2I_B + I_{oU}. \quad (9)$$

We can now see that the maximum output current of the upper circuit $I_{oU\,\max}$ is limited by the sinking capability of M_5 (first limit) and that $V_{\rm SG6}$ increases with I_{oU}, forcing M_1 to enter the triode region (second limit).

Based on the CMR setting mentioned in Section II-A and the practical output voltage swing of (5), it is reasonable for the DFVF circuit in Fig. 3 to have a quiescent point of

$$V_{D2Q} = V_{\rm DD} - V_{\rm eff7} - V_{tn} = V_{\rm DD} - \left(V_{tn} + \sqrt{\frac{I_B}{\beta_7}} \right). \quad (10)$$

Suppose that the current source I_B is implemented by a simple current mirror and requires a minimum voltage drop of $V_{\rm effB}$, the maximum gate voltage of M_5 is given by

$$V_{G5\,\max} = V_{\rm DD} - V_{\rm effB} - V_{\rm GS4}. \quad (11)$$

If V_{G5} goes higher than this value, current source I_B will enter the triode region, and (8) is no longer maintained. Hence, (11) restricts the maximum output current to

$$\begin{aligned} I_{oU\,\max} &= \beta_5 (V_{G5} - V_{\rm SS} - V_{tn})^2 - 2I_B \\ &= \beta_5 \left((V_{\rm DD} - V_{\rm SS}) - (V_{\rm effB} + V_{\rm eff4}) \right. \\ &\quad \left. - (V_{tn4} + V_{tn}) \right)^2 - 2I_B \end{aligned} \quad (12)$$

where we took the difference in the body effect of M_4 and M_1-M_3 into account. This first limit results from the CMR extension mentioned in Section II-A. It can be observed that, using this circuit, the output current will never meet the second limit since the gate voltage of the sinking transistor is limited within a very fixed range of $V_{G5\,\max} - (V_{D2Q} - V_{\rm GS4}) \cong V_{tn}$. The second limit, on the other hand, depends on $V_{\rm DD}$ and the dimension of M_6 which can be set to be higher than (12).

A similar circuit analysis can be applied to the lower part of the buffer, and the first limit of its output current can be expressed as

$$I_{oL\,\max} = \beta_{12} \left((V_{\rm DD} - V_{\rm SS}) - (V_{\rm effB} + V_{\rm eff11}) - 2|V_{tp}| \right)^2 - 2I_B. \quad (13)$$

III. Proposed Slew-Rate Enhancement Scheme

We have seen from the previous section that the buffer's output current affects the gate voltages of the sinking and sourcing transistors M_5 and M_{12}. The level shifters are inserted for

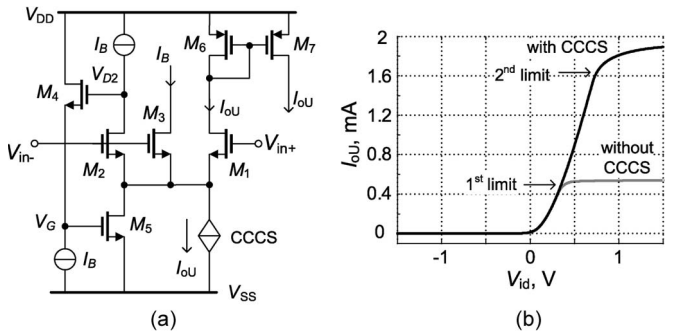

Fig. 4. (a) DFVF transconductor with adaptive tail current. (b) Output current dc transfer characteristics.

CMR extension, and unfortunately, they attenuate the voltage headroom of V_{G5} and V_{G12} significantly. The resulting small voltage headroom directly limits the output current.

Fig. 4(a) shows the proposed scheme to let the output current meet the second limit without the need for a larger voltage headroom. This is achieved by inserting a current-controlled current source (CCCS) between the common source terminal of M_1-M_3 and $V_{\rm SS}$. Current I_{oU} controls the CCCS with unity gain. In this case, the CCCS is responsible for the sinking current, thereby allowing M_5 to only provide a constant current of $2I_B$. For this reason, V_{G5} and V_{D2} do not require any signal swing headroom, and I_{oU} can go beyond the first limit. This allows the second limit to be met. As I_{oU} keeps rising when $V_{\rm id}$ is applied, $V_{\rm SG6}$ will increase, forcing the drain voltage of M_1 to go down. Eventually, for the case of $V_{\rm DD}=-V_{\rm SS}$ and $V_{\rm in-}=0$, M_1 will enter the triode region when

$$V_{\rm id}=V_{\rm in+}=V_{\rm DD}+V_{tn}-|V_{tp}|-\sqrt{\frac{I_{oU\,\max 2}}{\beta_6}} \qquad (14)$$

and the maximum output current can be approximated as (assuming $V_{tn}=-V_{tp}$)

$$I_{oU\,\max 2}\cong\beta_1\beta_6\left(\frac{V_{\rm DD}+\sqrt{\frac{I_B}{\beta_1}}}{\sqrt{\beta_1}+\sqrt{\beta_6}}\right)^2. \qquad (15)$$

Beyond this range, the output current continues to increase further according to the triode region behavior.

Fig. 4(b) shows the output current characteristics of the DFVF transconductor with and without an adaptive tail current. The graph was obtained from circuit simulation using the model parameters of a 0.35-μm CMOS technology with $V_{tn}\cong 0.55$ V and $V_{tp}\cong -0.71$ V. The power supply was set to 3 V and $I_B=10$ μA. As can be seen from the gray curve (without CCCS), the output current saturates when $V_{\rm id}$ $(V_{\rm in+}-1.5$ V) is slightly less than 0.5 V, giving a maximum output current of about 0.5 mA. When the CCCS is applied, the second limit is met at $V_{\rm id}\cong 0.75$ V and $I_{oU}\cong 1.65$ mA. For higher values of $V_{\rm id}$, I_{oU} continues to rise and reaches 1.85 mA at $V_{\rm id}\cong 1.5$ V which is at the maximum supply rail. It can be seen that, using this technique, the maximum output current is enhanced by more than 300%.

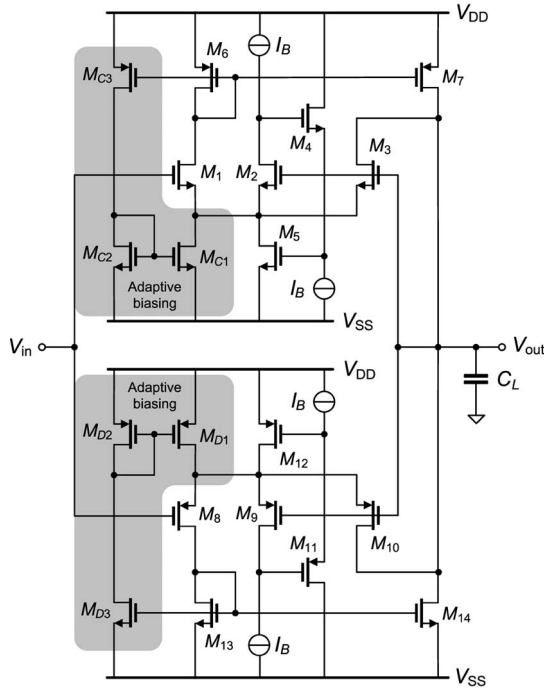

Fig. 5. Proposed class-AB rail-to-rail buffer with slew-rate enhancement.

IV. New High-Speed Buffer

The proposed adaptive biasing scheme can be implemented in a compact low-power fashion by using scaled current mirror circuits. Fig. 5 shows the schematic of the new slew-rate-enhanced rail-to-rail class-AB buffer. Developed from the compact design in [9], the set of transistors M_{C1-3} and M_{D1-3} shown in the two shaded areas is inserted to implement the CCCSs. In the upper part of the circuit, the drain current of M_6 (I_{D6}) is scaled down by M_{C3} with a scaling-down factor of k. This scaled current is subsequently injected into the current mirror $M_{C2}-M_{C1}$, which has a reciprocal scale factor of k^{-1}. M_{C1} is conducting I_{D6} from the same branch of M_1 and M_6, and thus, the current consumption of this branch remains the same. The additional current consumption of kI_{D6} is required only for the branch of M_{C3} and M_{C2}. To keep power consumption low, k should be as small as possible. In practice, it is limited by the value that keeps the current mirror pairs $M_{C1}-M_{C2}$ and $M_{D1}-M_{D2}$ working in their SIVS region. In this design, $k=0.05$ was used. This results in a 1.25% increase in power and current consumption compared to the buffer in Fig. 3. Nevertheless, the device count, silicon area, and power consumption of the new buffer are still smaller than the buffer in Fig. 3 (see results in Section V). In the lower part of the circuit, the adaptive biasing mechanism is formed via $M_{D1}-M_{D3}$.

V. Experimental Results

For verification and comparison, the two buffers of [7] and [9] and the new buffer were designed and fabricated in a 0.35-μm CMOS technology for a 3-V-power-supply operation. Fig. 6 shows the die microphotograph with the area of each buffer marked. Buffer 1 is the circuit in Fig. 2, buffer 2 is the circuit in Fig. 3, and buffer 3 is the new buffer. Referring to Fig. 2, transistors M_1-M_{14} are found in all three buffers and were given the same sizing. Bias current I_B was set to 10 μA in

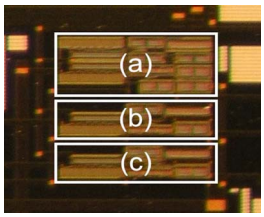

Fig. 6. Die photograph of the buffers. (a) Buffer 1. (b) Buffer 2. (c) Buffer 3.

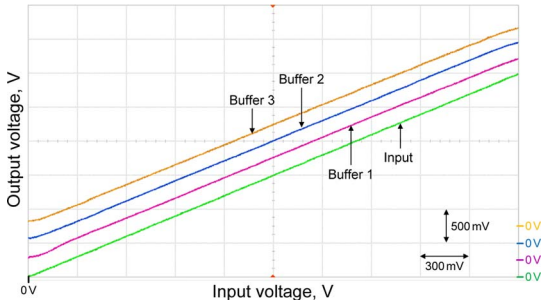

Fig. 7. Measured dc transfer characteristics of the buffers. The input signal is also shown. For clarity, the line graphs are offset by 250 mV.

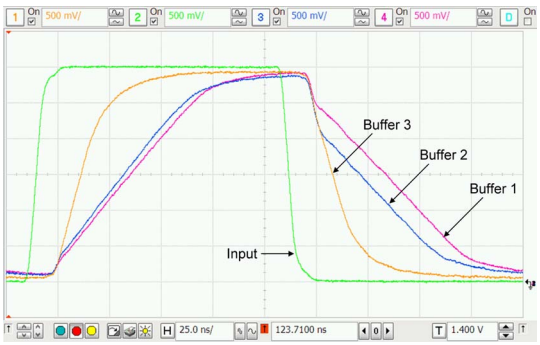

Fig. 8. Rail-to-rail step responses of the buffers each driving a 20-pF load. The input signal has an amplitude of 3 V and a frequency of 4 MHz.

all buffers. In total, 20 chips were fabricated and tested with all samples working. The chips exhibited a similar behavior with variations in performance of less than 5%. The results reported hereinafter are from a typical chip.

Fig. 7 shows the buffers' dc transfer characteristics showing their rail-to-rail capability. The maximum offset voltage $|V_{\rm in} - V_{\rm out}|_{\rm max}$ at the extremes of the input range (0 and 3 V) as calculated by the math function of the oscilloscope (Agilent MSO9104A) is similar for all buffers, 47 , 44, and 41 mV for buffer 1, buffer 2, and buffer 3, respectively. These offset voltages occur when the output transistors operate outside their SIVS region into the triode region. For the majority of the transfer functions, the offset voltage is less than 5 mV.

Fig. 8 shows the buffers' rail-to-rail step responses with a load capacitance of about 20 pF each. The load consisted of the parasitic capacitances associated with the chip package and printed circuit board (∼8 pF) and the probe input capacitance (12 pF // 2.2 MΩ). Buffer 3 has the fastest slew rate (rising edge slew rate is 79.4 V/μs; falling edge slew rate is 83.6 V/μs), while buffer 1 has the slowest slew rate (rising edge slew rate is 34.5 V/μs; falling edge slew rate is 33.6 V/μs). Table I summarizes the measured performance of the three buffers.

TABLE I
PERFORMANCE SUMMARY OF BUFFERS

Parameter	Buffer 1 [7]	Buffer 2 [9]	Buffer 3 [new buffer]
Process technology	0.35 µm CMOS		
Power supply (V)	3		
Total quiescent current (µA)	110	80	81
Transistor count	22	14	20
Active area (µm^2)	25935	13655	14060
$\lvert V_{\rm in} - V_{\rm out}\rvert_{\rm max}$ (mV)	47	44	41
THD, 10 kHz sine input (%)			
1.5 V peak-peak	0.046	0.043	0.041
2.9 V peak-peak	1.124	1.116	1.090
Settling time, 20 pF load (ns)			
2 V square input	138	139	52
3 V square input	175	176	87
Slew-rate (V/µs)	34	37	81
–3dB bandwidth (MHz)	5.9	5.6	5.8

They exhibit a similar total harmonic distortion (THD) and −3-dB bandwidth.

VI. CONCLUSION

In this brief, a simple slew-rate enhancement scheme for rail-to-rail class-AB CMOS buffers has been presented. The technique enables the buffer's slew rate to increase by more than 100% compared to prior art, with only a small increase in static power consumption and silicon area. For comparison, the three buffers were fabricated in a 0.35-μm CMOS technology for a power supply of 3 V. Measurements verify that the new buffer has superior slew rate and settling time, while it has similar harmonic distortion, bandwidth, and offset to the two other buffers.

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