A 90 nm-CMOS IR-UWB BPSK Transmitter With Spectrum Tunability to Improve Peaceful UWB-Narrowband Coexistence

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***Abstract*—A new ultra wideband (UWB) pulse generator covering a –10 dB bandwidth of 2.4–4.6 GHz with a tunable center frequency of 5–5.6 GHz to mitigate coexistence issues of impulse radio UWB (IR-UWB) systems and IEEE802.11.a WLAN or other narrowband (NB) systems in 90 nm-CMOS technology is proposed. The UWB pulse is generated based on frequency up-conversion of the first derivative of the Gaussian pulse, which creates an adjustable null in the frequency spectrum. Simulation results show that employing the proposed pulse generator mitigates the mutual interference between UWB and WLAN systems, significantly. The proposed transmitter consists of a low frequency signal generator, an LC oscillator and a mixer, whose output directly drives the antenna using a matching on-chip transformer. Two control signals change the bandwidth and center frequency of the transmitted spectrum depending on the NB frequency and considering process, supply voltage and temperature (PVT) variations. A fast start-up circuit is used in the LC oscillator using current pulse injection and together with the mixer is duty cycled to reduce the power consumption. Post-layout simulation results show a null depth of 23 dB for a null bandwidth of 100 MHz. The energy/pulse and energy/pulse normalized to the output voltage amplitude are 14.4 pJ/pulse and 35.7 pJ/(pulse-V) from a 1-V supply for a pulse rate of 860 Mpulse/s with an active circuit area of only 0.18 mm².**

***Index Terms*—BER performance, IEEE802.11a WLAN, narrowband interference avoidance, spectrum null, UWB pulse generator.**

I. Introduction

BECAUSE of coexistence issues of UWB systems with in-band narrow-band (NB) systems, shaping the power spectrum of the UWB signal to mitigate mutual interference is an important concern. The main idea is to have a spectral notch in the transmitted frequency band where the NB spectrum appears. Both bit sequence and pulse shaping of the output signal can affect the spectrum. In [1]–[4], time-hopping codes are designed to generate a notch at the desired RF frequency. However, finding a large set of codes (required for multiple access) is a difficult problem. In [5]–[7] UWB pulse shaping that produces a null in the frequency spectrum has been proposed. Implementation issues, null tunability to align with the NB frequency and its stability have not been considered in these designs. The authors in [8] generated two UWB pulses using fixed bandpass filters in the low and high UWB band and added them together to get a new pulse that contains a non-tunable null in the spectrum.

In this paper, the pulse generator is designed to be implemented in 90 nm CMOS technology and to have a notch in its transmitted frequency spectrum. To accomplish this, the first derivative of the Gaussian pulse (the so-called monocycle) has been multiplied by a carrier to realize frequency shifting. The up-converted pulse will include the desired tunable notch in its spectrum located at the local oscillator frequency (f_{LO}). The design is based on the conceptual effort in [9]. This structure allows for more flexibility as the notch frequency can be precisely controlled according to the existing NB system. The interference performance of 802.11a WLAN on UWB and UWB on 802.11a WLAN are simulated using Advanced Design System (ADS) software. In addition, for a fair comparison, the results include a frequency shifted Gaussian pulses (the so-called modulated Gaussian without a null) as well.

The proposed transmitter circuit consists of a low frequency signal (LFS) generator to generate the monocycle pulses, an LC oscillator with a fast start-up circuit and a mixer, whose output directly drives the antenna using a matching on-chip transformer. Two control signals change the bandwidth and center frequency of the transmitted spectrum. A first control signal changes the total bandwidth of the transmitted spectrum from 2–4 GHz. A second control signal is used to tune the center frequency from 5.0–5.6 GHz. The controls allow for adjustment of the null to coincide with the NB interference and also to compensate for process, supply voltage and temperature (PVT) changes that can affect the generated spectrum. In order to reduce the power consumption, current impulse injection is used in the oscillator, which together with a mixer is turned on and off. Post layout simulations using Spectre RF exhibit a null depth of more than 22 dB for a null bandwidth of 100 MHz which is sufficient for almost all NB systems when the output power spectrum density (PSD) is -41.3 dBm/MHz. The energy/pulse normalized to the output voltage amplitude is

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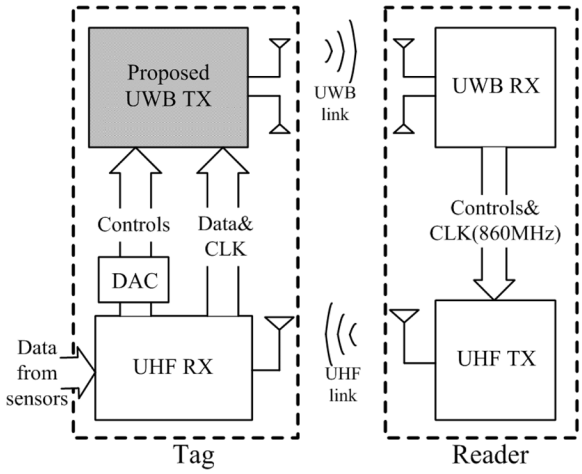

Fig. 1. RFID Tag and Reader system with control and calibration.

35.7 pJ/(pulse-V) from a 1-V supply for a 860 Mpulse/s pulse rate. The integrated circuit (IC) occupies a die area of 0.6 mm^2 including bonding pads, ESD pads and capacitors, while the active circuit area is only 0.18 mm^2.

Fig. 1 shows an application of the proposed transmitter in the Tag section of an UWB RFID system. This type of RFID employs two different communication links including UWB and UHF in uplink and downlink, respectively [10]. The UWB RX is composed of a matched filter receiver and a Phase Locked Loop (PLL). Before the data detection in UWB link, the Reader performs the following tasks: 1) Scanning the spectrum of the environment to discover the center frequency of interference. 2) Approximate tuning of the center frequency, null depth and FCC mask requirements of the UWB TX by transmitting appropriate commands via UHF link. 3) Frequency and phase locking on the center frequency of UWB TX. After performing the above tasks, the Reader starts to detect the Tag transmitted data. As shown above, the frequency and phase of UWB TX and RX in the data detection stage are equal, thereby providing the matched filter or coherent detection in the Reader.

The paper is organized as follows: Section II gives analytical formulations for the proposed IR-UWB pulse, showing how to create the null in the spectrum. The mutual interference of UWB and 802.11a WLAN when using the proposed UWB pulses is simulated in Section III. The proposed transmitter circuit block diagram and the post layout simulation results are presented in Sections IV and V. Finally conclusions are given in Section VI.

II. UWB Pulse Synthesis

The modulated Gaussian (MG) pulse and modulated monocycle pulse (MM) have been introduced in [9], [11] and are defined as below in the time and frequency domains:

$$g_{MG}(t) = k_1 e^{-\left(\frac{t}{\tau}\right)^2} \cos(2\pi f_{LO} t) \tag{1}$$

$$\begin{aligned} G_{MG}(f) &= \int_{-\infty}^{+\infty} g_{MG}(t) e^{-j2\pi f t} dt \\ &= k_1 \tau \frac{\sqrt{\pi}}{2} \left[e^{-(\pi\tau(f-f_{LO}))^2} + e^{-(\pi\tau(f+f_{LO}))^2} \right] \end{aligned} \tag{2}$$

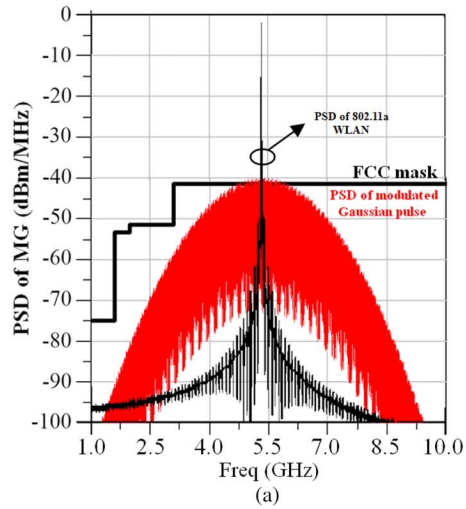

Fig. 2. PSD of transmitted UWB signals and PSD of 802.11a WLAN with a center frequency of 5.3 GHz (a) the PSD of 802.11a WLAN and the PSD of the UWB signal when using a modulated Gaussian pulse shape. (b) The PSD of 802.11a WLAN and the PSD of the UWB signal when using a modulated monocycle pulse shape (proposed pulse).

$$g_{MM}(t) = k_2 \frac{-2t}{\tau^2} e^{-\left(\frac{t}{\tau}\right)^2} \cos(2\pi f_{LO} t) \tag{3}$$

$$\begin{aligned} G_{MM}(f) &= \int_{-\infty}^{+\infty} g_{MM}(t) e^{-j2\pi f t} dt \\ &= k_2 \tau \pi \sqrt{\pi} j \left[(f - f_{LO}) e^{-(\pi\tau(f-f_{LO}))^2} \right. \\ &\qquad \left. + (f + f_{LO}) e^{-(\pi\tau(f+f_{LO}))^2} \right] \end{aligned} \tag{4}$$

where k_1, k_2 and τ are the energy and time scaling factors, respectively. Comparison of (2) with (4) reveals that $G_{MM}(f)$ contains a null at $f = f_{LO}$. Figs. 2(a) and (b) show the PSD of the transmitted signal $P_s(f)$, when utilizing MG and MM pulse shapes. The energy and time scaling is chosen to meet the FCC requirements. In this plot, we have depicted the PSD of both 802.11a WLAN and the PSD of the UWB signals for easy understanding of coexistence issues.

III. UWB and 802.11a WLAN Coexistence Simulation

The use of an MM pulse in the UWB transmitter makes the system extremely robust. The UWB link can withstand large

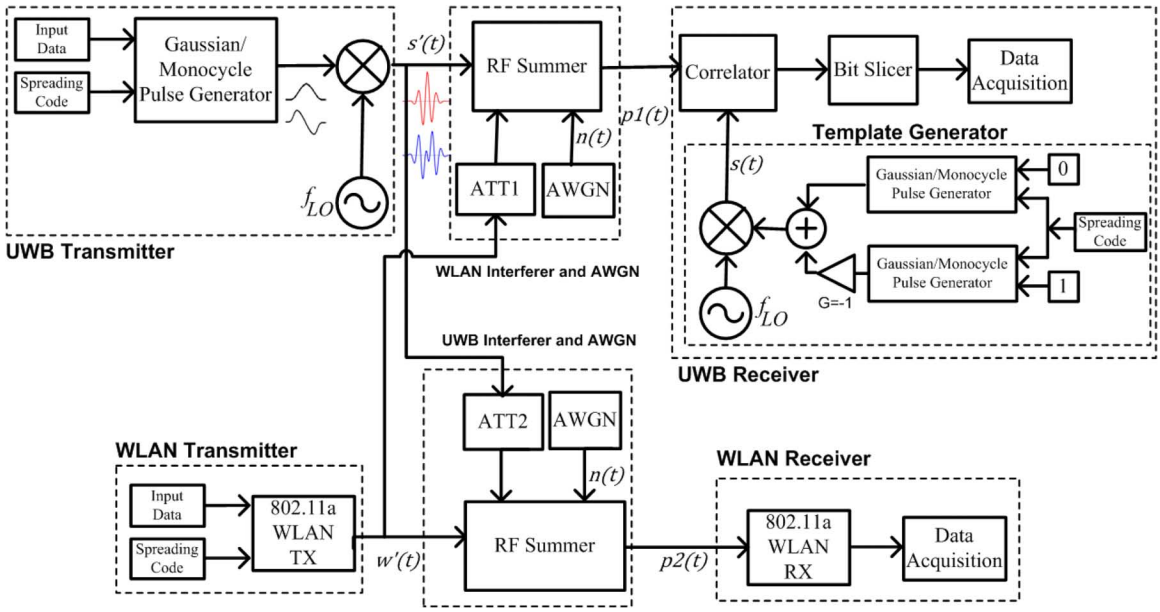

Fig. 3. UWB and 802.11a WLAN coexistence test bench.

NB in-band interference. In this section a comparative analysis is performed to exhibit the resilience of an MM UWB link compared to a link using Modulated Gaussian pulses. Fig. 3 shows both the UWB and 802.11a WLAN systems with mutual interference. The UWB receiver is considered to comprise a matched filter to maximize the signal to noise ratio (SNR) at the sampling instant when the input signal, $p_1(t)$, is corrupted by additive white Gaussian noise (AWGN) [12]. It is clear that a matched filter is an optimal receiver only for detecting signals in the presence of AWGN. Thus, it is realistic to assume that the UWB receiver is suboptimal because the signal is distorted by NB interference and AWGN.

The UWB system interfered by 802.11a WLAN is composed of three sections: 1) the UWB Transmitter, which up-converts the Gaussian or monocycle pulses to generate MG or MM pulses, 2) a WLAN Interferer and AWGN added to the RF path and 3) an UWB Correlator receiver. An attenuator ATT1 is used to model the WLAN transmitted signal at the input of the UWB receiver. The UWB receiver generates a template pulse that is being correlated with the received signal. The "Bit Slicer" then extracts the bit from every 5 pulses. For a more realistic simulation, every bit is represented by 5 pulses $(N_C = 5)$.

The 802.11a WLAN system under consideration is modeled as a single user operating at a data rate of 11 Mbps and is composed of three sections: 1) the WLAN transmitter that implements the WLAN physical layer based on a spreading code and input data 2) the UWB Interferer and AWGN added to the RF path and 3) a WLAN receiver. An attenuator ATT2 is used to model the UWB transmitted signal at the input of the WLAN receiver.

A simplified channel is used for both systems. To consider the jitter of the UWB transmitter and the jitter generation in the UWB receiver clock data recovery, which result in a practically limited null depth, a 10 MHz offset in the WLAN signal frequency has been taken into account. Other parameters are as reported in Table I.

TABLE I
PARAMETERS OF THE UWB AND WLAN SYSTEMS

E_P	UWB pulse energy	0.5 pJ
P_{UWB}	Max. PSD of UWB signal	-41.3 dBm/MHz
f_{UWB}	UWB center frequency	5.30 GHz
BW_{UWB}	-10 dB bandwidth	MG:3.45 GHz MM:4.40 GHz
τ	UWB time scaling	290 ps
T_c	UWB chip period	2 ns
N_C	#UWB pulses/bit	5
P_{WLAN}	WLAN Power	40 mW
f_W	WLAN frequency	5.31 GHz
BW	bandwidth	20 MHz

Advanced Design Systems (ADS) is used to simulate this set-up. The coexistence of the two systems is characterized in terms of bit error rate (BER) vs. SNR for different values of signal to interferer ratio (SIR) and two types of MG and MM pulses as shown in Fig. 4. For reference the BER in the absence of interference is also depicted in Fig. 4. As shown in this figure, using MM pulses gives more than 38 dB better performance compared to using MG pulses. In other words, the proposed UWB pulses significantly mitigate the mutual interference between UWB and 802.11a WLAN systems.

IV. PROPOSED TRANSMITTER CIRCUIT BLOCK DIAGRAM

The block diagram of the proposed transmitter that explains our design is shown in Fig. 5. This architecture uses BPSK modulation, where information is encoded as a low frequency pulse with either positive or negative polarity. The scheme includes five blocks: 1) *Synchronizer* 2) *LFS Generator* 3) *Differential Oscillator* 4) *Differential Mixer* 5) *Output Transformer and Antenna*.

Due to large bandwidth requirement of the UWB antenna, a symmetric differential structure is known to have better performance. In addition, in order to obtain enough LO feed-through

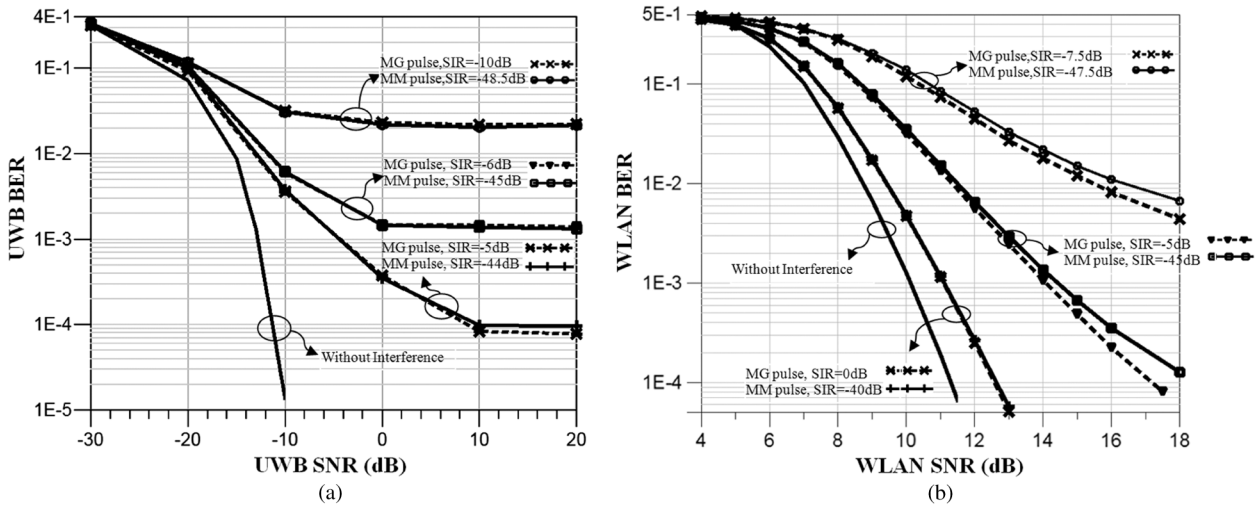

Fig. 4. BER performance of UWB and 802.11a WLAN systems when using a conventional modulated Gaussian (MG) pulse shape and the proposed modulated monocycle (MM) pulse shape. (a) UWB system in presence of WLAN interference. (b) WLAN system in presence of UWB interference.

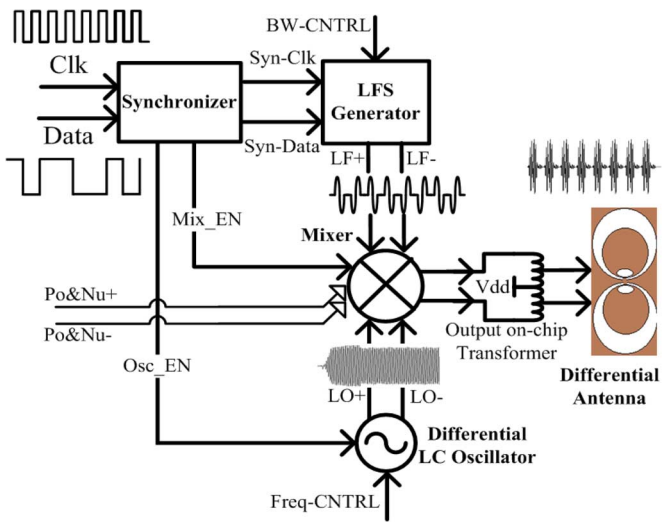

Fig. 5. Proposed transmitter circuit block diagram.

suppression, a fully differential structure is preferred. An efficient on-chip transformer is used for impedance matching as well as minimizing off-chip components.

The frequency of the input clock can vary up to 860 MHz (i.e. 1.16 ns of chip period). The input data rate therefore can be set up to 860 Mb/s. In the *Synchronizer* block, the input data is retimed and aligned with the clock and both together go to the *LFS Generator* block to generate the first derivative of the Gaussian pulses (or monocycle pulses). The *Synchronizer* also generates two signals to enable and disable the *Oscillator* and the *Mixer* and thereby reduce their power consumption.

The input BW_CNTRL of the *LFS Generator* changes the monocycle pulse width, which in turn controls the frequency bandwidth of the LFS. The polarity of the generated monocycle pulse depends on the input data (i.e. Syn_Data in Fig. 5).

The oscillator is a *differential LC oscillator* with a fast start-up time and on/off capability to reduce its power consumption as in [13]. In our implementation however a pre-charging scheme is used to speed up the response. The oscillator frequency can be varied (by setting Freq_CNTRL), which in turn controls the notch frequency of the UWB transmitted pulses. The frequency of the notch can be tuned to match the center frequency of the NB system. The *Differential Mixer* is enabled via the Mix_EN input. The mixer up-converts the input monocycle pulses by the oscillator signal. The up-converted signal in differential current form goes to the *Output Transformer* which is used to deliver the maximum available power to the *Differential Antenna*. In other words, the up-converted signal in the Mixer drives the antenna without a separate power amplifier. The differential antenna used here is based on models used in [14].

A. Synchronizer

The synchronizer circuit is composed of two buffers for input clock and data, a D-flip flop to generate output Syn_Data and also a *Timing Circuit*, as shown in Fig. 6. The input clock is a periodic sinusoidal signal which is readily converted on-chip into a binary square wave using edge sharpening inverters. Osc_EN is triggered at the rising edge of the input clock (see Fig. 6, Osc_EN trace) and will become low when the clock burst ends and the input clock does not appear for 2 ns (see Fig. 6). The oscillator circuit needs around 3.5 ns for settling its amplitude and frequency. Hence, the pulse-width of Mix_EN is shorter than Osc_En by around 3.5 ns as shown in Fig. 6. Syn_Data is used to modulate the LFS to be explained in the next subsection.

This circuit timing scheme allows for most of the IR-UWB signaling standards to be implemented with minimal power consumption.

B. Low Frequency Signal Generator

The LFS Generator, shown in Fig. 7, is composed of two sections: 1) an Adjustable Triangular Pulse Generator (ATPG) and 2) a Pulse Shaping Stage (PSS). The inverted Sync_clk at point "a" and two delayed clocks at points "b" and "c" in the ATPG are buffered and then inputted to two pairs of NAND and NOR

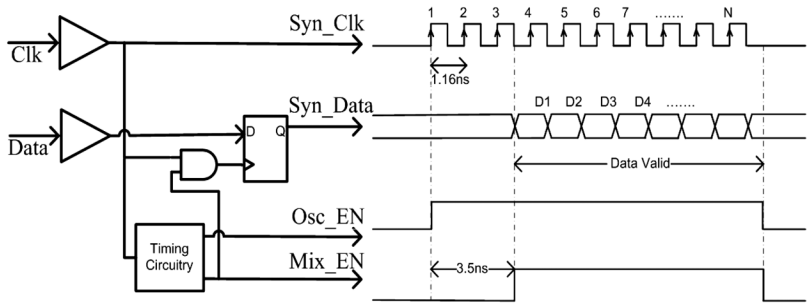

Fig. 6. Synchronizer block diagram and its output signals timing.

gates. The outputs of these are two pairs of rising and falling edge triangular pulses.

The input BW_CNTRL controls the currents that drive the NMOS transistors and in turn the falling edge of the output pulse in the delay cells in the ATPG (refer to points b and c in Fig. 7), thereby controlling the pulsewidth (Δt) of the triangular pulses.

Depending on Syn_Data, the appropriate triangular pulse pairs are connected to two pairs of PMOS and NMOS transistors. As a result, differential monocycle pulses are generated whose polarities are determined by Syn_Data (BPSK modulation). The PMOS and NMOS transistor sizes in the PSS are chosen based on the needed amplification to shape the low frequency waveform. Transistors M1–M4 are used for pulse shaping. When these devices are turned off, the two output DC levels are set by two unity gain OTAs. This is a critical part of the design. The OTAs should be slow enough as not to interfere with the M1–M4 pulse shaping but should be fast enough to bring the DC level to the desired point as soon as the M1–M4 transistors are all turned off. Any transient asymmetry or residual dc offset will affect the final depth of the resulting null in the frequency spectrum. Cpar is the equivalent capacitance at the output, including the input capacitance of the low frequency port of the mixer.

Fig. 8 shows the differential LFS ('LF+'-'LF-') in the time and frequency domains. As shown in this figure, by changing the BW_CNTRL values, it is possible to adjust the pulsewidth of the output pulse from around 0.8 to 1.3 ns in order to change the final UWB bandwidth or to compensate for any process and temperature variability.

C. Oscillator

The choice of the VCO design is between a ring and an LC oscillator. The ring oscillator suffers from process dependency, instability in frequency and high jitter and does not lend itself very well to a phase locked loop for coherent detection. The drawback of the LC VCO is more silicon area and slightly higher power consumption. The used LC oscillator is shown in Fig. 9. The oscillator consists of a newly proposed Gating and Pre_charge Pulse Generator (GPPG), Switching and Initializing Section (SIS), LC VCO and Buffer. The GPPG is used to reduce the start-up time in a similar fashion as has been presented in [13] and [15]. For high rate applications the oscillator is kept continuously "on" but for low pulse rate applications duty cycling the oscillator will save power. GPPG is used in this case for guarantying similar start up phase conditions for each and every UWB pulse. A conventional differential LC oscillator with cross-coupled transistors is used. The inductor, L, used in this circuit uses symmetric spirals, and is 137 μm by 137 μm in size with 4 turns and 7.02 μm trace width and 3.01 μm trace space. The inductor has an inductance of 1.563 nH and a differential quality-factor (Q) of approximately 16 at 5.3 GHz. The total capacitance, C, including the parasitic capacitances of the inductor, cross-coupled devices, current sources and shutdown switch transistors (M1–M6), common-source buffer, metal interconnections and PMOS Varactors (M7, M8) is about 0.517 pF to 0.648 pF when Freq_CNTRL changes between 0–1 V, thereby providing oscillations between 5.0–5.6 GHz.

The settling time of the differential oscillator output waveform, defined as the time needed for the oscillation to reach 90% of its steady-state amplitude is [13]:

$$t_s \approx \frac{Q_{res}}{\omega_0(A_{OL}-1)}\left[2ln\left(\frac{2v_0}{v(0)}-1\right)+1.45\right] \qquad (5)$$

where $A_{OL}=g_mR_P, Q_{res}=R_P\sqrt{C/L}$ and R_P are the open-loop gain, quality factor of the LC tank and equivalent parallel resistance of the tank, respectively. $2v_0$ and $v(0)$ are the steady-state oscillation amplitude and initial condition, respectively.

The settling time can be simplified by substitution of Q_{res}, ω_0 and A_{OL} and approximated for $A_{OL} \gg 1$ as:

$$t_s \approx \frac{C}{g_m}\left[2ln\left(\frac{2v_0}{v(0)}-1\right)+1.45\right] \qquad (6)$$

From (6), settling time t_s can be reduced by decreasing the C, increasing initial condition $v(0)$, or increasing transistor transconductance g_m. Thus, the smallest possible value of the varactors is chosen to cover the required frequency range from 5.0–5.6 GHz. On the other hand, increasing g_m increases the power consumption while increasing $v(0)$ does not have significant effect on the power consumption. Hence, the largest possible value of $v(0)$ and appropriate g_m is chosen. By switching on one side of the differential oscillator before the other (i.e., switching on M1 and M9 before M2 and M10 in Fig. 9), a current I_{inj} initially flows through the inductor which creates a large $v(0)$ as implied by (6).

An inverter chain in the GPPG sharpens the rising edge of the Osc_EN, which is used to turn the current source and oscillator on and off ($\overline{S1}$, S1, SB1, SB2) and generate pre-charge pulses (Pr1, Pr2). Pr1 and Pr2 are added to speed up the charging of the gates of M1 and M2 and thereby of the entire current mirror. The timing signals of the gating and pre-charge waveforms are

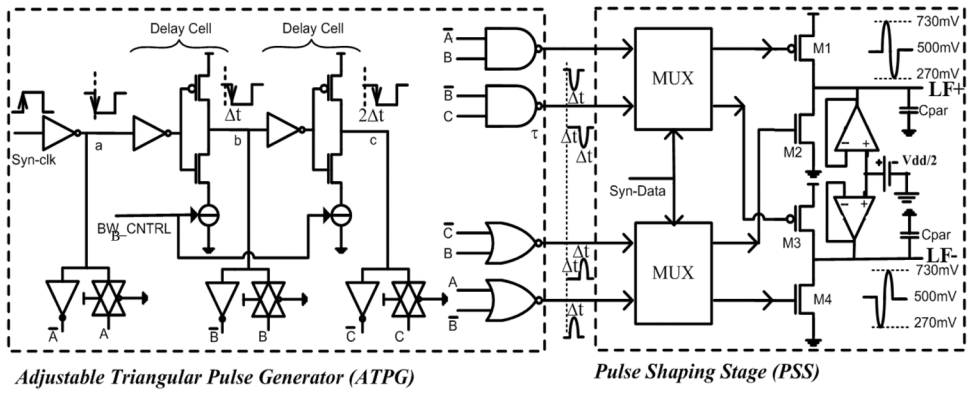

Fig. 7. LFS Generator circuit schematic.

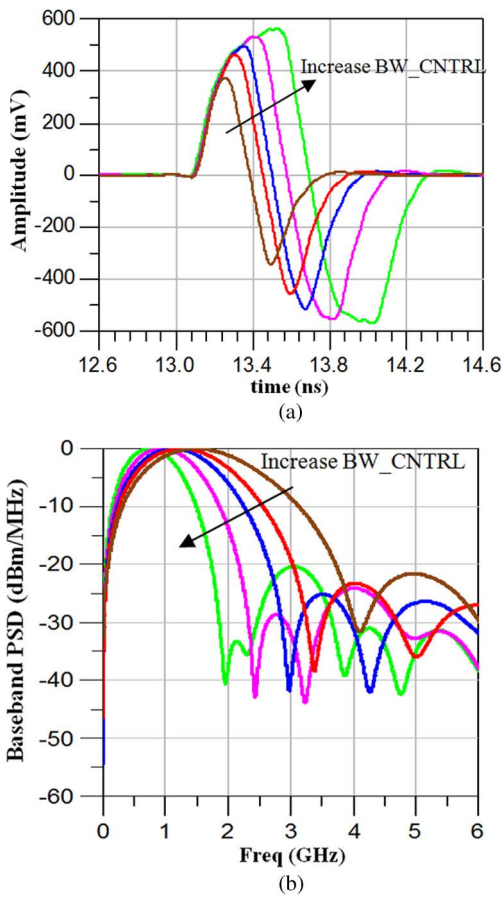

Fig. 8. Differential LFSs (monocycle waveforms) and their normalized spectra when BW_CNTRL and in turn Δt change. (a) Low frequency waveforms (b) their spectra.

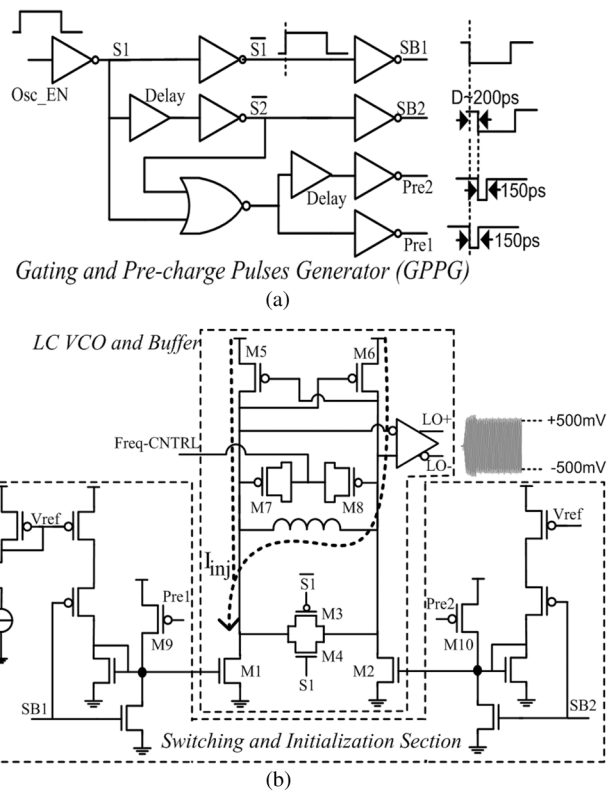

Fig. 9. Circuit schematic of fast start-up oscillator (a) Gating and Pre-charge Pulses Generator (GPPG) (b) switching and Initialization section, LC VCO and Buffer.

illustrated Fig. 9(a). Note that the SB2 and Pre2 signals are delayed around 200 ps with respect to the SB1 and Pre1 signals, respectively (Fig. 9(a)), allowing for sufficient time to generate $I_{\rm inj}$ and in turn $v(0)$. Thus the initial current $I_{\rm inj}$ only flows for a short time. In effect, a current impulse with a short time duration (around 165 ps) and high frequency content is injected through the LC tank, thereby creating a large initial condition $v(0)$ to achieve a short settling time [13], [15]. Transient simulation results of the oscillator are shown in Fig. 10, with different delays (D) between the SB1 and SB2.

As shown in Fig. 10, the settling time is about 1.95 ns, 1.12 ns and 1.3 ns when D is 150 ps, 200 ps and 250 ps, respectively. The injected current impulse $I_{\rm inj}$ in the time and frequency domains is illustrated in Fig. 11. As shown in this plot, $I_{\rm inj}$ has the largest frequency component at 5.3 GHz for $\rm D = 200$ ps compared to that for $\rm D = 150$ ps and $\rm D = 250$ ps, yielding a relatively large initial condition voltage $v(0)$ and in turn shorter settling time t_s. The process variability is not a great concern here since it can be compensated for by the input signal of Freq_CNTRL. As shown in Fig. 12(a), the Freq_CNTRL biasing voltage tunes the oscillator frequency between 5.0–5.6 GHz, thereby providing the flexibility to align the null with the carrier of the existing NB system.

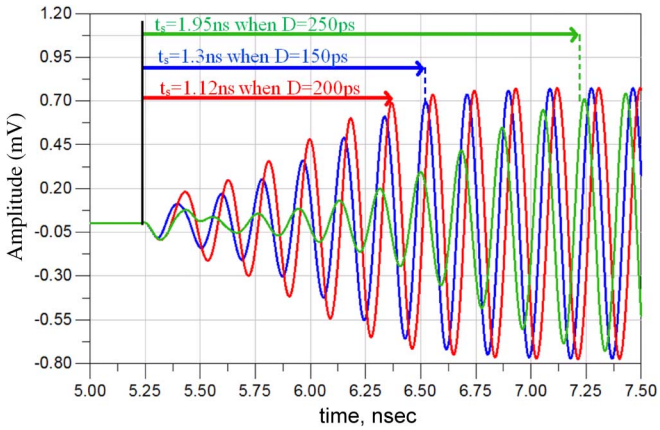

Fig. 10. Oscillator output voltage for D set to 150 ps, 200 ps and 250 ps, which shows the oscillator has the shortest settling time t_s for D = 200 ps.

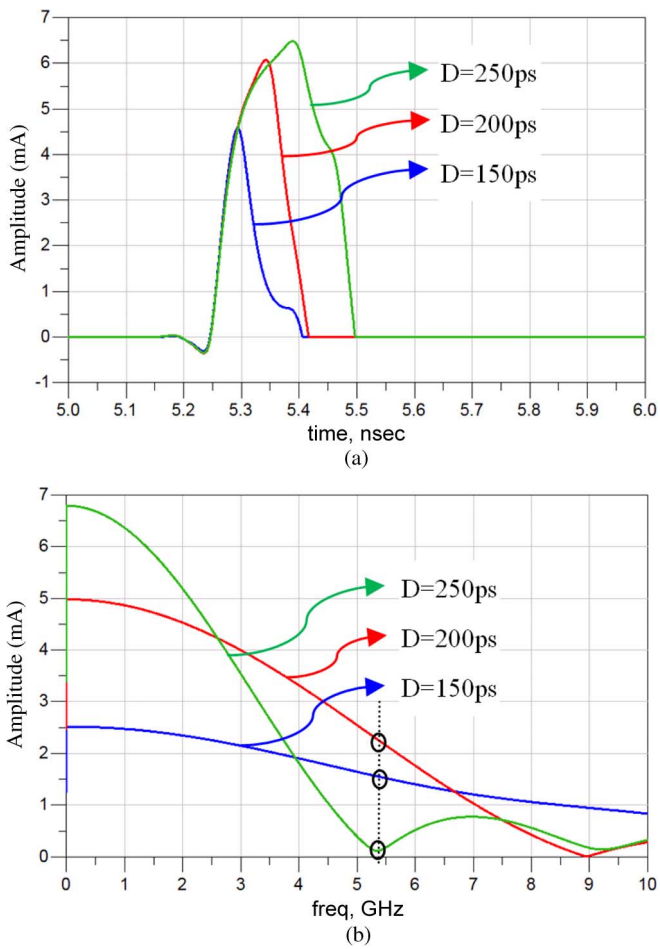

Fig. 11. (a) Current impulse injection for different values of D (delay between SB1 and SB2) in time domain. (b) Spectrum of the current impulse injection, which shows the current injection for D = 200 ps has the largest excitation of the oscillator, yielding a relatively shorter settling time t_s, as shown in Fig. 10.

Even though the symmetry in the oscillator is not as important as it is for the LFS Generator, the LO signal path is balanced to ensure equal amplitudes and 180° phase difference between the differential signals. The VCO frequency versus control voltage and phase noise of the free-running oscillator are plotted in Fig. 12, which shows the tuning range to be between 5.0–5.6 GHz and a relatively low phase noise of −112 dBc/Hz at 1 MHz offset.

D. Up-Conversion Mixer

The trade-offs involved in the design of the up-conversion mixer are, a.o., conversion gain, linearity, LO power, port-to-port isolation, and power consumption. The proposed transmitter uses a direct up-conversion structure. Hence, the LO signal is in band with the output RF signal and cannot be filtered out from the signal at the later stage/before it reaches the antenna. Furthermore, the transmitted signal is supposed to have a null at the LO frequency, thus a mixer with high LO to RF isolation is critical for implementing this transmitter. As shown in Fig. 13, the well-known Gilbert cell base architecture was adopted for the mixer due to its inherent immunity to LO to RF feed-through. The input LFS has a bandwidth of 1.5 GHz to 3 GHz (refer to Fig. 8) and the LO frequency can vary in the range of 5.0–5.6 GHz (refer to Fig. 12). Since the LFS is a large signal (500 mV ± 230 mV), linearity is more important than conversion gain. Although symmetry in the layout mitigates the LO feed-through problem, layout mismatch or PVT variations can increase the LO power present at the RF port. In order to compensate for this, the currents at the left and right sides of the mixer are controlled separately by the Po&Nu+ and Po&Nu- signals. The common mode voltage of these two control signals changes the output power and its differential mode voltage cancels the LO feed-through and in turn increases the null depth. M1 and M2 are biased in deep triode region to increase the linearity.

With a transformer connected at the output (refer to Fig. 14), the simulated result shows a conversion gain of −2 dB and a LO-to-RF and LO-to-IF isolation better than 60 dB for LO frequencies ranging from 5 to 6 GHz due to the differential and symmetrical structure.

E. Output Transformer

The output transformer consists of two two-turn autotransformers to match the differential antenna to the mixer. The linewidth, interwinding spacing, outer winding length and autotransformer spacing are shown in Fig. 13. A high coupling factor k of 0.843 at 5.3 GHz for each autotransformer is realized using stacked windings without ground shield. The mutual coupling factor between two autotransformers is only about 0.035 at 5.3 GHz.

The ADS electromagnetic simulation of the transformer, including parasitic capacitances of the output stage of the mixer and the bondpads is illustrated in Fig. 15 for differential source and load impedances of 400 Ω and 100 Ω, respectively. The transformer compact model [16] was completely extracted and used to simulate the entire transmitter circuit.

V. Post-Layout Simulation Results

The proposed IR-UWB transmitter, designed to be implemented in a standard 90 nm CMOS process, occupies a die area of 0.6 mm^2 including bonding pads, ESD pads and decoupling capacitors. The active circuit area equals only 0.18 mm^2. Post layout simulations using Spectre RF demonstrate a power consumption of 12.13 mW from a 1-V supply voltage for a pulse

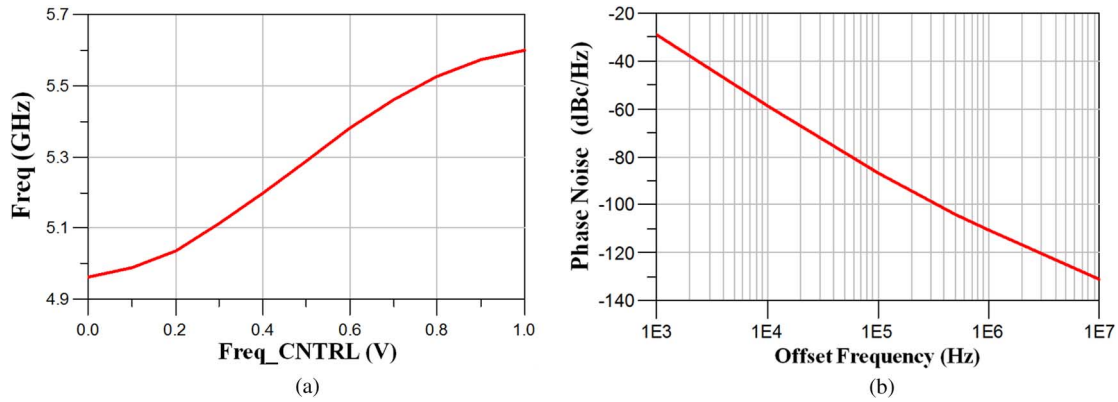

Fig. 12. LC oscillator specifications. (a) Frequency vs. Freq_CNTRL voltage. (b) Phase noise of free-running oscillator.

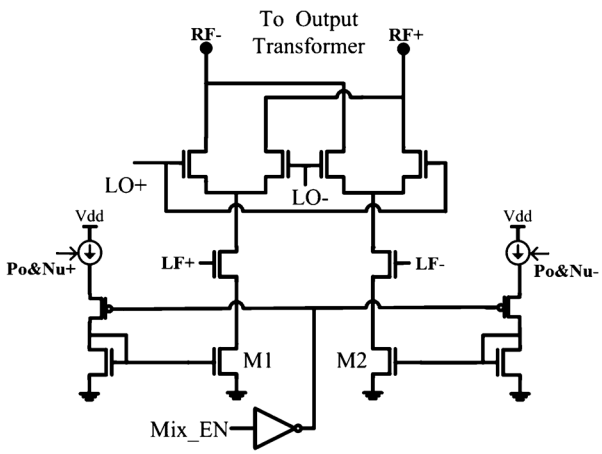

Fig. 13. Circuit schematic of up-conversion mixer.

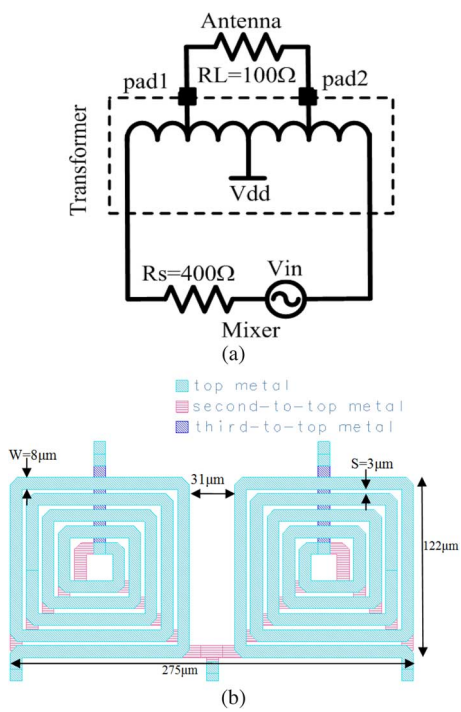

Fig. 14. Differential autotransformer. (a) Schematic. (b) Layout.

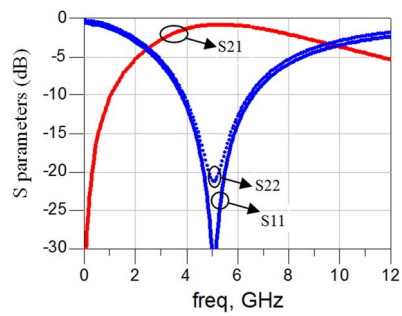

Fig. 15. S-parameters (magnitude only) of the transformer with full load, mixer output, pad, bond-wire and other parasitics included.

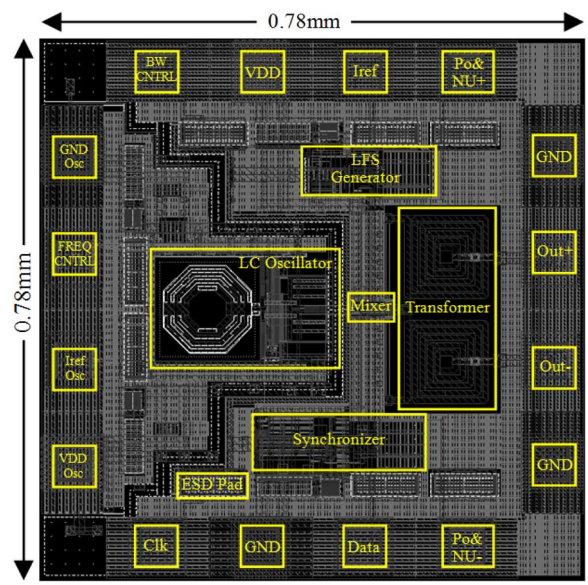

Fig. 16. Transmitter layout.

rate of 860 Mpulse/s. The transmitter layout is shown in Fig. 16. Out of the 16 pads shown in this figure, only the differential output pads and the clock input are of high frequency nature and together with the ground and Vdd pads require special attention. For delivering power, two separate Vdd's have been included, one for the oscillator and the other for the rest of the UWB Tx circuit. Two ground pads are used around the differential output for symmetry. One ground pad is for the oscillator and the remaining ground pad is dedicated to the rest of the circuit. The 85 μm by 87 μm pads and bond-wire equivalent models have been included in the simulatiom. Fig. 17

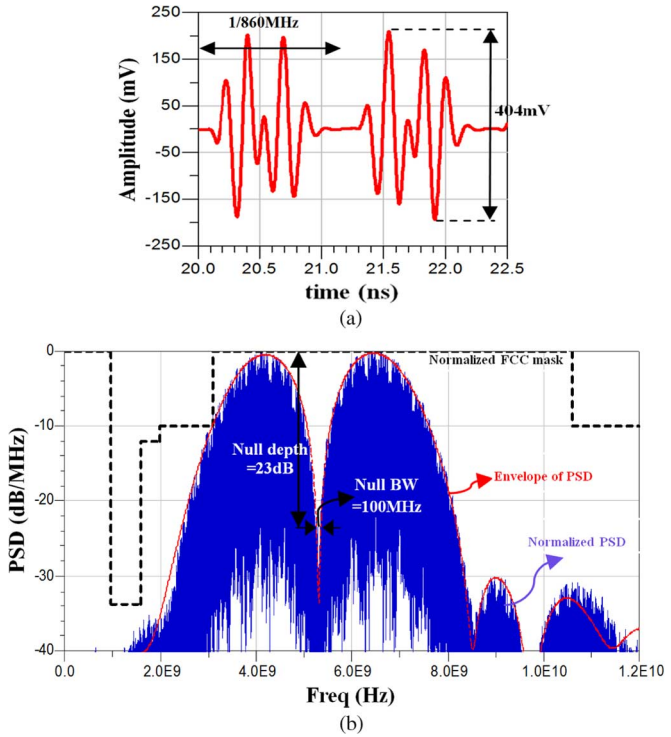

Fig. 17. The transmitted UWB signal. (a) Time domain. (b) Normalized PSD, envelope of normalized PSD and normalized FCC mask.

shows the simulated transmitted UWB signal and its normalized PSD for a pseudo random code length of 1000 and a pulse rate of 860 Mpulse/s when the Freq_CNTRL and BW_CNTRL are set to be 0.5 V. As shown in this figure, the null depth for a null bandwidth of 100 MHz is around 23 dB, which is sufficient for IEEE 802.11a WLAN systems. The spectrum of the pulses has also a −10 dB bandwidth of around 4 GHz and is free from spikes or spectral lines that occur due to LO leakage to the output. The peak-to-peak voltage of the UWB pulse at a 100 Ω load is 404-mV for Po&Nu+/- of 675-mV and can reach to 646-mV when Po&Nu+/- are set to be 1-V at the cost of higher power consumption. On the contrary to meet the FCC requirement the common mode signal applied to the Po&Nu+ and Po&Nu- will efficiently reduce the output power level by scaling all mixer currents as shown in Fig. 13 and Fig. 19. The bond-wire model and interconnection effect between microstrip and bond-wire are taken into account in this simulation.

Fig. 18 shows the envelope of the PSD of the transmitted UWB signal when the BW_CNTRL signal varies between 0 to 1 V and the oscillator frequency is set to be 5.3 GHz. A comparison of Fig. 8(b) with Fig. 18 shows that the PSD of the transmitted signal has a bandwidth that is somewhat smaller than the corresponding LFS bandwidth because of the output transformer and bond-wire frequency responses.

As mentioned before, the output power, Pout, can be controlled by the common mode voltage of the Po&Nu+ and Po&Nu- control signals as shown in Fig. 19.

A. Monte Carlo and Corner Simulations

The LFS shape and oscillator center frequency may vary due to PVT changes. These variations affect the final PSD. A

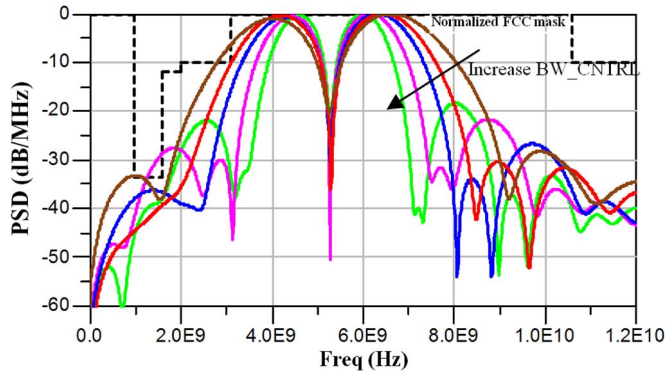

Fig. 18. The normalized envelope of PSD for changes in BW_CNTRL.

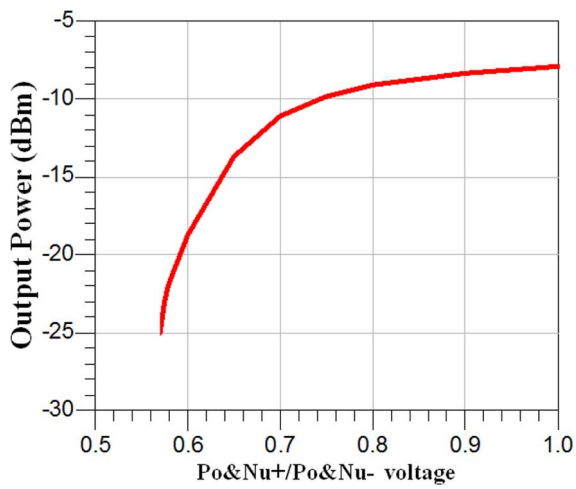

Fig. 19. Output power vs. common mode voltage of the Po&Nu+ and Po&Nu- voltages.

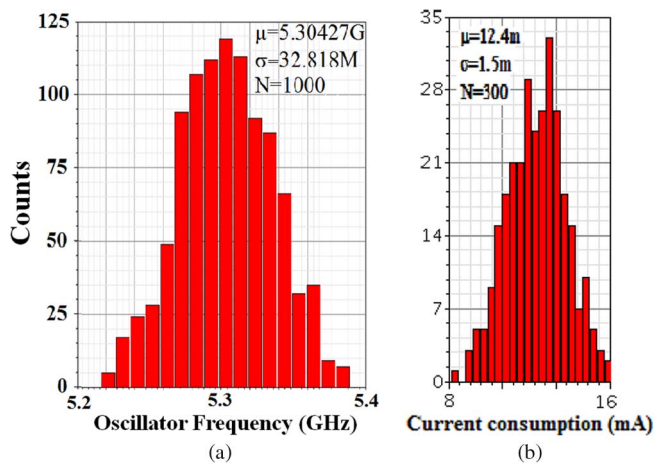

Fig. 20. Oscillator frequency and current consumption from Monte Carlo simulation.

Monte Carlo simulation of the effects of mismatch and process variations for 1000 iterations using Spectre RF shows that the center frequency of the LC oscillator has a standard deviation of only 33 MHz, as shown in Fig. 20(a). Moreover, Fig. 20(b) shows that the average and standard deviation values of the current consumption in Monte Carlo simulation are 12.4 mA and 1.5 mA, respectively. In addition, an 1000 iteration Monte Carlo analysis has been run on the LFS generator and the

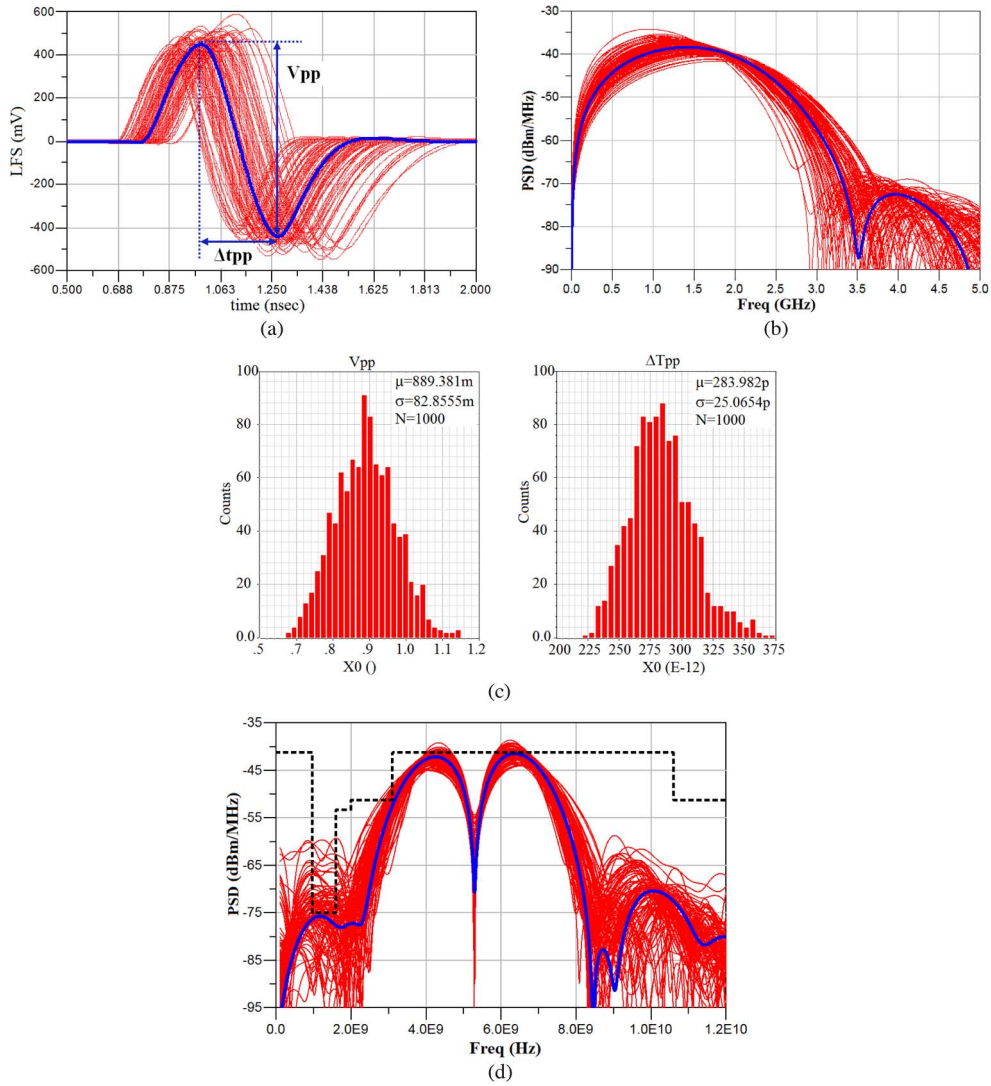

Fig. 21. Monte Carlo analysis of the LFS generator and the transmitted signal. (a) and (b) LFS in time and frequency domains, (c) Vpp and $\Delta\mathrm{tpp}$, (d) PSD of transmitted signal.

results are depicted in Fig. 21. The statistical variations result in a change in the spectrum occupancy as shown in Fig. 21(b). Both figures in the time and frequency domains show quite reasonable statistical variations as shown in Figs. 21(a) and (b). This figure shows Vpp variations and $\Delta\mathrm{tpp}$ which are defined in Fig. 21(a). The low frequency signal after upconversion exhibits a spectrum as shown in 21(d).

Corner simulations are performed in five modes (SS, TT, FF, SF and FS) at the nominal supply voltage of 1 V, a temperature of 27°C, and Freq_CNTRL and BW_CNTRL set to 0.5 V. The PSD of the output signals are plotted in Fig. 22. In this figure the dashed pink and solid red graphs show the PSDs in the typical and the corresponding corner, respectively, whereas the blue one depicts the PSDs after frequency and bandwidth tuning (refer to Fig. 12(a) and Fig. 18). As can be seen from Fig. 22, these variations in center frequency and final PSD can be compensated for by controlling Freq_CNTRL and BW_Control for all corners. Moreover, Fig. 23 depicts the output PSD and current consumption when the supply voltage and temperature vary between 0.9–1.1 V and 0–75°C.

B. Power Consumption

The circuit is fully differential and the output pulses have a peak-to-peak voltage amplitude of 404 mV. The total power consumption of all the circuits and including ESD pads is only 12.13 mW, which implies an energy/pulse and an energy/pulse normalized to the output voltage amplitude of 14.4 pJ/pulse and 35.7 pJ/(pulse-V) at 860 Mpulse/s for a supply voltage of 1 V.

Table II summarizes the circuit's characteristics in comparison with other works [8], [17]–[24]. To the best of the authors' knowledge, there are only two reports that present the design of an UWB pulse generator circuit whose PSD includes a null [8], [24]. Hence in Table II, this work is being compared with other works, and organized in two groups: 1) the works in [17]–[23] that do not have a null in their PSD 2) the works in [8] and [24] that have a null in the PSD. As shown in this table, our work offers an UWB pulse generator with tunability in PSD at a low energy consumption of 14.4 pJ/pulse which includes a null in the PSD with 23 dB depth for 100 MHz null

TABLE II
PERFORMANCE SUMMARY OF PROPOSED GENERATOR AND COMPARISON WITH PREVIOUS STUDIES (WITH AND WITHOUT NULL IN PSD)

	Group 1: without null in PSD							Group 2: with null in PSD		
Ref.	[17]	[18]	[19]	[20]	[21]^P	[22]^P	[23]^P	[8]	[24]	This work
Vpp (mV)	530	91	310	1400	600	240	500	60	2	404
Vdd (V)	1.2	0.9	0.5-1.2^T	1.2	1.2	1.2	1	1	N/A	1
Pulse width (ns)	1.8	1.1-2.6^T	1.9-15^T	0.83	1.8	1	1.5	2.5	0.6	0.9-1.5^T
-10 dB BW (GHz)	2.9	0.5-1.4^T	0.1-0.8^T	7.5	0.82	1.2	1.3	3.5	4.8	2.4-4.6^T
Data Rate (Mb/s)	550	50	10	1200	1	100	0.1	400	125	860
Center Freq (GHz)	3.5	3.1-5^T	0.3-4.4^T	5.7	5.6	3.2-4.1^T	3.5-4.5	6	4.9	5.0-5.6^T
Null Depth^N	×	×	×	×	×	×	×	25 dB	4 dB	23 dB
CMOS (nm)	130	65	130	130	65	130	90	90	180	90
Power Cons (mW)	0.031	0.6	0.16	12	0.025	2.2	0.008	17^E	N/A	12.13
Ep (/pulse)	26.5 pJ	12 pJ	32 pJ	10 pJ	25 pJ	22 pJ	80 pJ	42.5^E pJ	N/A	14.4 pJ
Normalized Ep (/pulse-V)	50 pJ	$>$ 64 pJ	103 pJ	7.1 pJ	42 pJ	92 pJ	160 pJ	708^E pJ	N/A	35.7 pJ
Die Area (mm^2)	0.1^C	0.032^C	0.004^C	0.54	N/A	0.32^C	0.42^C	1.9	0.49	0.18*
Modulation	OOK	PPM/BPSK	OOK	OOK	OOK	OOK	OOK	BPSK	OOK	BPSK

^{P}Only TX section ^{T}Tunable ^{N}100 MHz null bandwidth ^{E}Excluding the output buffer ^{C}Core area *Active and die areas: 0.18 mm^2 and 0.6 mm^2.

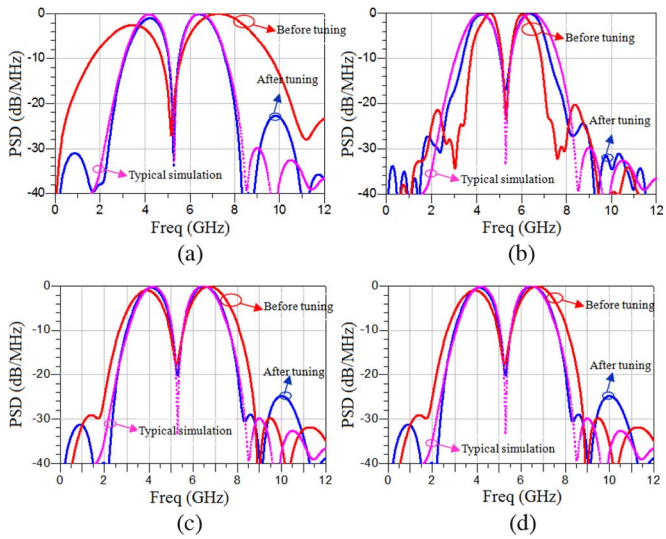

Fig. 22. The normalized Output PSD in corners before and after frequency and bandwidth tuning. (a) FF. (b) SS. (c) FS. (d) SF.

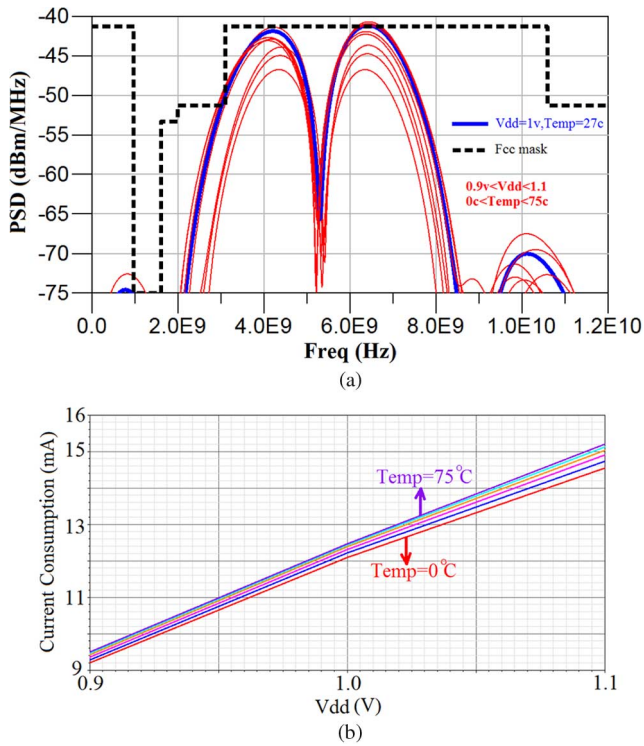

Fig. 23. Output PSD and current consumption when Vdd and Temperature vary between 0.9–1.1 V and 0–75° C, respectively.

bandwidth. It is also more energy efficient than all of the other designs, except [20], if the energy consumption is normalized with respect to the output peak-to-peak voltage. Furthermore, the proposed circuit has a relatively small chip area compared to other works.

VI. CONCLUSIONS

In this paper we proposed a new UWB pulse generator to be implemented in 90 nm standard CMOS technology, which can significantly improve coexistence of UWB systems with other NB systems like IEEE802.11.a WLAN. To generate its UWB pulse shape, we used an up-converted Gaussian monocycle, which results in an adjustable null in the transmitted frequency spectrum depending on the up-converting frequency. System simulation results show that both UWB and WLAN systems have noticeably improved performance when using the proposed pulse compared to when using conventional modulated Gaussian pulses in an UWB system without reduction in the throughput of the UWB system. The proposed fully differential transmitter circuit consists of an LFS Generator, an LC oscillator and a mixer, whose output directly drives the antenna using a matching on-chip transformer. Two control signals change the bandwidth and center frequency of the transmitted PSD to align it with the NB frequency and fulfill PVT requirements. A fast start-up circuit is used in the LC oscillator using current pulse injection, which, together with the mixer, is duty cycled to reduce the power consumption. Post-layout simulation results show a null depth of 23 dB for a null bandwidth of 100 MHz, which is enough for almost all NB systems. The energy/pulse normalized for output voltage amplitude is 35.7 pJ/(pulse-V) from a

1-V supply for 860 Mpulse/s with an active circuit area of only 0.18 mm^2.

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