Low-Dropout Voltage Source: An Alternative Approach for Low-Dropout Voltage Regulators

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***Abstract*— In this paper, a high-order temperature-compensated 0.6 V low-dropout voltage source (LDVS) is realized in standard 0.13-µm CMOS technology. The LDVS operates at supply voltages down to 0.75 V and consumes only 39µA while providing up to 100 mA of load current. Gate-to-channel capacitances of MOSFETs (MOSCAPs) are employed to integrate the capacitors, reducing chip area and enabling integration in any inexpensive CMOS technology. The regulation loop is compensated using a combined pole-splitting and feedforward technique, which results in stable operation from no-load to 100 mA of full load current. A temperature-dependent current-driven voltage generator is proposed to suppress the line voltage sensitivity of the LDVS. To further improve line regulation, a line voltage compensation circuit is introduced, which lowers the line sensitivity by about three times down to 0.54%/V. With a 1 V supply voltage and no output filtering capacitor, the mean power-supply rejection is −51 dB and −24 dB for 1 kHz and 10 MHz, respectively. The proposed LDVS requires no start-up circuit. The 0.1% start-up settling time is 73 µs with a 0.8 V supply voltage and a 1mA load current. In the temperature range of −25 °C to +85 °C, it demonstrates a maximum temperature drift of only 32 ppm/°C.**

***Index Terms*— Bandgap reference, line voltage compensation, low-dropout (LDO) regulator, MOSFET-only, start-up.**

I. Introduction

THE architecture of a typical electronic micro-system consists of several on-chip voltage sources for regulation and comparison [1]. These voltage sources should be independent of the load current (I_{Load}), process variation, voltage supply (V_{DD}) and temperature. A high-impedance bandgap reference can be designed to be insensitive to temperature. Nonetheless, its high-impedance output node does not remain stable in a harsh and noisy environment. Bandgap references should be followed by a low-dropout regulator (LDO) to drive a load [2]. Conceptually, an LDO amplifies/buffers the output of a bandgap reference within a regulation loop. However, the high-impedance bandgap reference is still vulnerable to transients. Also, the reference and LDO should both be optimized for good performance [3].

An alternative is the idea of a low-dropout voltage source (LDVS), depicted in Fig. 1. In this topology, the negative input terminal of the error amplifier is connected to a complementary-to-absolute-temperature (CTAT) voltage source. In contrast with an LDO, the temperature dependence of the output voltage (V_{REF}) is directly compensated at the output by adding an extra proportional-to-absolute-temperature (PTAT) current source. Assuming that the DC gain of the amplifier is high, V_{REF} is given by [4]:

$$V_{REF} = (1 + R_2/R_1)V_{CTAT} + R_2 I_{PTAT}. \quad (1)$$

Therefore, if carefully designed, a buffered yet tunable voltage source (depending on R_2/R_1) is achieved. This configuration has a number of advantages compared with the combination of a reference and an LDO. Foremost, no high-impedance bandgap reference is used in this circuit. High-impedance nodes are vulnerable to load current transients and also sensitive to supply-coupled noise. Another advantage of the proposed topology is its low temperature drift. For a classical LDO, there is always a residual temperature drift associated with random and systematic offset voltages referred to the output. These types of non-idealities can be considerably compensated for in a circuit which minimizes the errors by means of a negative-feedback control loop.

II. Temperature Compensation Design Considerations

The temperature drift of V_{REF} in Fig. 1 will be minimized if the temperature behaviors of I_{PTAT} and V_{CTAT} are contrary to each other.The threshold voltage of *n*MOS and *p*MOS devices ($V_{TH,n}$ and $V_{TH,p}$), are predominantly CTAT, according to [5]:

$$V_{TH}(T) = V_{TH}(T_0) - \alpha(T - T_0) \quad (2)$$

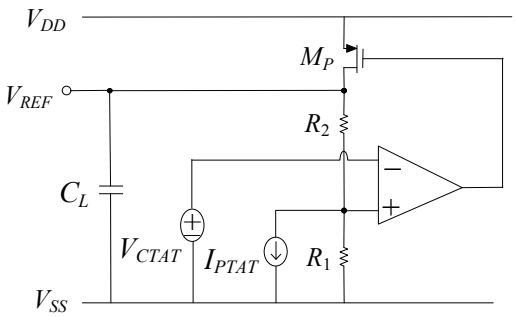

Fig. 1. The proposed low-dropout voltage source.

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where $V_{TH}(T_0)$ is the threshold voltage at T_0 where α has been evaluated. The thermal voltage, $V_T = kT/q$ (k is Boltzmann's constant and q is the electron charge) is, on the other hand, PTAT. Based on these temperature behaviors, the following sub-sections analyze the design considerations which help to minimize the temperature dependence of the proposed LDVS.

A. PTAT Current Generator

The drain current of a *p*MOS device operating in weak-inversion (saturation or triode) is given as follows:

$$I = \left(\frac{W}{L}\right) I_0 \exp\left(\frac{V_{SG}}{NV_T}\right)\left[1 - \exp\left(-\frac{V_{SD}}{V_T}\right)\right] \quad (3)$$

where (W/L) is the transistor aspect ratio; V_{SG} and V_{SD} are the source-gate and source-drain voltages, respectively; I_0 is a temperature-related parameter of the employed technology; and $N > 1$ is the sub-threshold slope factor. Fig. 2 shows a PTAT current generator based on MOS devices operating in the weak-inversion region [6]. In this circuit, the sub-threshold devices M_{P3} and M_{P4} generate a PTAT current that is equal to $I_1 = (V_{SG,P3} - V_{SG,P4}) / R_3$. Combining this equation and (3) for M_{P3} and M_{P4}, the PTAT current I_1 is related to V_T as:

$$I_1 = \frac{NV_T}{R_3}\left\langle \ln\left[\frac{(W/L)_{P1}}{(W/L)_{P2}}\frac{(W/L)_{P4}}{(W/L)_{P3}}\right] - \ln\left\{1 - \left[\frac{(W/L)_{P4} I_0}{I_2}\right]^N\right\}\right\rangle + \frac{NV_T}{R_3}\ln\left[1 - \exp\left(-\frac{V_{DD} - V_{GS,P2}}{V_T}\right)\right] \quad (4)$$

where $I_2 = (W/L)_{P2}/(W/L)_{P1} \times I_1$. This expression shows that any mismatch between M_{P1} and M_{P2}, or between M_{P3} and M_{P4} contributes only slightly to the absolute value of I_1 while the nature of the generated current still remains PTAT. The mismatch can therefore be readily compensated by trimming.

As typically $V_{DD} - V_{GS,P2} >> V_T$, $I_2 >> (W/L)_{P4} I_0$, and $V_{GS,P2} \approx V_{TH,n}$ for small bias currents, I_1 can be approximated as (5):

$$I_1 \approx \frac{NV_T}{R_3}\left\{\ln\left[\frac{(W/L)_{P1}}{(W/L)_{P2}}\frac{(W/L)_{P4}}{(W/L)_{P3}}\right] - \exp\left(\frac{V_{TH,n} - V_{DD}}{V_T}\right)\right\}. \quad (5)$$

The exponential V_{DD}-dependent term in (5) indicates a residual supply dependence in the generated PTAT current I_1. A solution to this issue is addressed in the following section.

B. Line Voltage Compensation Circuit

Line regulation can be improved by using a line voltage compensation mechanism for the generated PTAT current. In Fig. 3, the supply-dependent current I_{L1} is so small that the gate-source voltage of M_{L1} is almost equal to $V_{TH,p}$. Therefore:

$$I_{L1} = \frac{V_{DD} - V_{GS,L1}}{R_4} \approx \frac{V_{DD}}{R_4} - \frac{V_{TH,p}}{R_4}. \quad (6)$$

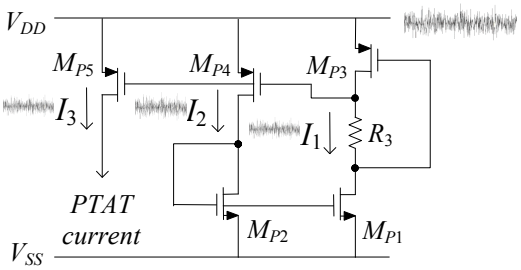

Fig. 2. Schematic of the employed PTAT current generator.

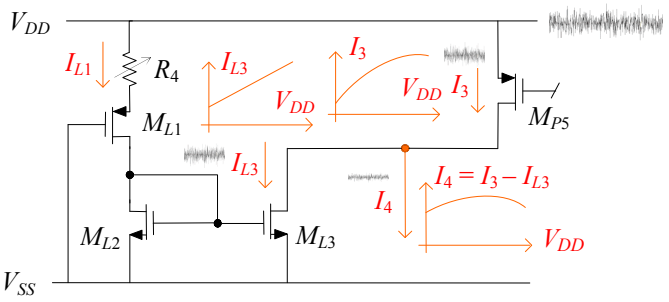

Fig. 3. The proposed line voltage compensation circuit (R_4 can be trimmed).

The proposed compensation scheme subtracts a scaled mirror of this current (I_{L3}) from a weighted copy of the original PTAT current (I_3) (see Fig. 3). The resulting PTAT current, i.e. $I_4 = I_3 - I_{L3}$, is obtained from:

$$I_4 = \frac{NV_T}{R_3}\frac{(W/L)_{P5}}{(W/L)_{P3}}\ln\left[\frac{(W/L)_{P1}}{(W/L)_{P2}}\frac{(W/L)_{P4}}{(W/L)_{P3}}\right] + \frac{(W/L)_{L3}}{(W/L)_{L2}}\frac{V_{TH,p}}{R_4} - \frac{NV_T}{R_3}\frac{(W/L)_{P5}}{(W/L)_{P3}}\exp\left(\frac{V_{TH,n} - V_{DD}}{V_T}\right) - \frac{(W/L)_{L3}}{(W/L)_{L2}}\frac{V_{DD}}{R_4}. \quad (7)$$

Since the behavior of the last two terms in (7) is contrary to V_{DD}, the supply dependence of I_4 is very limited. This line voltage compensation mechanism can be practically trimmed over process corners by using R_4 (see Fig. 3). In the fabricated LVDS, the trimming range spans from 100 kΩ to 140 kΩ.

C. CTAT Voltage Generator

Fig. 4 depicts the proposed current-driven CTAT circuit as an alternative to a voltage-driven design scheme [7]. Let us suppose that M_{C1} is in strong-inversion triode while all other devices are in strong-inversion saturation. Regardless of the temperature dependence of the biasing current $I_{PTAT,C}$ (i.e. PTAT, CTAT, or constant), the devices can be sized such that the CTAT output (V_{CTAT}) is merely a function of $V_{TH,n}$. For a PTAT current source as used in this design, the square-law I-V model for the transistors results in:

$$V_{CTAT} = \sqrt{\frac{I_{PTAT,C}}{\mu_n C_{ox}}} \times \left[(1 - \sqrt{\gamma})\sqrt{\frac{1}{(W/L)_{C1}} + \frac{1}{2(W/L)_{C2}}} + (3 + \sqrt{\gamma})\sqrt{\frac{1}{2(W/L)_{C2}}}\right] + \sqrt{\gamma} V_{TH,n} \quad (8)$$

where $\gamma = (W/L)_{C3}/(W/L)_{C4}$. This expression shows that if:

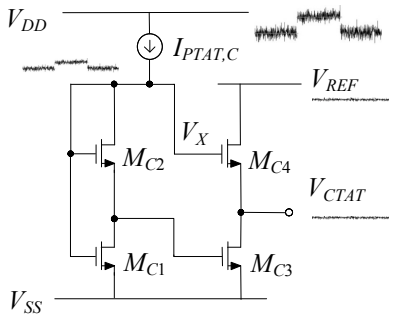

Fig. 4. The proposed CTAT voltage generator circuit.

$$\sqrt{\gamma}=\frac{\sqrt{\frac{1}{(W/L)_{C1}}+\frac{1}{2(W/L)_{C2}}}+3\sqrt{\frac{1}{2(W/L)_{C2}}}}{\sqrt{\frac{1}{(W/L)_{C1}}+\frac{1}{2(W/L)_{C2}}}-\sqrt{\frac{1}{2(W/L)_{C2}}}}, \quad (9)$$

the output voltage will be independent of $I_{PTAT,C}$ and can be expressed as:

$$V_{CTAT}=\sqrt{\gamma}V_{TH,n}. \quad (10)$$

When using long-channel devices, (8) to (10) describe the CTAT output voltage in a sufficiently accurate manner, at least to first order. Nonetheless, any residual model error can be readily compensated for by fine tuning the device sizes during simulations. To satisfy (9), we selected $(W/L)_{C2}$ = 12$(W/L)_{C1}$ and $(W/L)_{C3}$ = 4$(W/L)_{C4}$. Unlike a voltage-driven design scheme [4,7], the added high-output impedance $I_{PTAT,C}$ shields the sensitive nodes of this circuit from V_{DD}. The supply variations are thus highly attenuated when transferred from V_{DD} to V_{CTAT}. To further protect V_{CTAT} from V_{DD}, the second stage is biased directly from V_{REF} rather than V_{DD}. A better line regulation and power-supply rejection is therefore resulted. The biasing current of the second stage is defined by the first stage and is not affected by V_{REF} transients. This stable bias current causes V_{CTAT} to be robust against V_{REF} variations.

III. LDVS Complete Implementation

The circuit diagram of the proposed LDVS is shown in Fig. 5 (see also Fig. 1). A two-stage error amplifier with a PTAT tail current ($I_{PTAT,i}$) is employed. The second stage of the amplifier is push-pull to charge and discharge the gate of the large pass device M_P efficiently. The frequency compensation network consists of C_{C1}, C_{C2}, C_{C3} and R_C. Capacitor C_{C1} provides pole-splitting at the nodes V_X (corresponding to the dominant pole) and V_{REF} (corresponding to a non-dominant pole) [8]. The associated right-half-plane (RHP) zero is moved to the left-half-plane (LHP) by means of R_C in series with C_{C1}. Capacitor C_{C2} controls the damping factor of the non-dominant poles, thereby improving the gain margin [1,8]. Capacitor C_{C3} generates an LHP zero and adds more phase lead for stable operation. The feedforward stage between V_{in} and V_P (comprised of the input stage and M_{o2}-M_{o4}) operates in parallel with the main stage (comprised of the input stage and M_{o1}-M_{o3}-M_{o5}-M_{o6}). This feedforward stage adds another LHP zero for better stability [8].

The generated I_{PTAT} and V_{CTAT} cancel out each other's temperature dependency, thereby resulting in a temperature-insensitive V_{REF}. By substituting a weighed combination of (7) and (10) into (1) (by considering that I_{PTAT} =[$(W/L)_{P10}$/$(W/L)_{P9}$] × I_4) and neglecting the residual supply effect, V_{REF} becomes:

$$V_{REF}=\left(1+\frac{R_2}{R_1}\right)\left(\sqrt{\gamma}V_{TH,n}+V_{OS}\right)+\frac{R_2}{R_3}NK_{PTAT}V_T \quad (11)$$

where V_{OS} is the input-referred offset of the error amplifier and

$$K_{PTAT}=\frac{(W/L)_{P10}}{(W/L)_{P9}}\frac{(W/L)_{P5}}{(W/L)_{P3}}\ln\left[\frac{(W/L)_{P1}}{(W/L)_{P2}}\frac{(W/L)_{P4}}{(W/L)_{P3}}\right]. \quad (12)$$

The resistors' ratios R_2/R_1 and R_2/R_3 are temperature-independent as they are realized by the same resistor types. Ideally, if V_{OS} is temperature-independent, zero-temperature-coefficient (ZTC)output is achieved for all temperatures when:

$$\left(1+\frac{R_2}{R_1}\right)\sqrt{\gamma}\frac{\partial}{\partial T}V_{TH,n}+\frac{R_2}{R_3}NK_{PTAT}\frac{\partial}{\partial T}V_T=0$$
$$\Rightarrow \quad \frac{R_3}{R_1||R_2}=K_{PTAT}\frac{Nk}{q}\frac{1}{\alpha\sqrt{\gamma}}. \quad (13)$$

The resulting V_{REF} is obtained from:

$$V_{REF}=\left(1+\frac{R_2}{R_1}\right)\left[\sqrt{\gamma}V_{TH,n}(T_0)+\alpha T_0+V_{OS}\right]. \quad (14)$$

Equation (14) shows that V_{REF} is ideally a temperature-insensitive voltage reference that can be adjusted by the R_2/R_1 ratio. According to (13), the temperature sensitivity of V_{REF} can also be cancelled out by tuning R_3 and/or γ. In practice, however, there are a number of imperfections that cause residual temperature sensitivity. For instance, to derive (14) high order terms/effects that are temperature-dependent such as short channel effects are neglected. Moreover, the addition of the required building blocks (error amplifier, bias network, pass device) adds more temperature drift to the high-order temperature curve achieved.

Measurements confirm that the LDVS in Fig. 5 does not require any dedicated start-up circuit. Start-up circuits can introduce design difficulties such as leakage current, and power up issues during both start-up and normal operation [9]. In the proposed LDVS, as soon as the power supply is connected, the PTAT current generation circuit turns on and, in turn, biases all other blocks, which causes the entire LDVS to power up properly.

MOS devices and poly resistors are the only elements used to realize the circuit in Fig. 5. MOSCAPs are area-efficient and are compatible with every technology. Unlike the majority of analog circuits, voltage regulators are inherently nonlinear as the location of the poles and zeros depend strongly on the load current. MOSCAP nonlinearity is therefore not detrimental to an already nonlinear LDVS. In this design, C_L, C_{C1}, C_{C2} and C_{C3} are realized by simple MOS capacitors which help to save area (by about 10% in chip area in this design).

IV. Experimental Results

Fig. 6 depicts a micrograph of the LDVS implemented in IBM's 130-nm CMOS technology. Redundant pins have been assigned to calibrate and test the circuit. The resistors R_1 and R_2 are trimmed (from 630 kΩ to 850 kΩ and from 220 kΩ to 450 kΩ, respectively) to fine tune the absolute value of V_{REF} and its temperature drift.This trimming has a negligible impact (e.g. below 1%) on the dynamic characteristics of the LDVS.

Fig. 7 shows the start-up settling of V_{CTAT} and V_{REF} for a 0.8 V supply voltage and a 1 mA load current. The mean settling time among the tested samples is 73 µs. By switching on the proposed line voltage compensation circuit, the no-load line regulation is reduced from +1.4%/V to –0.54%/V (for supply voltages between 0.8 V and 1.5 V). The mean power-supply rejection is −51 dB for 1 kHz and −24 dB for 10 MHz respectively, for a 1 V supply voltage and 0 mA load current.

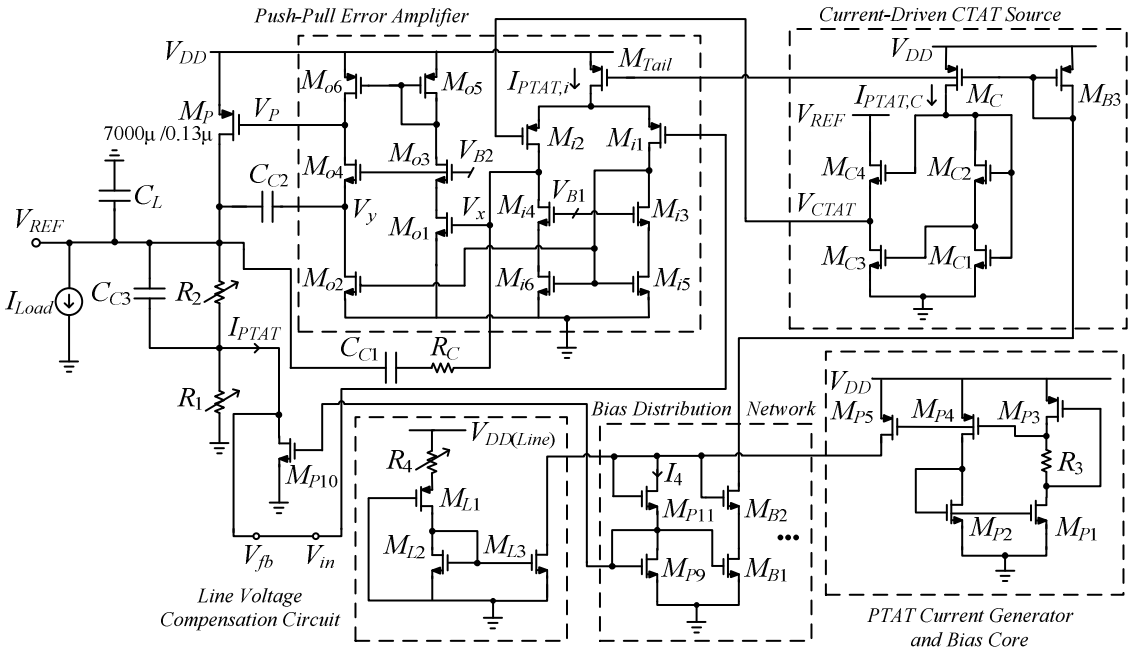

Fig. 5. The proposed voltage source in detail (R_1, R_2 and R_4 can be trimmed to compensate for process variations).

The measured current drawn by the LDVS from a 1 V supply is 39.1 µA for a 1 mA load current at 25°C temperature. The current reaches 43.2 µA at 85°C. The error amplifier consumes more than half this current. Without any filtering capacitor, the measured total noise between 0.1kHz and 10 kHz is 56 µV for load currents higher than 1 mA. For the same bandwidth, the noise reaches 97 µV when decreasing the load current to 0 µA.

Transient load/line responses were tested to verify the performance under various conditions. The load capacitor consists of an integrated MOSCAP (of about 3 pF at V_{REF} = 0.6V) and a parasitic capacitor of about 15 pF. The worst-case 1% settling time of the load response was measured at V_{DD} = 0.75 V, when a pulsed load current steps from 0 A to 100 mA and vice versa with a rise/fall time of 0.1µs. The settling times are 6.05 µs and 1.55 µs and the overshoot and undershoot are 92 mV and 270 mV, respectively. The overshoot and undershoot reduce to 73 mV and 142 mV, respectively, when the rise/fall time is increased to 1 µs. Increasing the size of the load capacitor also improves the overshoot/undershoot at the cost of more area. For a 0.1 µs rise/fall time, the overshoot and undershoot are reduced to 56 mV and 114 mV, respectively, when using a 100 pF capacitor. The worst-case 1% settling times of the line response are 12.3 µs and 9.4 µs, respectively. This is observed at zero load current when V_{DD} switches from 0.75 V to 1.50 V and vice versa with a rise/fall time of 0.2 µs. For a 100 mA load current, the 1% settling time reduce to 2.85 µs and 5.15 µs, respectively, for a V_{DD} transient with a rise/fall time of 2 µs. Fig. 8 shows the no-load reference voltage dependence on temperature for different supply voltages. The measured temperature coefficients at 0.75 V and 1.50 V are 26 ppm/°C and 32 ppm/°C, respectively, when the temperature changes from −25 °C to +85 °C. A comparison

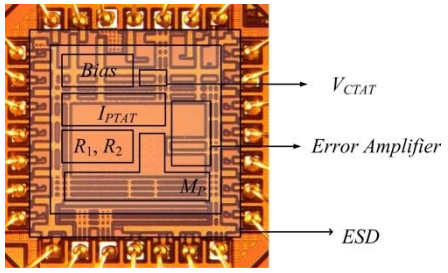

Fig. 6. Chip micrograph.

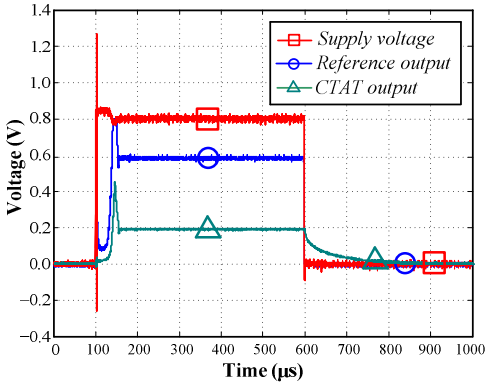

Fig. 7. Measured start-up settling response (V_{DD} = 0.8 V and I_{Load} = 1 mA).

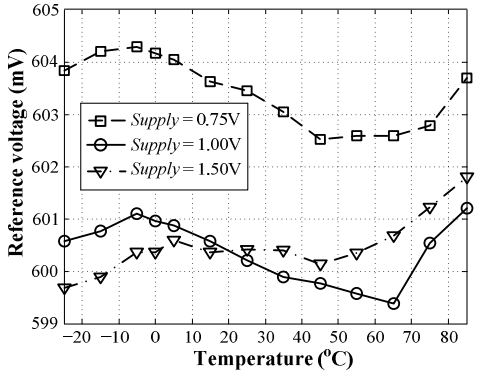

Fig. 8. Measured no-load temperature dependence.

TABLE I. COMPARISON OF THE PROPOSED WORK WITH PRIOR ART

	This work	Andreou 2012 [10]	Zhan 2012 [11]	Park 2014 [12]	Ng 2011 [3]	Gupta 2007 [2]
Technology	**0.13-µm CMOS**	0.35-µm CMOS	0.35-µm CMOS	0.18-µm CMOS	0.50-µm CMOS	0.60-µm CMOS
Supply range (V)	**0.75-1.5**	1.7-3.5	1.2	1.8-2.6	0.93-5.0	N/A
Dropout voltage (mV)	**148**	1100	200	200	702	N/A
Supply current (µA)	**39.14@1.0 V-1 mA** **43.20@1.5 V-1 mA**	38.35@2.5 V	28@0 µA	55@1.8 V standby 80@1.8 V operate	28@1.0 V	N/A
Load current range	**0–100 mA**	0 mA	0–100 mA	0–50 mA	0–9.6 mA	0–5 mA
Temp. compensation type, value (ppm/°C)	**High-order** **26@0.75 V-0 µA** **32@1.50 V-0 µA**	High-order 3.9 [−15°C, 150°C] 13.7 [−50°C, 150°C]	N/A	N/A	First-order 34 [−20°C, 120°C]	First-order 34.7 [N/A]
Line regulation (%/V)	**–0.54@0 µA** **–0.57@100 mA**	0.039	0.39@100 mA	N/A	3.68	N/A
Power-supply rejection (dB)	**–51@1 kHz** **–24@10 MHz**	N/A	–49.8@1 kHz –13@1 MHz	–70@1 MHz –37@10 MHz	–58@100 Hz –12@1 MHz	–30.8@500 kHz –8.1@4 MHz
Tran. load settling time (µs) step size - rise/fall time overshoot/undershoot (mV)	**6.05/1.55** **100 mA – 0.1 µs** **92/270@20 pF**	N/A	~5 100 mA – 1 µs 50/105@100 pF	<10 50 mA – 0.1 µs 120/80@100 pF	<10 0.35 mA >100 mV@100 pF	N/A 5 mA – 0.1 µs U.S. > 500 mV
Active area (mm^2)	**0.31***	0.102	0.0987	0.14**	0.0464	N/A

* Including the additional circuitry for trimming, measurement and test purposes. ** Excluding on-chip capacitor.

between this work and a number of recently reported bandgap references and voltage regulators [2-3, 10-12] is presented in Table I. The transient load regulation is comparable with the LDOs reported in [2-3, 11-12] when considering the value of the load capacitor, the step size and the rise/fall time of I_{Load}, and finally the overshoot/undershoot and the settling time of the output. The temperature coefficient is higher than the specifications reported in [10]. However, the proposed voltage source is designed to source up to 100 mA for supply voltages down to 0.75 V. The voltage reference in [10] has a minimum supply voltage of 1.7 V with a dropout voltage as large as 1.1 V. It cannot provide any load current either. Compared to [11], the proposed LDVS achieves a higher order temperature curve at a considerably lower supply voltage. The main advantages of the proposed low-voltage voltage source are high-order temperature response, high current drive capability and minimum dropout voltage. These advantages, however, result in an increase in the area compared to the architectures in Table I. One reason for this increase is the use of relatively large devices required to cope with the smaller voltage headroom at lower supply voltage. This, in turn, leads to the need for the multi-path compensation network that also calls for more area. By using the proposed line voltage compensation technique, the line sensitivity of the proposed LDVS is comparable with that of the stand-alone LDOs with the benefit of high-order temperature compensation.

V. CONCLUSIONS

The design and analysis of a high-order buffered low-dropout voltage source (LDVS) have been presented in this paper. Measurement data of a 100 mA-600 mV voltage source show that the circuit can achieve a temperature coefficient of up to 32 ppm/°C. Temperature compensation is achieved by properly combining the outputs of a PTAT current generator with a proposed current-driven CTAT voltage generator in a closed-loop configuration. A line voltage compensation technique reduces the line sensitivity by a factor of three.

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