CMOS Ultra Low-Power Wavelet Filter based Sense Amplifier for Cardiac Signal Analysis

Rohan Sehgal[1], Amandeep Singh[2], and Wouter A. Serdijn[1]
[1]Delft University of Technology, the Netherlands
[2]Punjab Engineering College, India
r.k.sehgal@student.tudelft.nl, w.a.serdijn@tudelft.nl

***Abstract*—An ultra low power CMOS implementation of an analog wavelet Gm-C filter is proposed, using MOS transistors in their strong-inversion region. The analog wavelet filter is combined with a CMOS current-mode decision stage comprising a rectifier, a peak detector and a comparator to form a cardiac sense amplifier and the entire system is verified for cardiac QRS complex detection. The operation of the sense amplifier is validated through simulations using UMC 130nm CMOS process. The power consumption of the resulting circuit was found to be 165nW, operating from a supply voltage of 1.2 V.**

***Index Terms*—Analog integrated circuits, biomedical circuits and systems, cardiac pacemakers, wavelet filters.**

I. Introduction

CARDIAC signal analysis forms one of the primary functions of an implantable pacemaker. Since usually cardiac signal and noise components share the same spectral bands, discrimination of signal from noise and interference is very important. In the past few years, many new approaches to cardiac signal analysis have been proposed, such as algorithms based on filterbanks, artificial neural networks, non-linear transformations and the wavelet transform (WT). Among them, wavelet-based signal processing methods, though relatively new, demonstrate the potential for accurate feature extraction from noisy cardiac patterns.

There are many cardiac sensing systems based on WT implemented in both analog and digital domains. The one reported in [1] by Haddad et al, uses the Dynamic Translinear (DTL) circuit technique in bipolar IC technology to implement [1]an analog wavelet filter that implements the desired WT. Although very well suited for low-voltage, micropower applications, the DTL circuit technique also suffers from some shortcomings that preclude its use in implantable systems, such as pacemakers. Firstly, as DTL circuits operate in the current domain, the input, intermediate and output signals are current-mode. Since the cardiac signal is a voltage, this necessitates a voltage-to-current converter at the input of the system. Secondly, DTL circuits suffer from a limited signal-to-noise ratio (SNR), as the internal voltages are compressed. So, in order to achieve sufficient SNR, relatively large currents have to be supplied. Thirdly, the time constants realized in DTL circuits are proportional to CV_T/I_O, C being the capacitance involved in the time constant, V_T the thermal voltage kT/q, approximately 26 mV at room temperature and I_O a control current. Hence, the relatively large currents needed for a sufficient SNR also entail a large total capacitance and thus a large chip area.

In this paper, an ultra low power CMOS implementation of an analog wavelet Gm-C filter is proposed, using MOS transistors in their strong-inversion triode region. In this region, the voltage swing can be larger than for DTL, whereas for the same dynamic range, the capacitances can be smaller, thereby saving chip area. The resulting analog wavelet filter is then integrated with a CMOS decision stage, comprising of a rectifier, a peak detector and a comparator, and the entire system is verified for QRS complex detection.

II. QRS Detection

The QRS complex waveform represents the depolarization of cardiac ventricles and its detection forms an important part of ECG characterization. Due to its slightly distinguishable features, it can be detected from the rest of the cardiac pattern through non-linear filtering.

WT is known to be very useful for local analysis of non-stationary and fast transient signals because of its good time-frequency decomposition. WT basically decomposes the signal into components for analysis at different resolutions (scales). The wavelet transform of a function $f(t)$ at scale a and position τ is given by:

$$C(\tau,a)=\frac{1}{\sqrt{a}}\int f(t)\psi^{*}\left(\frac{t-\tau}{a}\right)dt \qquad (1)$$

where $\psi(t)$ is known as the wavelet base.

The algorithm adopted for QRS complex detection is based on detection of the modulus maxima of the WT. The corresponding cardiac sense amplifier consists of a filtering stage, comprising a wavelet filter bank with dyadic scales, followed by a decision stage. The time localization of the modulus maxima and the classification of characteristic points of the cardiac signals are processed by a microprocessor, and will not be discussed here.

This work was supported in part by the Dutch Technology Foundation STW under Grant 06148.

III. CIRCUIT DESIGN

A. Filtering Stage

An analog wavelet filter has been defined, its impulse response being an approximated first derivative of the Gaussian (gauss1). The gauss1 wavelet was chosen because of its resemblance to the QRS complex and its best time-frequency resolution, a property shared by all members of the Gaussian family. A low-order transfer function was derived with the help of the Padé approximation. A 3/5 Padé approximation was used as it offers the minimum mean square error for a reasonable filter order.

The transfer function thus obtained equals:

$$F(s) = \frac{-0.798483 + 75.6128s - 13.0993s^2 + 3.3949s^3}{43.5957 + 80.69s + 65.7123s^2 + 29.9898s^3 + 7.88586s^4 + s^5}$$

To decrease the complexity of the filter, an orthonormal ladder realization was chosen because it is semi-optimized for dynamic range and offers high sparsity and offers a reasonably low sensitivity to coefficient mismatch.

Gm-C integrators were used to map this orthonormal state space description onto a filter circuit topology. As the state-space description requires positive as well as negative coefficients, a differential Gm cell was used. Another advantage of using a differential cell is the cancellation of even-order distortion terms, thus improving linearity. As the frequency of operation is very low, it necessitates the use of either large capacitances or very small Gm's. In order to restrict the maximum integrating capacitance value to 20pF, the lowest value of Gm required is in the order of several tens of pA/V.

1) pA/V CMOS Triode-Transconductor

The Gm Cell is based on the design discussed in [2]. The input stage depicted in Fig. 1(a), comprises of a pseudo-differential input stage using PMOS transistors, M1,2,3,4, in strong-inversion triode region as the core Gm cell. Two current conveyors, M5,7 and M6,8, are used to relay the output currents of the pseudo-differential input stage onto the output stage and impose a well-defined drain-source voltage V_C on the input-stage PMOS transistors. Apart from M1,2,3,4, all other transistors operate in weak inversion saturation. Common-gate transistors M5,6 are biased using a cascode NMOS current source, comprising M1A,2A and M1B,2B. The gate voltages for M1A,2A and M1B,2B (V_{G1} and V_{G2}) are generated using a current bias generator consisting of an NMOS cascode current mirror input stage and an external current source. The output currents of the two current conveyors are inputted into two cascode current mirrors and equal the input voltages times the transconductance factor of the above PMOSTs.

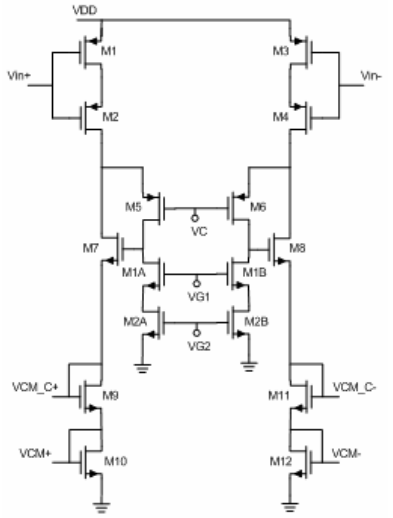


Fig. 1. (a) pA/V Triode Transconductor Input Stage

This factor equals $G_{m1} = \beta_1 V_{tune} = (W/L)_1 \mu_p C_{ox} V_{tune}$, where V_{tune} equals the applied drain-source voltage and the other variables have their usual meaning. Control voltage V_C is generated by an identical Gm cell input stage and a servo amplifier in a negative-feedback topology. Due to the negative feedback action, V_C will be adjusted such that V_{tune} becomes equal to the externally applied tuning voltage.

The NMOS cascode current mirror output stage forms the core of the transconductor output stage that is depicted in Fig. 1(b). Voltage source V_{offset} is used to further reduce the Gm. It also provides another parameter (besides V_{tune}) to tune the Gm of the transconductor. The upper part of the figure depicts the common-mode output voltage negative-feedback control loop.

A pair of anti-parallel diode connected thick-oxide transistors are used to generate the common-mode output voltage. This common-mode output voltage is offered to a

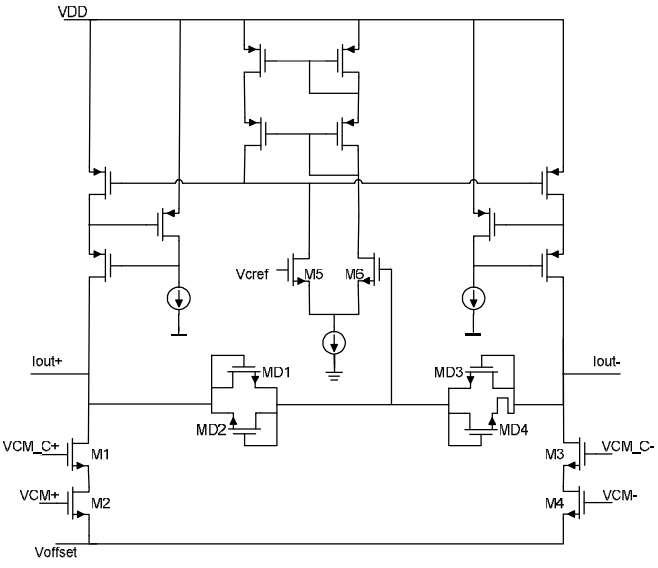


Fig. 1. (b) pA/V Triode Transconductor Output Stage

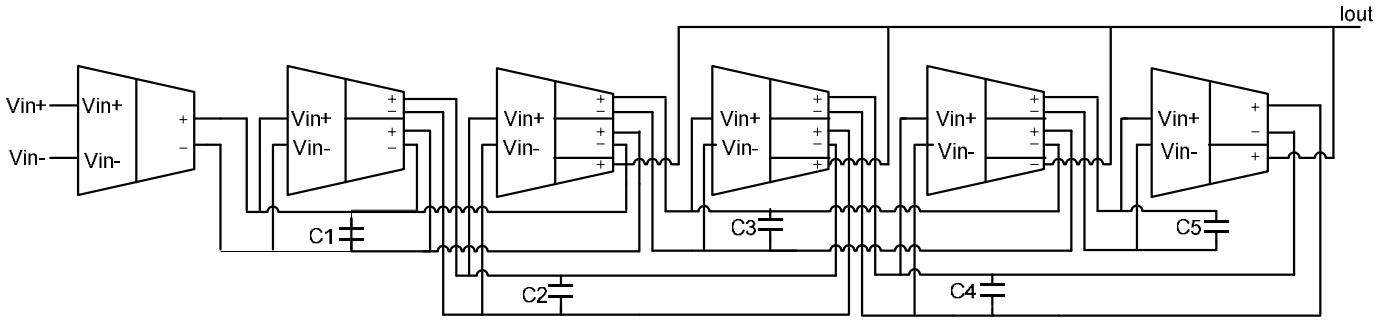


Fig. 2 Analog Wavelet Filter using Gm-C Topology

differential pair, M5 and M6, compared with the reference voltage V_{cref} and sets the voltage at the gates of the regulated cascodes at the proper level, such that the common-mode output voltage becomes equal to V_{cref}. The regulated cascode stages ensure a large differential (transconductor) output.

2) Filter Design

A fifth-order differential analog wavelet filter was designed. The state-space coefficients were implemented by choosing appropriate widths for the NMOS cascode current mirror transistors in the output stage of the Gm cell. In order to save power and chip area, the sparsity of the orthonormal filter topology is exploited using only one input Gm stage and multiple output stages, as shown in Fig. 2.

B. Decision Stage

The purpose of the decision stage is to detect the local modulus maxima of the WT of the cardiac signal. Hence, the signal from the wavelet filter is fed into a full-wave rectifier circuit, succeeded by a peak detector [1]. The final signal processing block is a comparator in order to detect the modulus maxima position of the QRS complex.

1) Full-wave Rectifier

The current-mode rectifier circuit is shown in Fig. 3. It is based on the circuit discussed in [3]. As all the transistors are operating in weak inversion, cascode mirrors are used to reduce the mismatch between the currents. Instead of using a

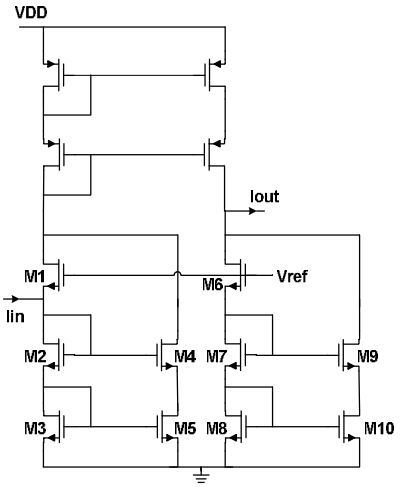


Fig. 3 Full wave Rectifier

diode-connected MOST like in [3], M1 is biased at a suitable V_{ref} in order to reduce the leakage current, and hence reduce the output offset current and power consumption. Since the output offset current and power consumption. Since the input-current levels can become as low as a few picoamps, the non-zero output offset current needs to be eliminated. This is performed by the combination of transistors M6,7,8,9,10, which is similar to the input stage for zero input. Voltage source Vref is designed using a peaking current source and a PMOS cascode current mirror [4].

2) Peak Detector

The current-mode peak detector shown in Fig. 4 is based on the concept proposed in [5]. In [5], current sources have been used to fix the biasing at the input and the output nodes. But the use of current sources introduces errors due to mismatch. Also in [5], a diode-connected transistor has been used as a switch, resulting in a significant amount of leakage.

In the circuit proposed here, a PMOST M1 in common-gate configuration is used as a unilateral switch as shown in Fig. 4. This is done to fix the voltage at the input node. Since the peak detector is used for very low frequencies, an additional capacitor is used, as the gate-to-source capacitances of M2 & M3 are not enough to hold such low voltages for a large amount of time.

A separate discharge path consisting of transistors M4 and M5 and current source Iref, is provided. By doing so, the discharge time constant is controlled by parameter I_{ref}. A small diode D1 is connected to ensure no discharge occurs via M1. In order to obtain a very large discharge time constant, the gate voltages of the transistors M4 and M5 are cross-coupled to obtain a discharge current of the order of few femtoamps.

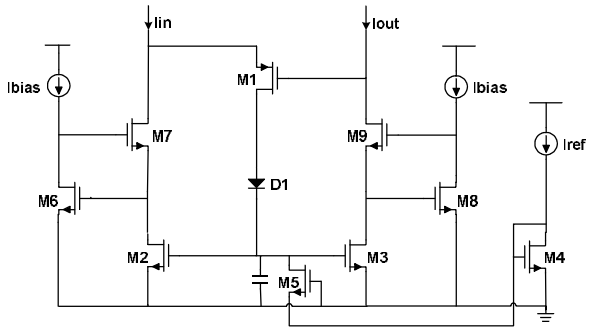


Fig. 4 Peak detector

A regulated cascode is used to increase the resistance at the peak detector input node, in order to make the peak detector more sensitive to input signal current. The biasing current I_{bias} for the regulated cascode structures are obtained by copying the PMOS cascode current mirror outputs of the rectifier.

By subtracting the peak detector output current from 4/3 times the rectifier output current, a bipolar current is obtained that is positive only when a peak occurs [6]. This current is offered to the final block in the system, the current comparator.

3) Comparator

For the comparator, a current switching CMOS comparator [7] shown in Fig. 5, is used. Its operation is as follows: for positive input currents, the voltage at the input node increases. This results in the CMOS inverter driving Mp into ON state. Similarly, for negative input currents, Mn is driven into ON state. The feedback loop around the inverter and Mp & Mn also helps in limiting voltage excursions at the input node. Another inverter is used as a binary buffer, to restore the output voltage levels and to drive the load (modeled as capacitance C_L). To reduce leakage, thick-oxide transistors, possessing a high threshold voltage, are used.

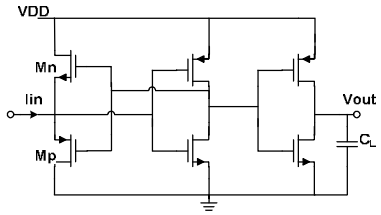


Fig. 5 Comparator Circuit [7]

IV. Simulation Results

The operation of the sense amplifier was verified using circuit simulations in UMC 130nm CMOS technology. The system has been designed to operate from a 1.2V supply voltage.

From circuit simulations, it was observed that the AC response of the wavelet filter exactly follows the AC response of the filter plotted from the intended transfer function $F(s)$. Fig. 6 shows the impulse response of the wavelet filter, which indeed approximates the Gaussian monocycle very well. Wavelet filter tuning voltage V_C was set at 10mV (referred to *VDD*). I_{bias} and V_{offset} are chosen to be 5nA and 45mV, respectively. For implementing other (dyadic) wavelet scales, the desired passbands and time constants can be selected by modifying V_{offset} or V_{tune}, or scaling the widths of the output current mirror transistors accordingly.

Fig. 7 shows the DC responses of the full-wave rectifier and comparator, with V_{ref} set at 0.15V. The transient response of the peak detector, with I_{ref} equal to 5nA, for a periodic pulse train as input is shown in Fig. 8. Finally, Fig. 9 shows the transient response of the entire system, block-by-block to a stylistic cardiac signal, contaminated by 50Hz interference. It can be seen that the modulus maxima of the cardiac signal have been detected accurately. The power consumption of the entire system amounts to 165nW per scale.

V. Conclusion

An ultra low-power CMOS implementation of an analog wavelet Gm-C filter has been proposed, using MOS transistors in strong inversion region. The analog wavelet filter is combined with a CMOS decision stage comprising a rectifier, a peak detector, and a comparator to form a cardiac sense amplifier and the entire system is verified for QRS complex detection. The whole system is highly programmable and operates from a 1.2V supply voltage, consuming 165nW per scale. The obtained results for a typical cardiac signal demonstrate a good accuracy in generating the desired wavelet transform and achieving accurate QRS complex detection.

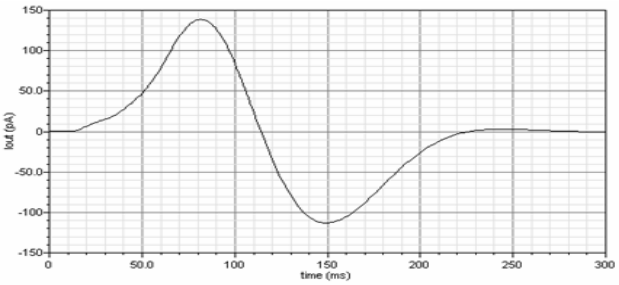


Fig. 6 Wavelet Filter (gauss1) Impulse Response

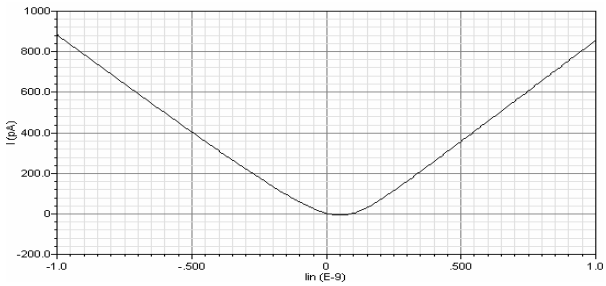
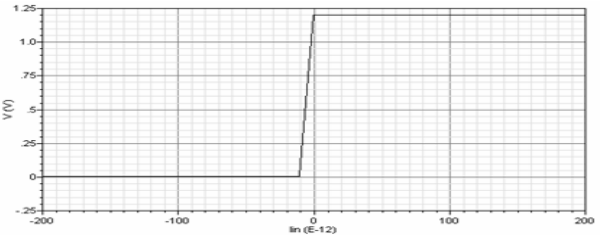


Fig. 7 DC response of (a) full-wave rectifier, and



(b) comparator

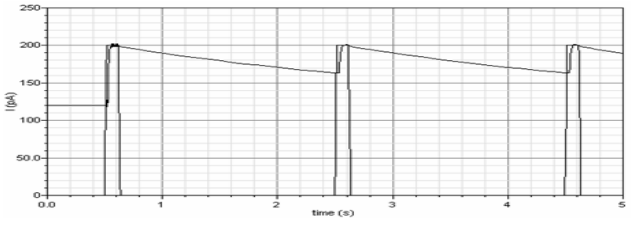


Fig. 8 Transient response of the peak detector

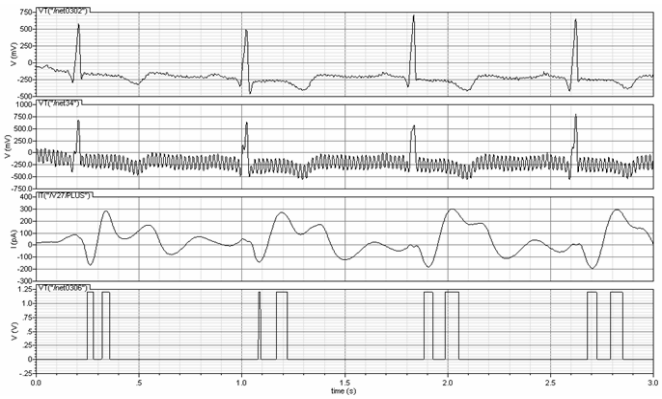


Fig. 9 Transient responses of the wavelet filter (3rd) and the comparator (4th) for a stylistic cardiac signal (1st) contaminated with 50Hz interference (2nd)

REFERENCES

[1] S.A.P. Haddad, R.P.M. Houben and W.A. Serdijn**,** "Analog wavelet transform employing dynamic translinear circuits for cardiac signal characterization," Proc. IEEE International Symposium on Circuits and Systems, Bangkok, Thailand, pp. 121-124, May, 2003.

[2] J.A. de Lima and W.A. Serdijn, "A compact nA/V CMOS triode transconductor and its application to very-low frequency filters," Proc. IEEE International Symposium on Circuits and Systems, Kobe, Japan, pp. 1988-1991, May, 2005.

[3] J. Poikonen and A. Paasio, "An area efficient full-wave rectifier for analog array processing," Proc. IEEE International Symposium on circuits andSystems, Bangkok, Thailand, pp. 757-760, May, 2003.

[4] Y. Xiaobin and C. Zhiliang, "Low voltage self-biasing reference circuits," Proc. International Conference on ASIC, pp. 314-317, Oct 2001.

[5] T. Fiez and M. Ismail, Analog VLSI: Signal and Information Processing, McGraw Hill, New York, 1992, pp. 291-295.

[6] Sandro A.P. Haddad, Ultra Low-Power Biomedical Signal Processing, Ph.D. thesis, Delft University of Technology, 2006.

[7] A. Rodriguez-Vazquez, R. Dominguez-Castro, F. Medeiro and M. Delgado-Restituto, "High resolution CMOS current comparators: Design and applications to current-mode function generation," Analog Integrated Circuits and Signal processing, Vol. 7, 1995, pp. 149-165.