Reconfigurable Subsampling Receiver Architecture For Wireless Body Area Networks

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***Abstract*—The wide range of wireless body area network (WBAN) applications gives rise to different system requirements for the carrier frequencies and data rates. In order to accommodate various standards in WBAN applications, a universal receiver system with good performance and low power is highly desirable. The subsampling receiver architecture is one of the promising receiver architectures that might fulfill the features of low power consumption and reconfigurability. However, there are two main concerns, namely the frequency stability and noise performance. In order to overcome these problems, a novel subsampling receiver architecture with two sampling branches as well as a new compensation algorithm are proposed and analyzed in this paper. The frequency stability and noise performance of the receivers can be greatly improved using this architecture. Simulation in different scenarios is carried out, and the results verify the effectiveness of the proposed architecture.**

I. Introduction

The wide range of Wireless Body Area Network (WBAN) applications gives rise to different system requirements for the frequency band and data rate. For example, the already existing IEEE 802.15.4 standard [1] which can be used in WBAN applications uses the frequency band of 2450 MHz for 250 kbps data rate communication. Recently, the emerging IEEE 802.15.6 standard [2] is under development to especially optimize the performance for low power wireless systems in WBAN applications. This newly proposed standard also uses several frequency bands and has different requirements for the data rate and modulation scheme. For instance, the frequency band from 402-405 MHz is used for the Phase Shift Key (PSK) like modulations with a data rate of 187.5 kbps, and the frequency band from 2400-2483.5 MHz is preserved for the PSK like modulations with a data rate of 600 Kbps. Due to the needs for the various wireless communication systems, a universal receiver system that can accommodate different data rates in multiple frequency bands is highly desirable.

Currently, work has been done to reduce the power consumption of the receivers for a single frequency band [3][4]. Still, besides the low power property, a universal wireless receiver that could support different WBAN standards in different frequency bands is highly desirable. This could further lead to lower cost since a reconfigurable system enabling wider applications would imply a higher volume of production, which means lower cost in the semiconductor industry.

The subsampling based Software Defined Radio (SDR) architecture [5] [6] is one of the promising receiver architectures which might fulfill the features of low power and reconfigurability, as shown in Fig. 1. In the traditional subsampling based SDR, the signal will be first down-converted into a lower frequency band by the subsampling operation, and then digitized by an analog-to-digital converter (ADC) working at a lower frequency. If the sampling frequency is high enough, signals in a wide frequency band could be captured. In this way, the reconfigurability of this receiver architecture can be guaranteed since the digital signal processing algorithm can be easily programmed.

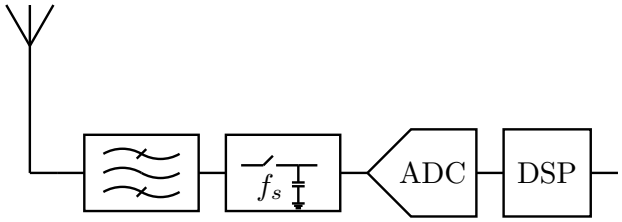

Fig. 1. Traditional Software Defined Radio Architecture.

However, there are two main problems about this simple subsampling based SDR architecture. One is the frequency stability of the downconverted signal, and the other one is the noise performance of the system. This prevents a wide application of this architecture in wireless systems.

In this paper, a novel reconfigurable subsampling receiver architecture is proposed to overcome the problems in the traditional subsampling architecture. In the proposed architecture, by using a reference signal, the frequency stability is guaranteed and not influenced by the sampling clock. Further more, the noise performance will be improved if a pure and clean reference signal is applied. This paper is organized as the following: in Section II, the drawbacks of the traditional subsampling architecture are elaborated in detail. Then in Section III, the reconfigurable subsampling receiver architecture is proposed and analyzed. Then in Section IV, the simulation results under different scenarios demonstrate the features of the proposed architecture. Finally the conclusion is given in Section V.

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II. Drawbacks of the Traditional Subsampling Receiver Architecture

To further illustrate the problems of the traditional subsampling architecture, a single channel signal at RF frequency will be presented in its complex form $\hat{x}(t)$ as

$$\hat{x}(t) = \hat{X}(t)e^{-j2\pi f_c t}, \tag{1}$$

where $\hat{X}(t)$ is the baseband complex signal with a bandwidth of B, and f_c is the carrier frequency. This baseband complex signal can be expressed also in the complex form as

$$\hat{X}(t) = X(t)e^{-j\Phi(t)}, \tag{2}$$

where $X(t)$ is the baseband amplitude information and $\phi_b(t)$ is the baseband phase information. Here, all the complex signals can be constructed by a real signal and its quadrature counter part.

If a sampling clock at frequency f_s with a certain root mean square (RMS) jitter δt_j is used for the subsampling operation, the jittered samples of the input complex signal can be written as:

$$\begin{aligned}\hat{x}_k &= \hat{x}(kT_s + \delta t_{kj}) \\ &= \hat{X}(kT_s + \delta t_{kj})e^{-j2\pi f_c(kT_s+\delta t_{kj})} \\ &= X(kT_s + \delta t_{kj})e^{-j[\Phi(kT_s+\delta t_{kj})+2\pi f_c kT_s]}e^{-j2\pi f_c \delta t_{kj}},\end{aligned} \tag{3}$$

where T_s is the time interval of the sampling instances which is $T_s = 1/f_s$, and δt_{kj} is the clock jitter at the kth instance.

According to the bandpass sampling theorem [7], if the subsampling frequency is larger than twice the bandwidth of the baseband signal $\hat{X}(t)$, which requires $f_s > 2B$,then the baseband signal can be fully reconstructed from the sampled data $\hat{X}(kT_s)$. This gives the theoretical minimum limit for the subsampling frequency f_s.

However, in (3), the sampled baseband information $\hat{X}(kT_s + \delta t_{kj})$ has both amplitude and phase error since the sampling jitter is present. These errors will cause the performance degradation. Furthermore, the first exponential term $e^{-j[\Phi(kT_s+\delta t_{kj})+2\pi f_c kT_s]}$ shows the center frequency of the down-converted signal, the exponential term $e^{-j2\pi f_c \delta t_{kj}}$ stands for another phase error from the sampling clock jitter. They will cause more severe performance downgrading.

A. Frequency Stability

The down-converted signal will be centered at another frequency f_b, which can be calculated using

$$f_b = f_c - ||\frac{f_c}{f_s}||f_s. \tag{4}$$

Here, $||f_c/f_s||$ stands for the nearest integer of f_c/f_s. This equation reveals the problem of the frequency stability. The final output central frequency can change significantly even when the sampling frequency changes slightly. For example, if the wanted IEEE 802.15.6 signal is located exactly at 2.4 GHz, and the ideal sampling frequency is 30 MHz. Then, in the deal case, the down converted signal will be located around DC. However, the frequency drift in the sampling clock is often expected in low power wireless systems. If the sampling frequency is 100 kHz off from the ideal 30 MHz, then the sampled output will be centered at 8 MHz. As a result, the frequency stability requirement for the subsampling clock will be very strict.

B. Noise Performance

The second problem for the traditional subsampling architecture is the noise performance. The noise contributions from noise folding and jitter in sampling systems have been widely discussed [8][9].

As shown in (3), the variance of the jitter δt_{kj} is the RMS jitter, then the additional variance of $\hat{x}_k$ caused by the exponential term $e^{-j2\pi f_c \delta t_{kj}}$ is

$$\text{Var}(\hat{x}_k) = [\hat{X}(kT_s)]^2 \cdot (2\pi f_c)^2 \cdot \text{Var}(\delta t_{kj}). \tag{5}$$

Clearly, in (5), the jitter term is multiplied by the RF carrier frequency. Since f_s is at least two times larger than the baseband bandwidth B, then the amplitude and phase errors in the sampled baseband signal is quite small. As a result, the additional phase error of $e^{-j2\pi f_c \delta t_{kj}}$ is much more dominant. Thus in the later discussions, the amplitude and phase errors in the sampled baseband signal is not addressed.

This equation also suggests that the noise power of the sampled signal is related to the carrier frequency and the RMS jitter, and a higher carrier frequency will result in a higher noise power in the sampled signal if the RMS jitter remains the same. For example, the noise power in the downconverted 2.4 GHz signal is about 6.25 times larger than that of the 950 MHz signal, when the sampling clocks have the same RMS jitter in the subsampling architecture.

From the discussion above, it is clear that, for the subsampling architecture, the sampling clock is very important. It is desirable to use clean and stable sampling clocks. However, such clocks are not alway available. Therefore, methods are needed to release the tight requirements for the sampling clocks in the subsampling architecture.

III. Proposed Reconfigurable Architecture with Jitter Compensation

In order to overcome the problems in the normal subsampling based SDR, a novel subsampling based SDR architecture is proposed as in Fig. 2. In this architecture, in one branch, the RF input signal is first filtered by a reconfigurable filter in order to choose the correct frequency band and filter out other unwanted RF signals. The filtered RF signal is sampled at a frequency f_s. In the second branch, a reference sinusoidal signal with an known frequency is also sampled by the same sampling clock as in the first branch. Then, in both branches, sampled signals are digitized by analog-to-digital converters (ADC) and then enters in the digital signal processing (DSP) unit. In the DSP, a compensation algorithm shown in Fig. 3 is used to achieve the frequency selectivities and cancel the jitter. The compensated signal can be used for the later processing, like filtering and demodulation.

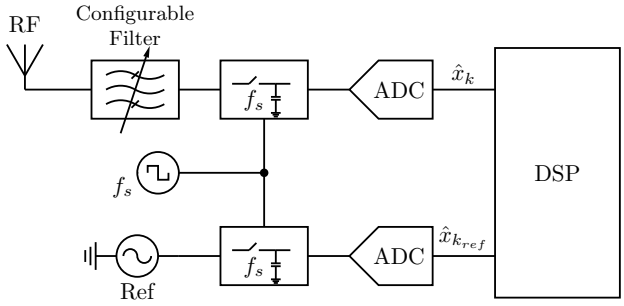

Fig. 2. Proposed subsampling SDR architecture with two identical sampling branches.

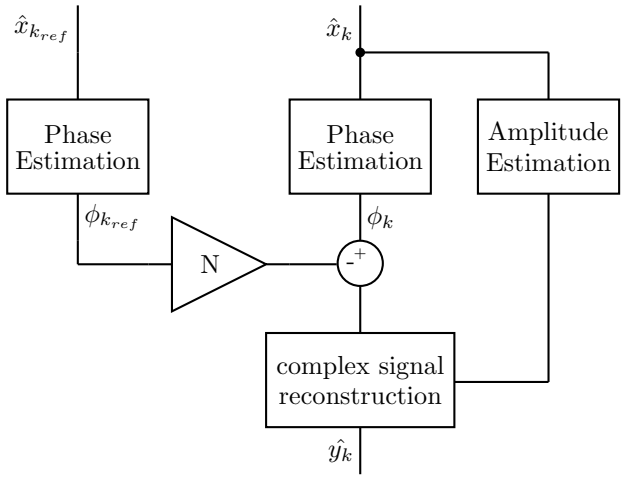

Fig. 3. Proposed algorithm in the DSP to achieve the frequency selectivities and jitter cancellation.

To analyze the performance of the proposed architecture, the sampled reference complex signal $\hat{x}_{k_{ref}}$ can be expressed as

$$\hat{x}_{k_{ref}} = \hat{x}_{ref}(kT_s + \delta t_{jk}) = e^{-j2\pi f_{ref} kT_s} e^{-j2\pi f_{ref}\delta t_{jk}}. \quad (6)$$

Comparing (6) and (3), since both the reference signal and the RF signal are sampled by the same sampling clock, there are similar jitter introduced noise contributions in both signals.

In the algorithm shown in Fig. 3, to simplify the analysis, the perfect estimation is assumed. Then the phase information of the reference signal $\phi_{k_{ref}}$ and the phase information of the RF signal ϕ_k are extracted from the sampled value. The amplitude information of the RF signal is extracted. Then the new phase information can be generated by subtracting N times $\phi_{k_{ref}}$ from ϕ_k. Here N is a changeable value which can be set on demand. Using this phase information and the amplitude information of the RF signal, a new signal $\hat{y}_k$ can be constructed,

$$\hat{y}_k = X(kT_s + \delta t_{jk}) e^{-j(\phi_k - N\cdot\phi_{k_{ref}})}, \quad (7)$$

where $\phi_k = \Phi(kT_s + \delta t_{jk}) + 2\pi f_c(kT_s + \delta t_{jk})$ and $\phi_{k_{ref}} = 2\pi f_{ref}(kT_s + \delta t_{jk})$.

Expanding (7), the final output $\hat{y}_k$ is

$$\begin{aligned}\hat{y}_k =& X(kT_s + \delta t_{jk}) e^{-j\Phi(kT_s+\delta t_{jk})} \\ & \cdot e^{2\pi kT_s(f_c - Nf_{ref})} e^{-j2\pi\delta t_{jk}(f_c - Nf_{ref})} \\ =& \hat{X}(kT_s + \delta t_{jk}) e^{2\pi kT_s(f_c - Nf_{ref})} e^{-j2\pi\delta t_{jk}(f_c - Nf_{ref})}.\end{aligned} \quad (8)$$

In this case, if N=0, then it is just working as the traditional subsampling architecture. If N is set to some other value, then the reconstructed output signal $\hat{y}_k$ will have different output center frequency and noise performance.

In reality, there are always some errors in the estimation algorithms, then the errors from the estimation can be expressed as another additional complex noise signal term to (8). However, if the accuracy of the ADCs and the estimation algorithms can be improved, then this error can be minimized. Therefore, the errors from the estimation algorithms are not addressed in the following discussions.

A. Frequency Stability

In (8), the first exponential term determines the central frequency of the output f_b. In this case,

$$f_b = f_c - Nf_{ref} - ||\frac{f_c - Nf_{ref}}{f_s}||f_s. \quad (9)$$

If f_s is large enough, and the value of N and f_{ref} are chosen to satisfy

$$f_c - Nf_{ref} < f_s, \quad (10)$$

then the output central frequency f_b is only determined by

$$f_b = f_c - Nf_{ref}. \quad (11)$$

Here, the final frequency down-conversion is not even related to the sampling frequencies, and it is only determined by the value of N and the reference frequency f_{ref}. Thus, the frequency stability requirement for the sampling clock is relaxed, and the frequency of the sampling clock can be set to a certain convenient value. Then the requirement for the frequency stability should hold for the reference clock. Normally, signals from quartz crystal oscillators are pure and clean compared to sampling clocks, and have good frequency stability. Therefore they can be good candidates for the reference signals.

As a result, if the reference frequency f_{ref} is chosen, then the value of N determines the spectrum location of the downconverted signal. Since N can be reconfigured, the wanted RF signal which is downconverted to DC can be also reconfigured. By choosing different N value, this architecture is quite flexible and reconfigurable to adapt to different central carrier frequencies, which means it is easy to make this architecture multi-standard compatible.

B. Noise Performance

The second exponential term in (8) stands for the jitter introduced noise from the sampling clock. Then the variance

of $\hat{y}_k$ due to the RMS jitter of the sampling clock can be calculated as

$$\text{Var}(\hat{y}_k) = [\hat{X}(kT_s)]^2 \cdot [2\pi(f_c - Nf_{ref})]^2 \cdot \text{Var}(\delta t_{kj}). \quad (12)$$

Comparing (12) to (5), clearly the noise from the sampling clock jitter will be reduced by $(f_c - Nf_{ref})^2/f_c^2$ times. Thus, if the value of N and f_{ref} is well chosen, there should be significant reduction of the noise from the sampling clock jitter.

In conclusion, this proposed subsampling architecture can provide easy reconfigurability and good jitter cancellation performance. The robustness and reconfigurability of the subsampling based SDR can be improved. In the following section, simulation results will reveal more properties of this architecture.

IV. Simulation Results

In this section, spectrum simulations and bit error rate (BER) simulations are carried out to verify the performance of the proposed subsampling architecture. In the spectrum simulations, the reconfigurability of the proposed architecture for different frequency bands is demonstrated. Further BER simulations indicate good noise performance when sampling clock jitter is present.

A. Spectrum Analysis

Fig. 4 shows the difference in performance between the traditional architecture and the proposed architecture in frequency selectivities. In this case, according to the IEEE 802.15.6 standard draft, a π/8-D8PSK modulated RF input signal is centered at 2404 MHz with a data rate of 600 ksps. In the two experiments, this RF signal is sampled by a 40 MHz and a 42 MHz clock both with a 20 ps RMS jitter respectively. As shown in the upper figure, in the traditional architecture, the down converted signals are centered at different frequencies which can be calculated using (4). On the contrary, the down-converted signals are all centered at DC in the proposed architecture when the reference signal is chosen to be 1 MHz and N=2404, and the reference signal is assumed to to clean. This verifies that the frequency plan of the down-converted signal is not related to the sampling clock frequency. Furthermore, the noise floor in the upper plot is mainly caused by the jitter from the sampling clock. In the lower plot, the noise floor of the downconverted signals is obviously much lower. This demonstrates the jitter reduction effect of this architecture.

In order to demonstrate the reconfigurability of the proposed architecture, a simulation is done with a multi-band input signal. Using this architecture, signals from different frequency bands can still be captured provided that all frequency bands are received by the antenna. As shown in the first plot in Fig. 5, four channels of signals from three different bands specified in the IEEE 802.15.6 standard draft are received: one 187.5 KHz signal at 405 MHz, one 250 KHz signal at 950 MHz, one 600 KHz signal at 2402 MHz and a 250 KHz signal at 2404 MHz. The sampling frequency is still 40

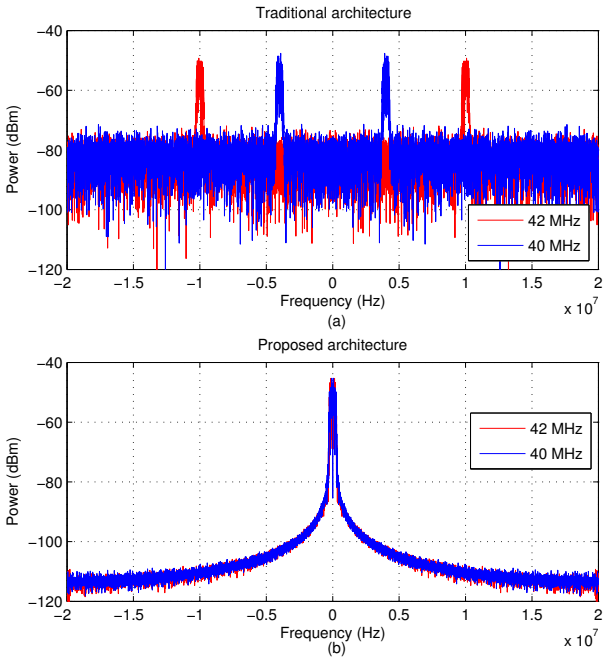

Fig. 4. Comparison between the proposed architecture with the traditional one with different sampling frequencies. (a) output signal spectrums with sampling frequencies of 40 MHz and 42 MHz when N=0. (b) output signal spectrums with sampling frequencies of 40 MHz and 42 MHz when N=2404.

MHz, and the reference signal frequency is 1 MHz. Before the sampling, proper filtering operations are applied to select the main frequency to avoid spectrum overlapping. As shown in the rest of the plots in Fig. 5, different N values indicate different signal frequencies to convert down to DC. In this way, the selectivity of different frequency bands and different channels can be achieved.

B. BER Simulation

Fig. 6 shows the BER performance for two different input carrier frequencies under different N values as a function of the sampling RMS jitter. In this case, the D8PSK modulated input signals with Eb/No of 15 are centered at 2400 MHz and 950 MHz respectively. The reference signal is a 1 MHz sinusoidal with a jitter of 1 ps. The sampling clock is 50 MHz with a changing RMS jitter. When N=0, it indicates that the proposed architecture is just working like the traditional subsampling architecture. When N=950, the signal of 950 MHz is downconverted. N=2400 means the down-conversion is done for the signal of 2400 MHz.

As predicted, the signals with a lower carrier frequency will have better BER performance than those at a higher carrier frequency. It can be observed from the figure that the noise power for the 950 MHz signal is about 6 times less than that of the 2400 MHz for the given BER of 0.1%.

Also from this figure, the reduction of the jitter introduced noise is obvious. When the sampling jitter goes high, the BER performance goes down for the traditional architecture,

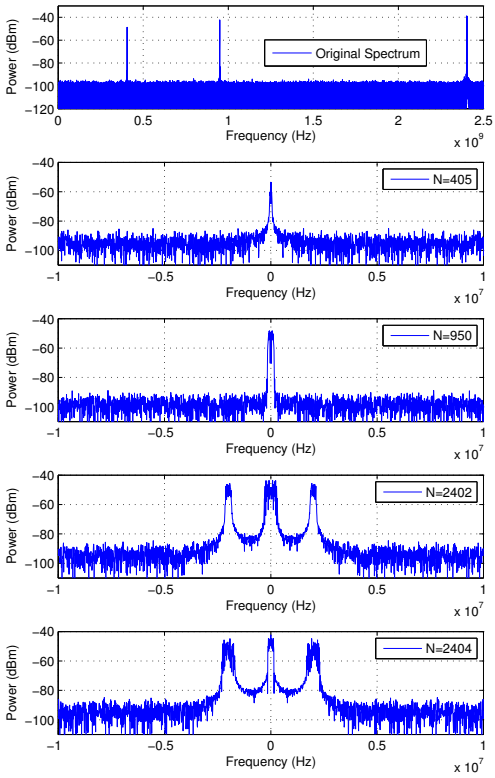

Fig. 5. Output spectrum of different vales of N. This demonstrates the ability of channel tuning.

namely the N=0 case. However, for the N value that correctly downconverts the input signal, the BER performance almost remains the same, since the BER performance is mainly determined by the jitter power from the reference signal. When the reference has less jitter than the sampling clock, a substantial BER performance improvement is expected.

In conclusion, all the simulations verify the viability of the proposed architecture. In this architecture, the reconfigurability is easily achieved by tuning the value of N. Meanwhile, the noise reduction of the jitter introduced noise can be observed.

V. Conclusion

The subsampling receiver architecture is one of the candidate receiver architectures to achieve both ultra low power consumption and reconfigurability for WBAN applications. However, there are two main drawbacks which greatly affect the performance, namely the frequency stability and noise performance. In order to overcome these problems, a novel subsampling receiver architecture as well as its accompanying processing algorithm are proposed and analyzed. By applying this architecture, the frequency stability and noise performance can be greatly improved. Moreover, this architecture features easy reconfigurability to accommodate different frequency

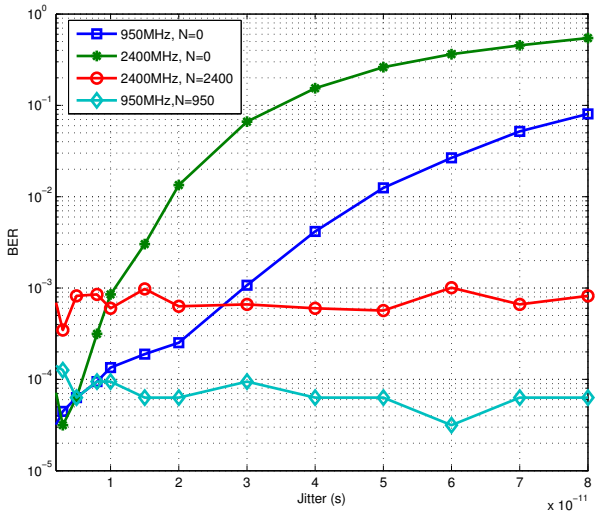

Fig. 6. BER performance under different sampling clock jitters at different carrier frequencies and different N values. The reference clock has 1ps RMS jitter.

bands.

In conclusion, the proposed subsampling receiver architecture can be a promising low power, reconfigurable and robust wireless architecture for WBAN applications. It enables the viability of a future universal receiver system with good reconfigurability and performance.

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