Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters

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***Abstract*—In this paper, a design method for the co-design and integration of a CMOS rectifier and small loop antenna is described. In order to improve the sensitivity, the antenna-rectifier interface is analyzed as it plays a crucial role in the co-design optimization. Subsequently, a 5-stage cross-connected differential rectifier with a 7-bit binary-weighted capacitor bank is designed and fabricated in standard 90 nm CMOS technology. The rectifier is brought at resonance with a high-Q loop antenna by means of a control loop that compensates for any variation at the antenna-rectifier interface and passively boosts the antenna voltage to enhance the sensitivity. A complementary MOS diode is proposed to improve the harvester's ability to store and hold energy over a long period of time during which there is insufficient power for rectification. The chip is ESD protected and integrated on a compact loop antenna. Measurements in an anechoic chamber at 868 MHz demonstrate a –27 dBm sensitivity for 1 V output across a capacitive load and 27 meter range for a 1.78 W RF source in an office corridor. The end-to-end power conversion efficiency equals 40% at –17 dBm.**

***Index Terms*—Antenna, CMOS rectifier, co-design, integration, RF energy harvester, sensitivity, WSN.**

I. Introduction

THE vision of realizing a network of autonomous wireless sensor nodes (WSNs) attracted much attention over the years as it offers a wide range of applications [1]. These WSN networks can sense, process and wirelessly transmit information such as temperature, humidity, location and sensor identification. Typical applications are inventory management, smart buildings, structural maintenance and health monitoring in personal body area networks (BANs) [2], [3]. The majority of WSNs require a low update rate (less than one hertz) and a limited wireless range of several meters [4]. The average power consumption of a WSN has been estimated by various authors to be in the order of 10 to 100 μW [3], [5], [6], but strongly depends on the type of sensor and application.

Manuscript received August 07, 2013; revised November 19, 2013; accepted January 14, 2014. Date of publication February 13, 2014; date of current version March 05, 2014. This paper was approved by Associate Editor Gyu-Hyeong Cho.

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Digital Object Identifier 10.1109/JSSC.2014.2302793

Providing this power by means of an energy harvester truly makes the WSN autonomous and significantly extends lifetime. RF energy sources can be used in many applications where energy sources such as light, vibrations and thermal gradients are not available. Fig. 1(a) illustrates a typical RF scavenged WSN network where each WSN (Fig. 1(b)) harvests energy from an RF source and converts the captured electromagnetic (EM) energy into electrical DC power. This DC power is locally stored in a capacitor or battery and re-used as power supply when required. Besides delivering energy, the RF source can also serve as a communication hub and provide a system clock by modulating the RF carrier wave [7].

Apart from designing for efficient power transfer, the harvester can be designed for superior sensitivity. The available power at an impedance and polarization-matched antenna in far field can be calculated using

$$P_{\mathrm{av}} = P_{\mathrm{EIRP}} G_A \left(\frac{\lambda}{4\pi d}\right)^2 \tag{1}$$

where $P_{\mathrm{EIRP}} = P_{TX} G_{TX}$ is the Equivalent Isotropic Radiated Power, P_{TX} is the output power of the transmitter, G_{TX} is the transmitting antenna directional gain, G_A is the receiving antenna directional gain, λ is the wavelength and d is the distance from the radiating source [8]. Note that although the available power decreases with the square of the distance, the area covered by the RF source *increases* by the same amount. This can be exploited in high density and heavily duty cycled WSN networks. By harvesting at μW power levels and storing the accumulated energy in a buffer, a mW power budget can be realized for each individual WSN combined with long wireless range [7]. In this work, a dedicated RF source is assumed which provides strong and reliable power at the 868 MHz European Industrial, Scientific and Medical (ISM) band. The maximum allowed radiated power in this band is 3.28 W EIRP [9].

Generating a sufficiently large voltage to activate the rectifier with a few μWs of power is the major design concern for long range RF harvesters as MOS transistors inherently are voltage-controlled devices. For example, the terminal voltage of a 50 Ω antenna with -20 dBm available power is only 63.24 mV, much too low to overcome the threshold voltage of a standard CMOS process which lies around 400 mV in 90 nm technology.

Some solutions have been proposed to reduce the rectifier turn-on voltage by using (near) zero V_{TH} transistors [10], [11], gate pre-biasing [12] or V_{TH} self-cancellation schemes [13]–[16]. However, the high fabrication costs, calibration phase or reverse current leakage make these solutions too expensive and impractical. Moreover, the majority of published

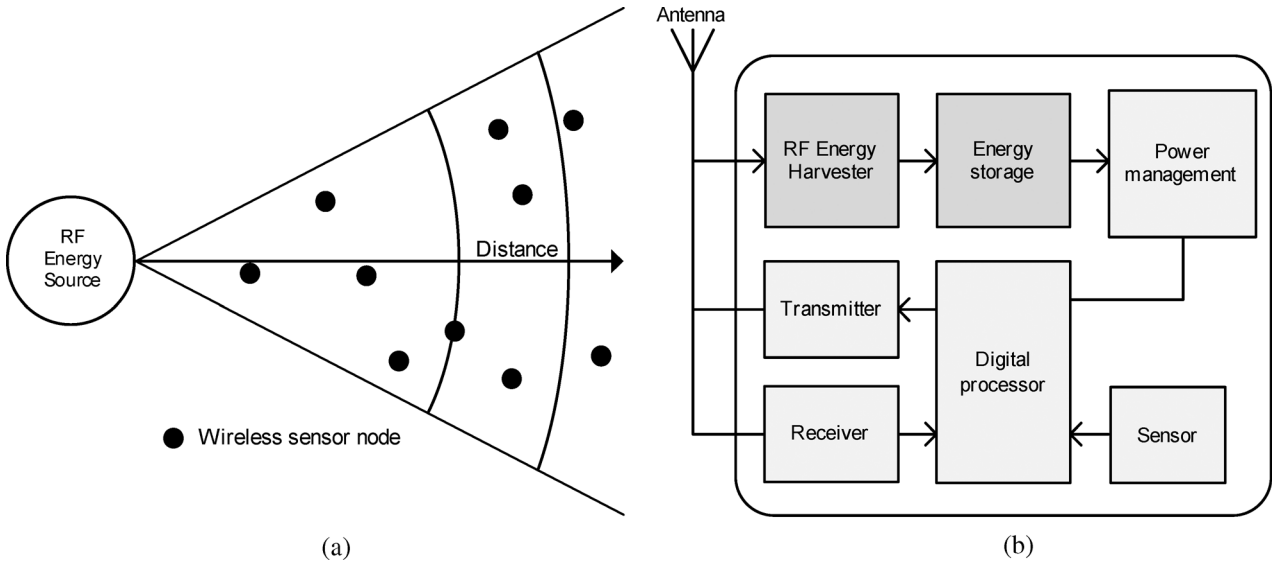


Fig. 1. RF scavenged wireless sensor node network. (a) RF scavenged sensor network using a dedicated or ambient RF energy source. (b) System level block diagram of a wireless sensor node.

CMOS rectifiers designed for long range RF energy harvesters are tested only in the electrical domain by using a signal generator as a well defined input power source with well defined impedance. Although this is a convenient way of measuring, it oversimplifies and neglects many aspects that can have a dominant effect on the end-to-end performance. Antenna characteristics such as impedance, efficiency and radiation pattern are a strong function of wavelength and hence the surrounding environment. By including an antenna in the measurements, the complete energy conversion from the EM domain to the electrical domain can be evaluated over distance and therefore include all performance-limiting effects such as misalignment, radiation efficiency, polarization and impedance mismatch. In addition, this allows to co-design the antenna and rectifier for maximum performance as the interface is no longer constrained by the traditional 50 Ω characteristic impedance.

In this work, we demonstrate a compact self-calibrating and highly sensitive RF energy harvester in standard CMOS technology. The design methodology is given in Section II followed by the circuit design in Section III. The co-design with the antenna is discussed in Section IV and the experimental results are given in Section V.

II. Design Methodology

In this section, a design methodology is presented to optimize the antenna-rectifier interface in order to generate a specific output voltage with minimum input power. The choice of interface impedance plays a crucial role in this optimization. Therefore the interface model is defined first.

A. Interface Modeling

The rectifier essentially is a nonlinear circuit, meaning that a full wave nonlinear analysis such as in [10] is required to accurately predict the behaviour of the rectifier over a wide range of input powers. Although this method offers an accurate model for the rectifier, it provides less insight in the antenna-rectifier optimization procedure and increases the complexity of the model

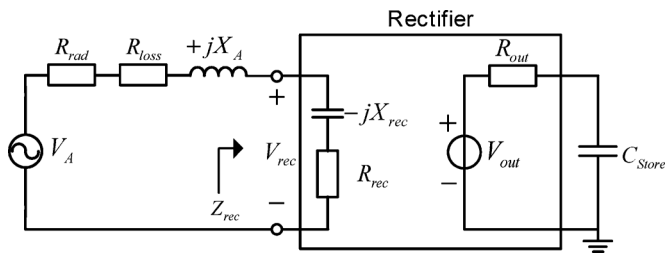


Fig. 2. Antenna-rectifier interface equivalent circuit model.

as intuitive concepts such as impedance and frequency domain by definition can no longer be used. Furthermore, a nonlinear analysis requires knowledge of the implementation of the rectifier, and therefore does not allow for a general analysis that can be used for any antenna-rectifier topology. Therefore, the simplified linear interface model in Fig. 2 is used in this work as it provides a very useful and intuitive understanding of the fundamental properties at the antenna-rectifier interface.

The interface model shows an equivalent circuit model of a rectifier with capacitive load connected to a loop antenna. The voltage induced by the electric field is represented by a Thévenin equivalent voltage source V_A and is a function of the radiation resistance $R_{\rm rad}$ and the available power $P_{\rm av}$ calculated from (1). The conduction loss resistance $R_{\rm loss}$ is related to the radiation efficiency. The reactive element jX_A represents the energy stored in the near field and is inductive since the loop antenna is used below its first anti-resonance frequency. The rectifier output is also modeled as a Thévenin equivalent circuit. The input impedance of the rectifier is mainly capacitive where $R_{\rm rec}$ is the real part of the impedance and $X_{\rm rec} = 1/(\omega C_{\rm rec})$ represents the imaginary part. Both $R_{\rm rec}$ and $X_{\rm rec}$ can be assumed constant at low input power levels (i.e., around the power-up threshold) as the rectifier impedance will be dominated by the linear parasitic components [15].

By using an antenna with an inductive reactance, the rectifier capacitance can be compensated for without using other

TABLE I
ANTENNA EQUIVALENT CIRCUIT ELEMENTS

Thévenin equivalent voltage	$V_A = \sqrt{8R_{rad}P_{av}}$
Radiation resistance	$R_{rad} = \eta_A R_A$
Conduction loss resistance	$R_{loss} = (1-\eta_A)R_A$
Antenna resistance	$R_A = R_{rad} + R_{loss}$
Antenna reactance	$X_A = \omega L_A$
Radiation efficiency	$\eta_A = \frac{R_{rad}}{R_{rad}+R_{loss}}$

external components. Moreover, this LC combination also provides passive voltage boosting, which effectively increases the rectifier input voltage $V_{\rm rec}$ for the same input power. The relations between the antenna equivalent circuit elements are described in Table I.

As the rectifier input voltage $V_{\rm rec}$ determines the sensitivity of the RF energy harvester, an expression is derived below that relates $V_{\rm rec}$ to the interface impedance and the available power. The input voltage swing at the rectifier can be written as

$$V_{\rm rec} = V_A G_{V,\rm boost} \tag{2}$$

where $G_{V,\rm boost}$ is the passive voltage boost obtained from the resonating network. When $X_{\rm rec} \gg R_{\rm rec}$ and the interface is at resonance ($X_{\rm rec} = X_A$), it holds that

$$G_{V,boost} = \left|\frac{V_{\rm rec}}{V_A}\right| \approx \frac{X_{\rm rec}}{R_A + R_{\rm rec}}. \tag{3}$$

When combining (2) and (3) and using $V_A = \sqrt{8\eta_A R_A P_{\rm av}}$ from Table I, the minimum required available power for a desired $V_{\rm rec}$ is written as

$$P_{\rm av} = \left(\frac{R_A + R_{\rm rec}}{X_{\rm rec}}\right)^2 \frac{V_{\rm rec}^2}{8\eta_A R_A}. \tag{4}$$

Equation (4) indicates that increasing $X_{\rm rec}$ is a very effective way of improving the sensitivity. The radiation efficiency η_A highly depends on the antenna size and becomes low when the area is scaled down too much. The rectifier input resistance $R_{\rm rec}$ and reactance $X_{\rm rec}$ depend on the rectifier implementation. In reality, the input power dependence of $R_{\rm rec}$ and $X_{\rm rec}$ reduces the passive voltage boost at high input powers. This effect is not included in this linear model but will be taken into account during circuit simulations in Section III-C.

If for example the design parameters are $\eta_A = 0.8$ and $X_{\rm rec} = 400\ \Omega$, the curves in Fig. 3 show the minimum required available power to generate $V_{\rm rec} = 0.4$ V for three different values of $R_{\rm rec}$ as function of the antenna resistance. Evidently, a smaller $R_{\rm rec}$ lowers the required available power as it increases the passive voltage boost at the interface. The minimum point of each curve is when conjugate matching occurs. When $R_A > R_{\rm rec}$, the antenna voltage V_A increases but the passive voltage boost becomes lower. Much more power is required when $R_A < R_{\rm rec}$ as the antenna voltage becomes smaller and no benefit is gained from the passive voltage boost due to the current limiting $R_{\rm rec}$. In this example, the minimum required available power to generate $V_{\rm rec} = 0.4$ V for a 50 Ω interface equals -16 dBm (25.1 μW), while only -23 dBm (5 μW) is required for a 10 Ω interface, resulting in a 7 dB sensitivity improvement. This indicates the importance of a low resistive and high-Q antenna-rectifier interface. This design methodology can be applied to any rectifier and loop antenna implementation and can also be extended to rectifiers with a resistive load [17].

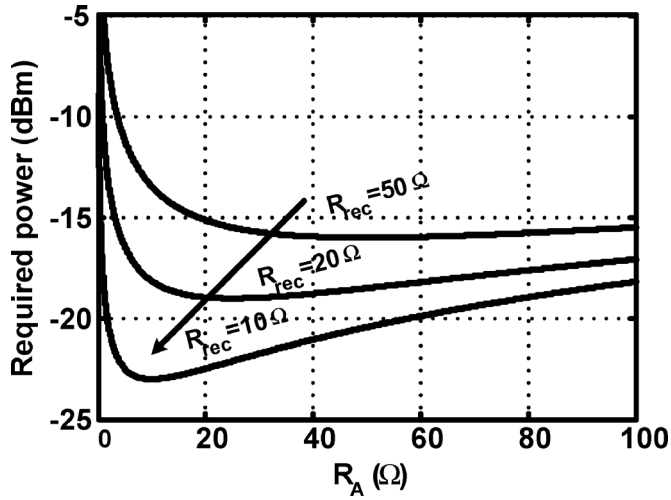


Fig. 3. Calculated minimum required power to generate $V_{\rm rec} = 0.4$ V versus antenna resistance for various $R_{\rm rec}$. $\eta_A = 0.8$ and $X_{\rm rec} = 400\ \Omega$.

B. Control Loop

All antenna parameters described so far are dependent on wavelength and therefore also the surrounding environment. Moreover, the rectifier nonlinear input impedance also varies with frequency and input power. This makes the high-Q interface very sensitive to any impedance variation. To compensate for this, a control loop is added to tune the impedance such that a resonance is created with the antenna. The proposed RF energy harvester in Fig. 4(a) shows a feedback controlled voltage boosting and tuning network that compensates variation at the interface that may occur in a realistic environment. As the antenna and rectifier reactance at the interface influences both the resonance frequency and the passive voltage boost of the interface, it is decided to compensate only for reactive variations. Also compensating the real part is less critical but will increase the complexity of the control loop implementation. This way, the loop still improves the RF energy harvester robustness while taking advantage of the passive voltage boost obtained from the high-Q resonator. Finally, a voltage monitor determines when enough energy is stored in the off-chip capacitor.

Fig. 4(b) illustrates the output voltage as function of time divided into five different regions for a constant input power. In Region I, there is no initial energy available to activate the control loop. The interface is therefore mismatched and the rectified voltage increases slowly with time. In Region II, Vout reaches the minimum voltage to activate the control loop. The output voltage slightly drops due to the power consumption of the control loop itself while optimizing the interface. Once the interface is optimized, the capacitor can be charged to $V_{\rm max}$ as indicated in Region III. In Region IV, the main circuit is connected

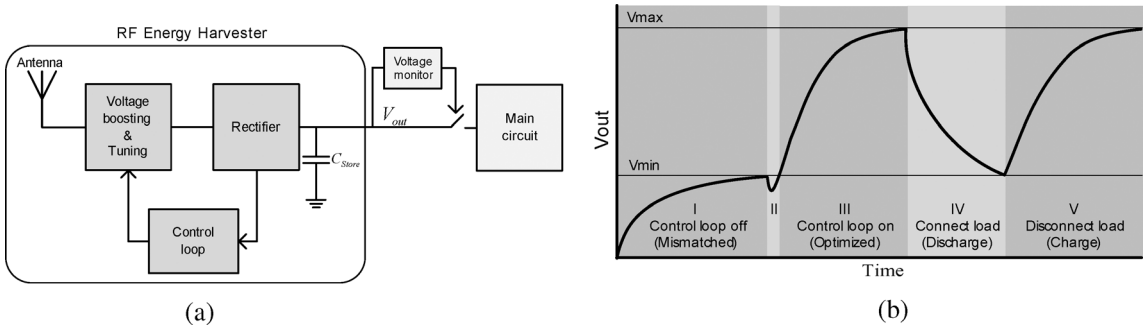


Fig. 4. (a) System overview of the proposed RF energy harvester with control loop. (b) Output voltage waveform with zero energy initial condition.

and discharges the capacitor until $V_{\min}$ to reactivate the control loop. The energy available to the main circuit in this region equals $E = C_{\text{store}}(V_{\max}^2 - V_{\min}^2)/2$. The load is disconnected again in Region V and the cycle repeats itself. This ensures optimum continuous operation after an initial start-up. The additional power and time required to generate $V_{\min}$ in Region I strongly depends on the rectifier and control loop implementation. This practical limitation will be discussed in more detail in Section V-A.

III. Circuit Design

A rectifier usually is designed for maximum performance in steady state for a given load voltage to current ratio. In this work however, the steady state performance is of little concern as no additional energy can be added to the storage capacitor once the capacitor is charged to the rectifier peak input voltage. Instead, the transient behavior must be optimized to reach steady state as fast as possible. The circuit design of an RF energy harvester in TSMC 90 nm CMOS technology is described in this section.

A. Single Stage Rectifier

The core of the harvester shown in Fig. 5 consists of a conventional cross-connected differential rectifier [13], [14]. In this structure, the output voltage and common-mode gate voltage generated during rectification provide additional biasing and effectively reduces the required turn-on voltage. Due to this V_{TH} self-cancellation, the rectifier can be activated at lower input power levels than other similar topologies [18]. Another benefit of the differential rectifier is its symmetry as it cancels all even order harmonic currents. In practice, this implies that it is sufficient to only suppress the 3rd harmonic in order to prevent power loss due to reradiation. This will be dealt with at the antenna-rectifier co-design in Section IV.

When the rectifier operates in the subthreshold region, the steady state output voltage is independent of the threshold voltage and device dimensions. These parameters only affect the input impedance and charging time as noticed in [19]. The charging time however, is mainly determined by the storage capacitance and available power. The required transistor width is determined by analyzing the relative charging curve for different input voltages. In Fig. 6, the simulated 90% charging time versus transistor width curves are normalized to the charging time for $W = 1$ μm for a rectifier input voltage of 200–600 mV. Here, the PMOS width is 2.5 times larger than of

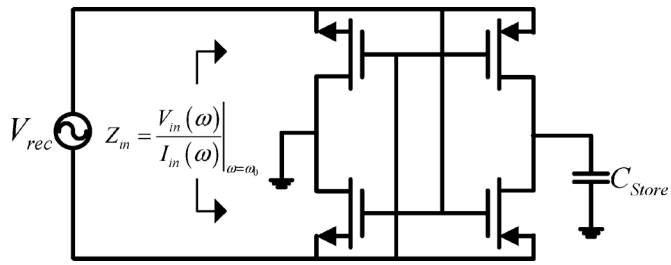


Fig. 5. Rectifier circuit implementation with V_{TH} self-cancellation [13].

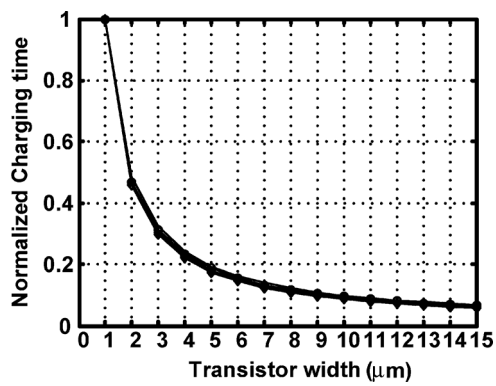


Fig. 6. Simulated normalized charging time versus transistor width for 200–600 mV input voltage.

an NMOS to compensate for the difference in hole and electron mobility. Note that the charging curves are nearly identical for all input voltages. This allows the designer to reduce the charging time by the same amount over a broad input voltage range for a given transistor width. In this work, a total transistor width of 6 μm (10 fingers) with minimum gate length is chosen as larger transistors do not significantly improve the charging time but will reduce the input reactance as the transistor parasitic capacitances dominate the rectifier impedance for $C_{\text{store}} \gg C_{par}$. The simulated voltage efficiency η_v of a single rectifying stage in this case is around 90%. The quasi steady state input impedance is calculated by the ratio of the FFTs of $V_{\text{in}}(t)$ and $I_{\text{in}}(t)$ at the operating frequency [20]. For an input voltage of 300 mV it is found that $Z_{\text{rec}} = 196.6 - j4896\ \Omega$.

B. Multi-Stage Rectifier

An output voltage higher than $\eta_v V_{\text{rec}}$ is achieved by cascading N rectifying stages. Coupling capacitors ensure that the

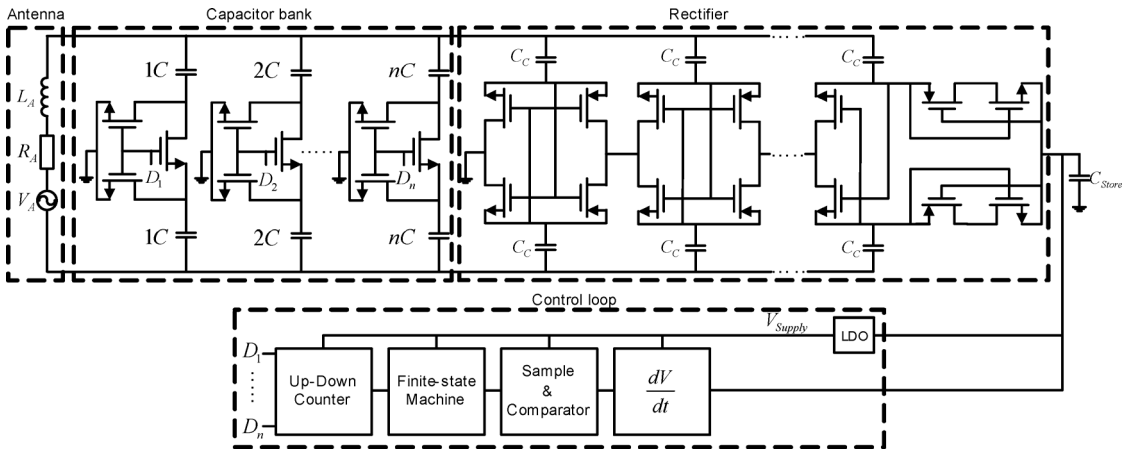


Fig. 7. Multi-stage RF energy harvester with complementary MOS diode in the last stage and control loop.

AC voltage is added in parallel while the rectified DC voltage of each stage is added in series with the previous stages (Fig. 7). The coupling capacitors are chosen to be 800 fF to avoid voltage division with the parasitic capacitors while keeping the chip area small.

Although the voltage gain of a cascade of rectifiers increases linearly with N, it also linearly decreases the input impedance. Consequently, the antenna resistance R_A needs to be scaled down with N as well to obtain conjugate matching, which decreases V_A for the same input power. The steady state output voltage for an N-stage conjugate matched rectifier with capacitive load can then be written as

$$V_{\rm out} = \sqrt{\frac{2P_{\rm av}\eta_A N}{R_{\rm rec,single}}} X_{\rm rec,single}\eta_v \tag{5}$$

where $R_{\rm rec,single}$ and $X_{\rm rec,single}$ are the rectifier input resistance and reactance of a single stage. The output voltage scales with $\sqrt{N}$ when including the interface passive voltage boost. Note that although the rectifier voltage efficiency η_v actually drops with decreasing power, simulations show that $\eta_v \geq 80\%$ when $V_{\rm rec} \geq 0.15$ V. Due to the large passive voltage boost, this voltage swing can be generated relatively easy even at power levels down to -30 dBm. Assuming $\eta_v > 80\%$ is therefore a reasonable assumption for the power levels of interest in this work.

Fig. 8 shows the calculated output voltage by using (5) for an N-stage rectifier at conjugate matching with $P_{\rm av} = -25$ dBm (3.16 μW), $\eta_A = 0.8$, $\eta_v = 0.9$ and a total additional capacitance of 350 fF, representing the additional capacitance associated with bondpads, ESD protection and tuning capacitance (to be discussed later).

The simulated 90% charging time is normalized to the charging time for N $=$ 1 to evaluate the increment with N. Note that the charging time increases rapidly with increasing N, which is mainly the result of the body effect of the NMOS transistors in the latter stages (assuming a standard process with $V_{bs,n} \neq 0$ V). The number of stages therefore is highly dependent on the required output voltage and charging time (update rate) of the application. A single stage rectifier with

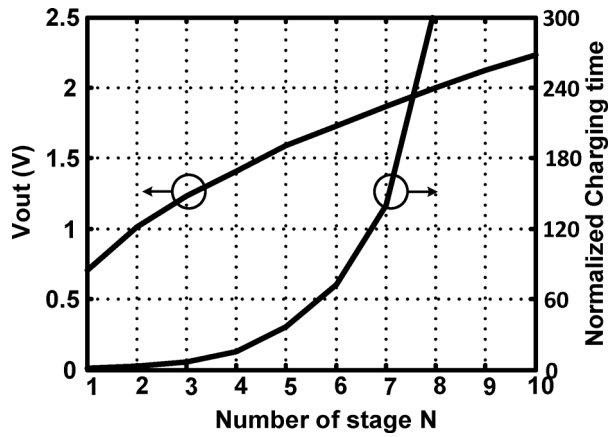


Fig. 8. Calculated $V_{\rm out}$ and simulated normalized charging time versus number of stages N for $P_{\rm av} = -25$ dBm.

$P_{\rm av} = -25$ dBm takes approximately 60 msec to fully charge a 450 nF storage capacitance to 0.7 V. A 7-stage rectifier however, can generate 1.85 V but takes approximately 8.5 seconds. This may be good enough for a simple wireless temperature sensor with low update rate, but is too slow for real-time monitoring of an electrocardiographic (ECG) signal. Adding just one more stage (Vout $=$ 2 V) would increase the charging time to 18.2 seconds. Hence, a high Q-network is preferred rather than using a large number of stages in order to improve performance. In this work, a rectifier structure with 5 stages is chosen to generate 1.5 V with reasonable charging time at low power levels like -20 dBm or less.

C. Rectifier Input Impedance

The simulated input impedance of the 5-stage rectifier is depicted in Fig. 9. In the subthreshold region ($V_{\rm rec} < V_{TH}$), the input impedance is dominated by the parasitic capacitance of the MOS transistors. As $V_{\rm rec}$ increases, the magnitude of $Z_{\rm rec}$ decreases as the transistors start to conduct more current. This causes a transformation in the real part of $R_{\rm rec} = \sqrt{|Z|^2 - X_{\rm rec}^2}$ and results in a significant increase of $R_{\rm rec}$. Nonetheless, an interesting fact is that both curves shift

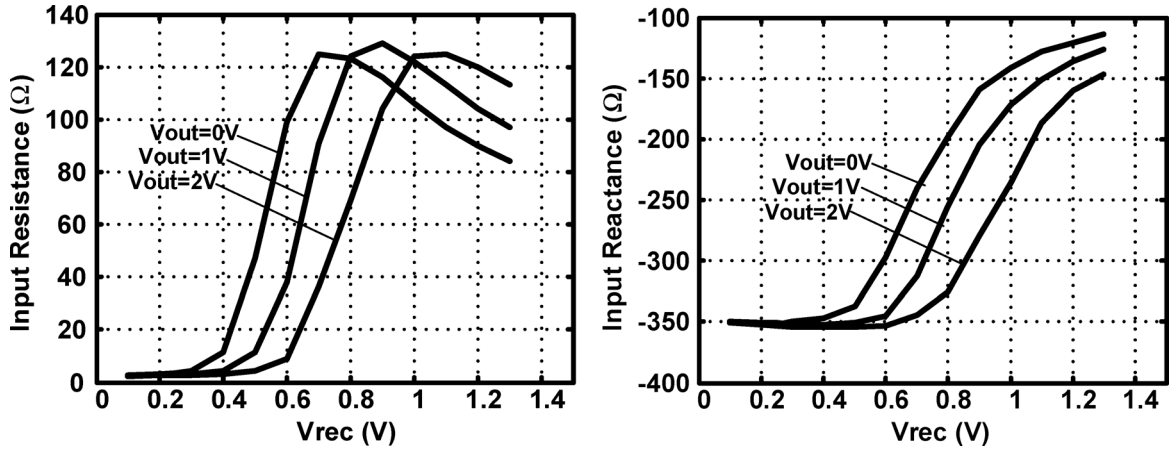


Fig. 9. Simulated input impedance versus $V_{\rm rec}$ and $V_{\rm out}$.

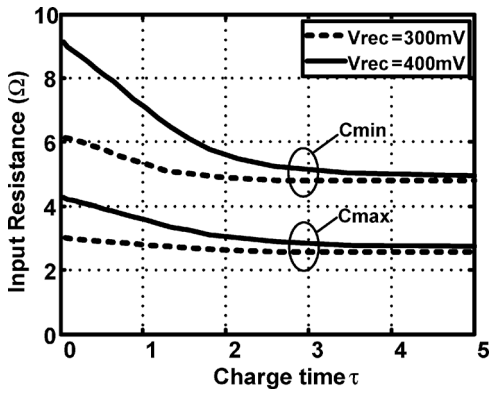


Fig. 10. Simulated input resistance during a complete charging period for different $V_{\rm rec}$ and tuning capacitance.

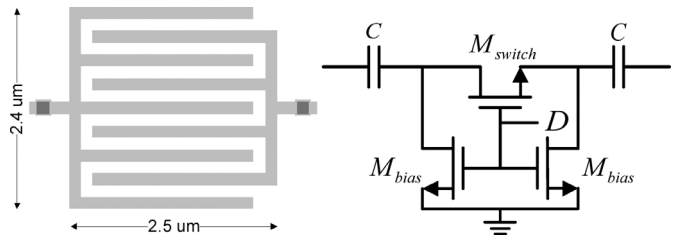


Fig. 11. Unit capacitance layout and nMOS switch implementation.

to the right when $V_{\rm out}$ increases due to the body effect and thereby partly compensates the increasing resistance.

Until this point in the design flow, an ideal independent voltage source has been used to simulate the rectifier input impedance. In reality, the inductive antenna limits the change in current and influences the input voltage during charging. To model this transient behavior, an inductance is added to the voltage source and is set to resonate with the rectifier reactance. Fig. 10 shows the simulated input resistance during a 5τ charging period for two values of $V_{\rm rec}$ and the minimum and maximum tuning capacitance. Note that $R_{\rm rec}$ slightly decreases and is almost constant for $V_{\rm rec} = 300$ mV. The variation in $X_{\rm rec}$ is only 3%. The interface impedance during charging is therefore relatively well defined at low power levels.

D. Switched Capacitor Bank

The impedance variations at the interface are compensated for by means of a binary-weighted capacitor bank parallel to the rectifier. The required tuning capacitance step $\Delta C_{\rm tune}$ is determined at low input power levels as the rectifier Q-factor is at its maximum in this region. Simulations show that a $\Delta C_{\rm tune}$ of 2 fF is sufficient to maximize performance for power levels down to -30 dBm. As such a small capacitance is not available in this design kit, two custom designed metal-metal capacitors are used in series as illustrated in Fig. 11. The capacitor is realized using metal 6 and 7 stacked together with minimum width and spacing to minimize parasitics. With an area of 2.4×2.5 μm, the post-layout simulated capacitance is found to be 4 fF.

Each unit cell consists of two capacitors, a main switching transistor ($M_{\rm switch} = 1/0.1$) and two small biasing transistors ($M_{\rm switch} = 0.2/0.1$) to enhance the Q-factor. With a voltage of 0.7 V as D = '1', the post-layout Q-factor is >100 over all process corners. The on-off capacitive tuning ratio $C_{\rm on}/C_{\rm off}$ in this case equals 2.2. The number of bits is determined by the desired tuning range and voltage boost. If too many capacitances are added in parallel to the rectifier, it reduces the available voltage boost at the interface. It was chosen to use a 7-bit capacitor bank consisting of 127 unit capacitor switches where $C_{\rm max} = 256$ fF and $C_{\rm min} = 116$ fF. This results in a tuning range in reactance of $340\ \Omega \leq X \leq 460\ \Omega$ for the rectifier and antenna as $X_{\rm rec} = X_A$.

E. Reverse Current Leakage Reduction

The harvester's ability to store and hold the energy over a long period of time is another very important aspect that is not discussed often in the literature. This allows a WSN to operate and re-activate the control loop after a long period of time without sufficient power for rectification. To minimize the current leakage of the external storage capacitor itself, a polyester (PET) film capacitor is used with a minimum insulation resistance of 10 GΩ. The second dominating leakage mechanism occurs when $V_{\rm rec} \ll V_{\rm out}$ when for example the available input power suddenly drops with several dB. This results in a negative gate-source voltage of the pMOS transistors in the last stage

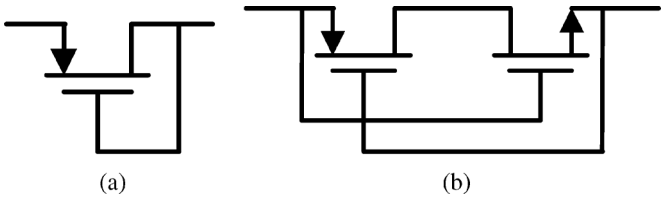


Fig. 12. Conventional (a) and complementary (b) diode connected MOS transistor.

and causes current to flow from the capacitor back into the rectifier. This issue often is solved by replacing the pMOS transistors with conventional diode-connected transistors (Fig. 12(a)) at the expense of a lower power efficiency. At reverse biasing ($V_{GS} = 0$), the reverse current is mainly determined by the threshold voltage as the subthreshold current of a pMOS is given by

$$I_{D,p} = \frac{W}{L} I_0 e^{\frac{-V_{GS}+V_{TH}}{nV_t}} \left(1 - e^{\frac{V_{DS}}{V_t}}\right) \quad (6)$$

where I_0 is the technology related characteristic current, W and L are the transistor width and length, V_{TH} is the threshold voltage, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, n is the subthreshold slope and V_t is the thermal voltage. Ultra-low threshold voltage (ULVT) transistors may be used to lower the voltage drop but will exponentially increase the current leakage.

The complementary diode shown in Fig. 12(b) is used to overcome the aforementioned drawbacks. This circuit topology is proposed for memory cell applications [22], but can also be used for high-frequency rectification. For complementary pMOS and nMOS, the structure behaves as a single diode when forward biased. For reverse biasing however, the current initially increases due to increasing $V_{DS,p}$ and then strongly decreases as $V_{GS,p}$ becomes more and more positive. Due to the symmetry of the circuit, exactly the opposite holds for the nMOS transistor as $V_{GS,p} = -V_{GS,n}$ and $V_{DS,p} = -V_{DS,n}$. A combination of ULVT and LVT transistors is sized to realize symmetrical devices with $V_{TH} = \pm 0.4$ V.

The simulated I-V characteristics of the two diode implementations are shown in Fig. 13. The reverse current of the conventional MOS diode actually increases with a larger reverse bias voltage due to the body effect. The complementary diode however, strongly benefits from the exponential current reduction at reverse biasing. The reverse current at $V_{\text{diode}} = -0.6$ V equals 6 nA for the conventional diode and only 2.6 pA for the complementary diode, providing more than three orders of magnitude in reverse current reduction.

F. Control Loop

The loop consists of a 7-bit binary-weighted capacitor bank that is controlled by an up-down counter. The harvester initially charges the storage capacitor to the turn-on voltage of the loop. Then the energy transfer to the off-chip capacitor is optimized by maximizing the slope of the load voltage. A possible control loop implementation in combination with a multi-stage rectifier including reverse leakage reduction is shown in Fig. 7.

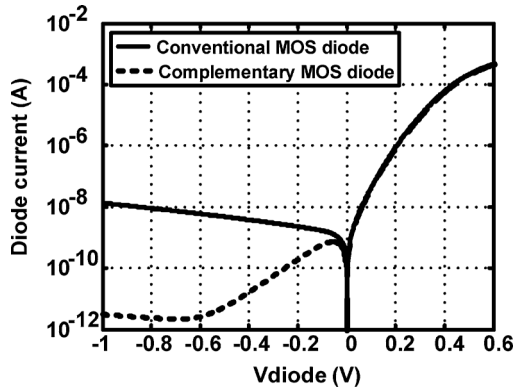


Fig. 13. Simulated diode characteristics for a conventional and complementary MOS diode.

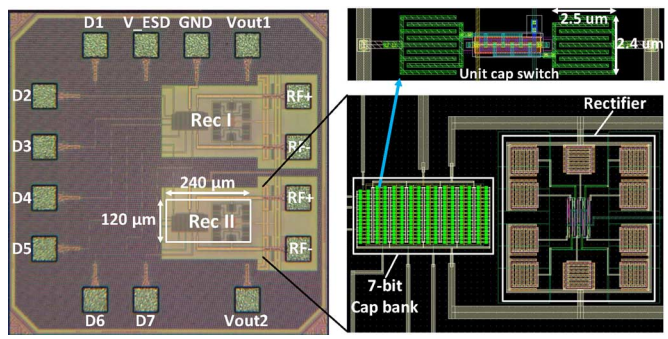


Fig. 14. Chip microphotograph and layout details.

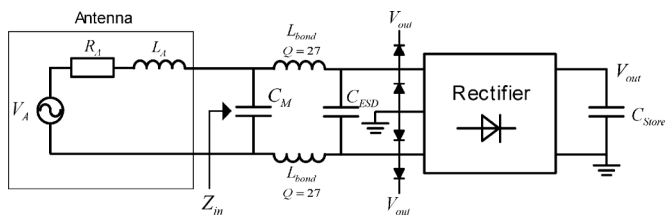


Fig. 15. Antenna-chip interface model with parasitic components.

The slope information is obtained using a differentiating network. Subsequently, a sample & comparator stage compares the slope information with the previous sample and determines if the slope has increased or decreased. This information is fed to a finite-state machine that determines if the up-down counter should keep counting or change count direction. A more detailed description on how the loop can compensate for antenna impedance variations can be found in [21], [23].

As a proof of principle, the control loop is implemented off-chip using a micro controller. However, preliminary simulation results show that a similar mainly digital control loop can also be implemented on-chip. When optimizing for low leakage current, the average power of the control loop can be in the order of 30 nW due to the relaxed requirements on the clock speed and accuracy ($\sim$ kHz range). The loop can be activated around 300 mV, meaning that the storage capacitor should not be discharged lower than this voltage to ensure continuous operation. Once the loop is calibrated, it can be duty-cycled or turned off so that it is not loading the rectifier for very low input power levels.

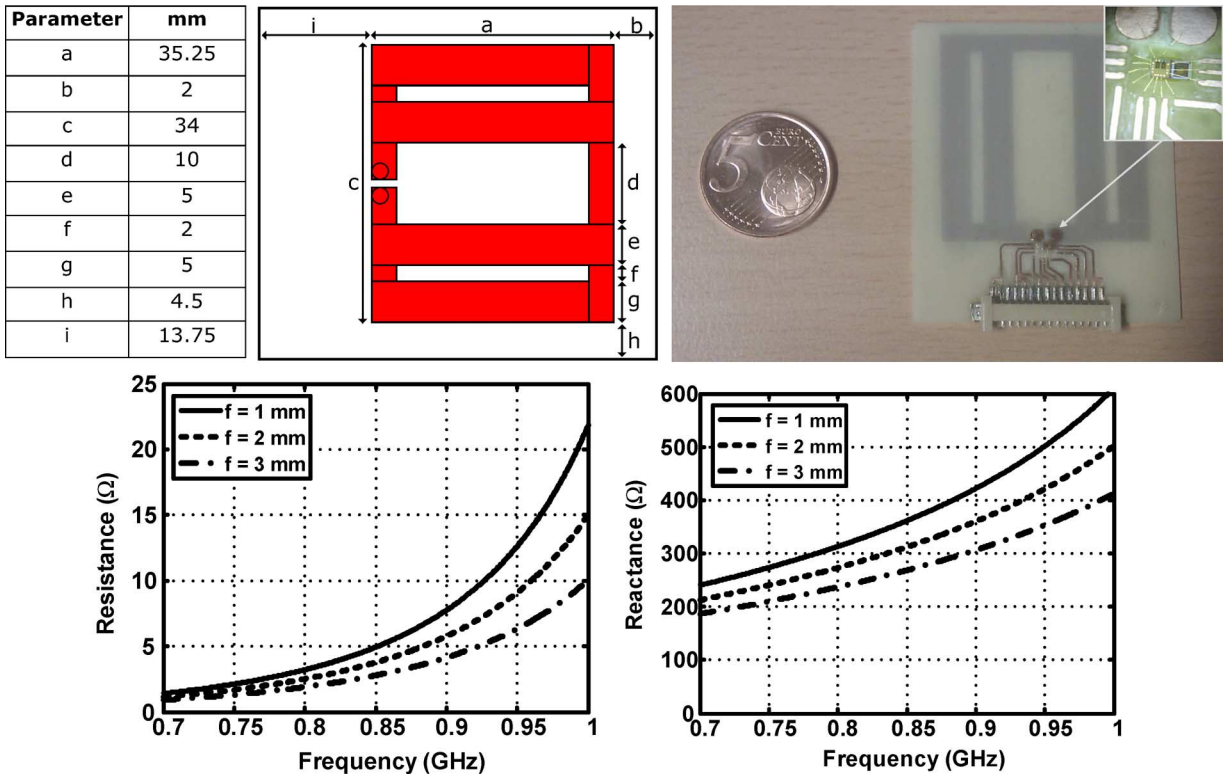


Fig. 16. Proposed antenna structure, dimensions and simulated input impedance with integrated chip on the backside.

G. Layout Design and Parasitic Components

Two rectifiers with the 7-bit capacitor bank have been implemented in TSMC 90 nm CMOS technology. The first implementation (Rec I) uses the conventional differential rectifier shown in Fig. 5 while the second implementation (Rec II) includes the complementary diode in the last stage as depicted in Fig. 7. Since the input impedance is mainly determined by the rectifier parasitic capacitances, careful layout is essential. The high required quality factor of the IC's input impedance is achieved by optimizing the number of fingers and using sufficiently wide metal connections. A symmetrical and interdigitated layout further improves device matching. The top plate of each metal-insulator-metal (MIM) coupling capacitor is connected to the antenna side to prevent the larger bottom-plate parasitic capacitance from additionally shunting the capacitor bank.

The RF bondpads are custom designed to minimize the parasitic capacitance and include ESD protection. The ESD diodes are biased at the lowest and highest generated voltage in the circuit (GND and $V_{\rm out}$) as illustrated in Fig. 15. The extracted bondpad capacitance is 191 fF and is modeled with $C_{\rm ESD} = 95.5$ fF as the two ESD diode capacitances are connected in series via the ground terminal. An external supply is used to bias the ESD control pins D1–D7. The bondwires to the antenna feedpoint are approximately 1.5 mm in length each and are modeled with an inductance of $L_{\rm bond} = 1.5$ nH with 0.3 Ω loss resistance. The bondwire mutual capacitance is modeled with $C_M = 25$ fF. The post-layout input impedance seen from the antenna feedpoint for $V_{\rm rec} = 300$ mV is found to be $Z_{in,0} = 7.6 - j418\,\Omega$ for $C_{\rm min}$ and $Z_{in,1} = 4.3 - j310\,\Omega$ for $C_{\rm max}$.

IV. Antenna-Rectifier Co-Design

Given the post-layout simulated rectifier input impedance as described in the previous section, the required antenna impedance is set to $Z_A = 4.3 + j350\,\Omega$ at 868 MHz. The exact value of the reactance is not very critical as the control loop will ensure resonance. The antenna resistance is set to $R_A = 4.3\,\Omega$ in order to prevent that $R_A < R_{\rm rec}$ as discussed in Section II-A. The power loss due to the resistive mismatch at higher input powers is then compensated for by the increased available power.

The proposed antenna structure in Fig. 16 is a compact square loop antenna with additional short-circuited arms. These arms can provide fine tuning of the antenna impedance by for example varying parameter f. After optimizing all antenna parameters (dimensions, substrate thickness and permittivity), it is decided to use 0.5 mm thick GML 1000 substrate ($\epsilon_r = 3.05$ and $\tan\delta = 0.003$) for high radiation efficiency. The antenna impedance is simulated in CST Microwave Studio using frequency, transient and transmission line solvers and all converge to approximately $Z_A = 4.4 + j328\Omega$, thereby ensuring a high degree of confidence in the simulation results. At the 3rd harmonic (2.604 GHz), the simulated antenna and rectifier impedance are 92.0+j12.7 Ω and 1.78–j124.5 Ω, respectively. This causes a highly mismatched interface which attenuates the harmonic currents produced by the rectifier with 15 dB and thereby minimizes power loss due to reradiation. In addition, the power contained at the 3rd harmonic is relatively small for the power levels discussed in this work.

Fig. 17 illustrates the elevation plane radiation pattern (theta versus antenna gain G_A in dBi) and the 3D directivity to give

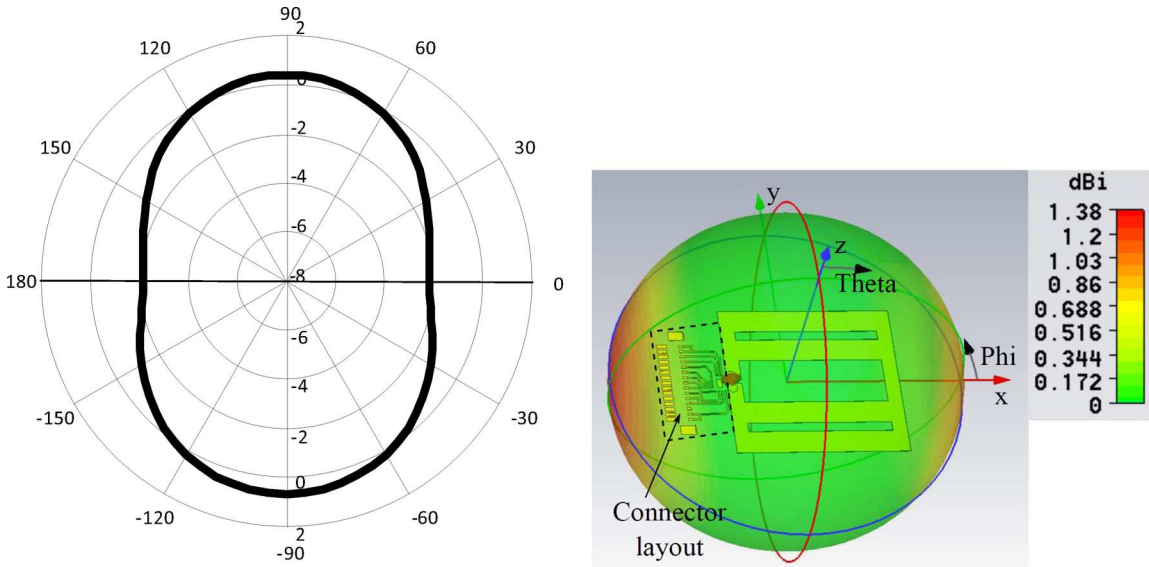


Fig. 17. Simulated elevation plane radiation pattern (theta versus antenna gain G_A in dBi) and 3D directivity pattern.

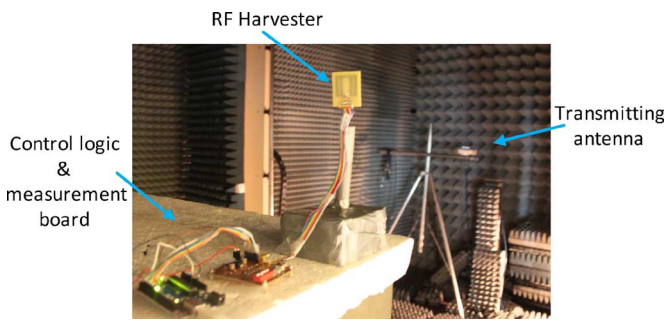


Fig. 18. Measurement setup in anechoic chamber.

insight in the directional dependence. The proposed antenna is horizontally polarized and has a maximum antenna gain of 0.659 dBi, corresponding to 84.7% radiation efficiency.

The chip is integrated on the backside of the antenna to minimize its effect on the radiation characteristics. The RF inputs are bond wired to vias (2 mm in diameter) that connect to the antenna feed point. In this prototype, the control and output signals are connected to a measurement board via a connector. Once the control loop is completely integrated on chip and the connector is no longer required, it is expected that the antenna area can be scaled down further without significant performance loss.

V. Experimental Results

The RF energy harvester performance first was measured in an anechoic chamber to mimic free space conditions. Then, the harvester was measured in a realistic office environment. The following measurement results are obtained using the harvester with rectifier II (complementary MOS diode) implementation unless stated otherwise. The RF energy harvester is positioned for optimal directional alignment and polarization with respect to the transmitting antenna. As the control loop is off-chip, its power consumption during calibration is not included in the measurements.

A. Measurements in Anechoic Chamber

The setup is calibrated at 868 MHz using two identical broadband log periodic antennas (HG824-11LP-NF) separated by 3.6 meter to ensure far-field conditions. Since the harvesting antenna dimensions are much smaller than the wavelength ($\mathrm{a} = \lambda/9.8$ and $\mathrm{c} = \lambda/10.2$), the antenna performance is included in the measurements by defining the input power as the maximum power available from an impedance and polarization-matched isotropic antenna ($G_A = 0$ dBi). This power is determined by measuring the received power using the reference antenna at the harvester position and subsequently subtract the reference antenna gain to obtain $P_{\mathrm{in}} = P_{\mathrm{av,iso}}$. The measured power is within ± 0.5 dB agreement with the theoretical available power calculated from (1).

Fig. 19 shows the measured output voltage for an optimizing control loop and a capacitance sweep for $R_{\mathrm{load}} = 1\mathrm{M}\ \Omega$ and $P_{\mathrm{in}} = -20$ dBm. During a capacitance sweep, the control loop is continuously counting from the minimum to the maximum capacitance value. Clearly, an optimum capacitance exists that corresponds to maximum power in the load. In de second measurements, the loop optimization is activated at 0.5 seconds and maximizes the power dissipation in the load.

The measured output voltage versus input power for different load resistances in Fig. 20 shows excellent sensitivity at low power levels. The unloaded performance of Rec I and Rec II are very similar and both are able to generate 1 V with approximately -27 dBm input power.

The efficiency of the RF energy harvester needs to be defined carefully. When the energy efficiency is defined as the ratio of the stored energy in the capacitor over the integral of the available power, it is required to specify the integration time. Hence, this efficiency definition becomes arbitrary and therefore difficult to compare in a fair way to previous work. Moreover, the energy efficiency approaches 0% for a long integration time as no additional energy can be stored when the capacitor is fully charged.

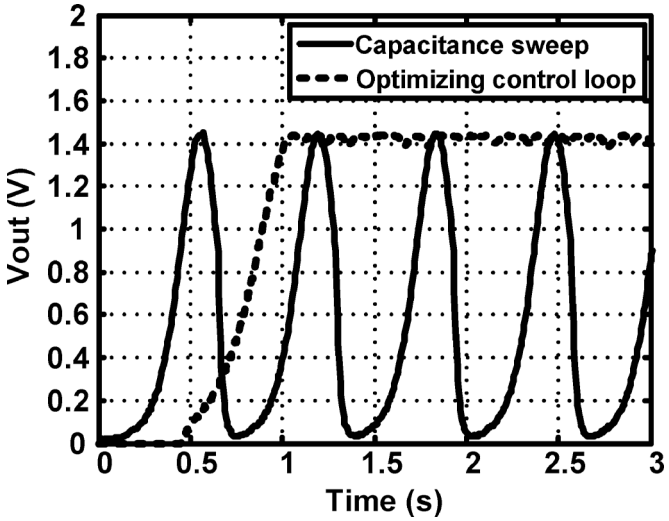


Fig. 19. Measured $V_{\rm out}$ for capacitance sweep and optimizing control loop, $R_{\rm load} = 1$ MΩ and $P_{\rm in} = -20$ dBm.

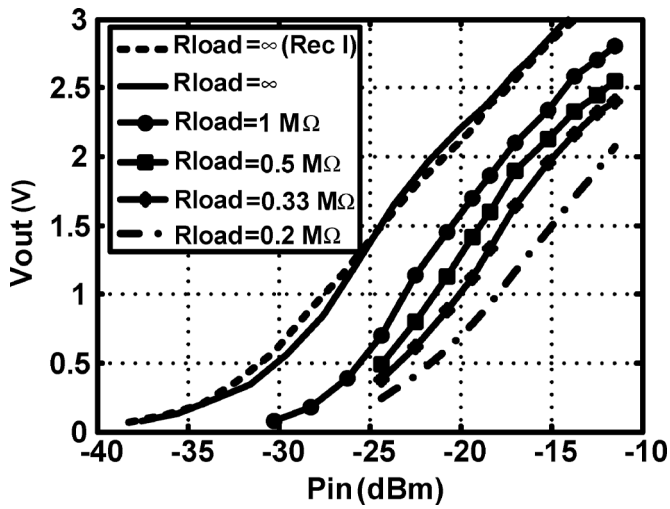


Fig. 20. Measured $V_{\rm out}$ for different $R_{\rm load}$ versus $P_{\rm in}$.

In this work, the RF-DC power conversion efficiency (PCE) is defined using a resistive load

$$PCE = \frac{P_{\rm load}}{P_{\rm av,iso}} = \frac{V_{\rm out}^2}{R_{\rm load} P_{\rm av,iso}}. \quad (7)$$

Fig. 21(a) shows that the PCE peaks around -17 dBm with a maximum of 40% for a load resistance of 0.33 MΩ. This includes all losses of the antenna, interface and rectifier. The 10–90% charging time versus Pin for a 450 nF load capacitance is shown in Fig. 21(b). Evidently, the charging time increases due to the decreasing input power and hence lower PCE. As the charging time scales linearly with capacitor size, Figs. 20 and 21(b) give a good indication of the available energy as a function of input power and time.

The harvester frequency response is obtained after calibrating the setup over frequency and is depicted in Fig. 22 for two scenarios. In the first scenario, the control loop is active and adapts the antenna-rectifier interface. The -3 dB bandwidth in this case is approximately 60 MHz for a 1 MΩ load resistance and -20 dBm input power. The maximum output peaks at 855 MHz, slightly lower than the 868 MHz used for the measurement in this work. To compare this to a static antenna-rectifier interface, a second measurement is performed where the capacitor bank is tuned to maximize the output at the 868 MHz band. Evidently, the control loop more than doubles the bandwidth of the RF energy harvester compared to the static interface scenario.

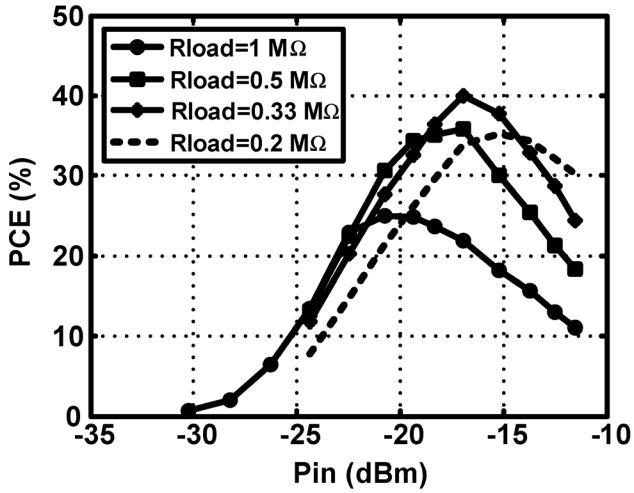
In order to test the performance with zero initial energy stored in the capacitor (i.e., control loop is off, D = '0'), three measurements are carried out to find the required initial start-up power and charging time to reach the start-up voltage of the control loop for $V_{\rm min} = 0.5$, 0.6 and 0.7 V. When $V_{\rm out} > V_{\rm min}$, the off-chip micro controller activates the control loop and optimizes the interface as shown in Fig. 23. When for example $V_{\rm min} = 0.5$ V, the RF energy harvester needs an initial start-up power of -24 dBm and 21.5 sec charging time in order reach $V_{\rm min}$ and to activate its control loop. This demonstrates the feasibility and limitations of a WSN under worst case conditions.

To test the energy storage capabilities of the harvester over a long period of time, the two RF harvester implementations with $C_{\rm store} = 350$ nF initially are charged to three different values of $V_{\rm out}$. Then, the signal generator is switched off and $V_{\rm out}$ is measured as a function of time. As an example, the discharge curves in Fig. 24 show that for an initially stored voltage of 1.5 V, the capacitor is discharged to 0.5 V after approximately 75 seconds for Rec I. The harvester implementation with Rec II is able to store the energy significantly longer. The discharge time to 0.5 V for the same initial voltage is now more than 4.1 hours. This greatly improves the functionality and practical use of the RF energy harvester in a WSN and demonstrates the advantage of using the proposed complementary diode.

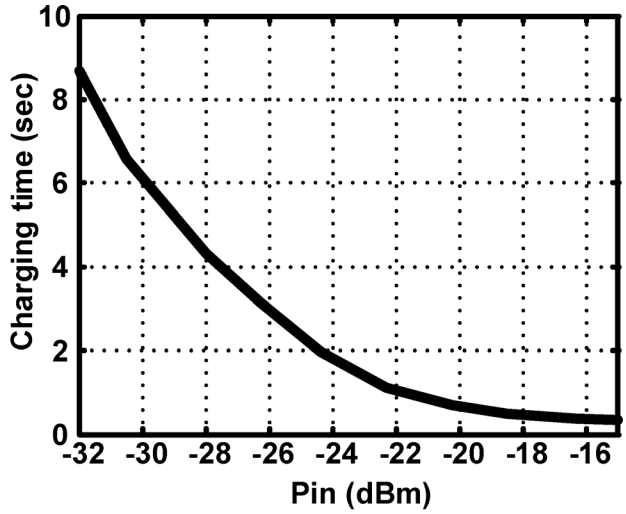
B. RF Energy Harvesting in a Realistic Environment

To test the harvester in a realistic environment, a 1.78 W EIRP dedicated RF source at 868 MHz was used to measure $V_{\rm out}$ versus line-of-sight distance in an office corridor for a capacitive load. Fig. 25 illustrates the measured data points with curve fitting and the theoretical $V_{\rm out}$ in free space calculated from the measured sensitivity in Fig. 20. On average, the performance is better than in free space condition for distances closer than 27 meters from the RF source. This may be explained by the waveguide effect of the corridor, where high power density waves reflect from the walls, floor and ceiling and contribute to the total available power. In this experiment, 1 V could be generated at 27 meter distance. Due to limitations of the measurement equipment it was not possible to transmit at the maximum allowed radiated power of 3.28 W in the European ISM band, which would theoretically result in a 1.4× larger range.

The energy harvesting from ambient RF sources is demonstrated by measuring the output voltage when using a GSM-900 mobile phone from 2 meter distance (Fig. 26). Although the frequency and power levels varied greatly during a call (peak power levels of -4.6 dBm were measured between 886 MHz and 907 MHz), we observed that it is feasible to charge a capacitor to 2.2 V.



(a)



(b)

Fig. 21. (a) Measured power conversion efficiency and (b) 10–90% charging time versus $P_{\rm in}$.

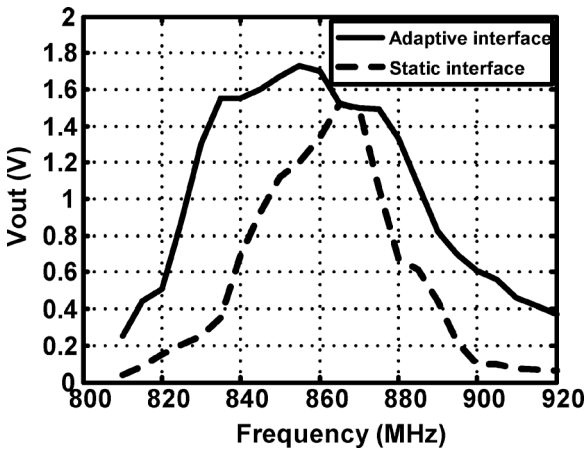


Fig. 22. Measured frequency response for $R_{\rm load} = 1$ MΩ and $P_{\rm in} = -20$ dBm.

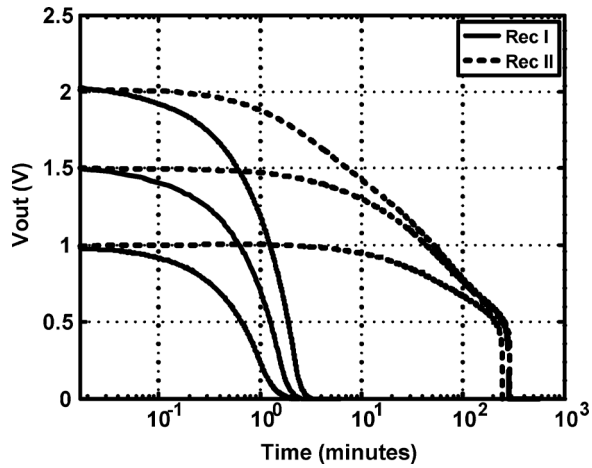


Fig. 24. Measured discharge time for Rec I & II for $C_{\rm store} = 350$ nF.

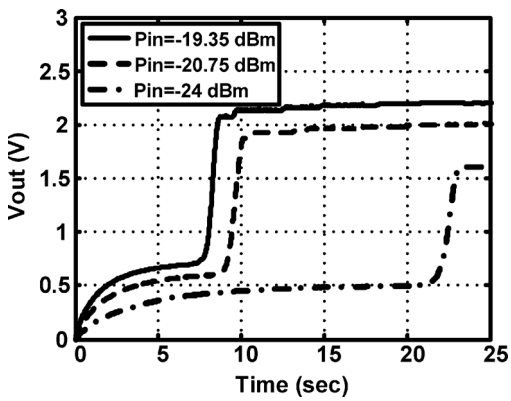


Fig. 23. Measured minimum $P_{\rm in}$ for zero energy initial condition for$V_{\rm min} =$ 0.5, 0.6 and 0.7 V.

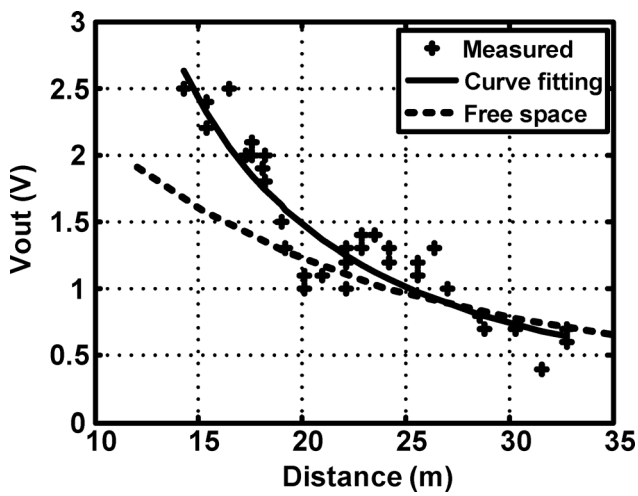


Fig. 25. Measured output voltage versus distance in an office corridor for $P_{\rm EIRP} = 1.78$ W and $C_{\rm store} = 350$ nF.

C. Comparison With Previous Work

Table II shows a comparison with state-of-the-art CMOS RF energy harvesters. This work shows superior wireless range performance and demonstrates a -27 dBm sensitivity for 1 V output in an anechoic chamber and 27 meter range from a 1.78 W RF source in an office corridor. Also, a PCE of 40% at -17 dBm is among the highest reported in the literature. The rectifier and capacitor bank are implemented in standard CMOS technology, occupying only 0.029 mm^2 and requires no calibration procedure. Moreover, the proposed antenna is

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

Parameters	This work	T. Le '08 [12]	J. Yi '07 [10]	S. Mandal '07 [15]	G. Papotto '11 [16]
Technology	90 nm	0.25 μm	0.18 μm	0.18 μm	90 nm
Die area	0.029 mm^2	0.4 mm^2	0.084 mm^2	n.a.	0.19 mm^2
Antenna area	21.9 cm^2	30 cm^2	n.a.	37.4 cm^2	no antenna
Frequency	868 MHz	906 MHz	900 MHz	970 MHz	915 MHz
Rectifier stages	5	36	24	2	17
Requirement	Control loop	External pre-charge	Zero V_{TH} transistor	-	Deep n-well
Sensitivity ($R_{load} = \infty$)	-27 dBm for 1V	-22.6 dBm for 2V	n.a.	-17.7 dBm for 0.8V	-24 dBm for 1V
Measured distance	27 meter @ 1.78 W	15 meter @ 4 W	1.1 meter @ 0.32 W	n.a.	none
Max PCE	40% @ -17 dBm	30%$^{(a)}$ @ -8 dBm	26.5 % @ -11 dBm	37%$^{(a)}$ @ -18.7 dBm	16.1% @ -15.83 dBm

$^{(a)}$Calculated from graph

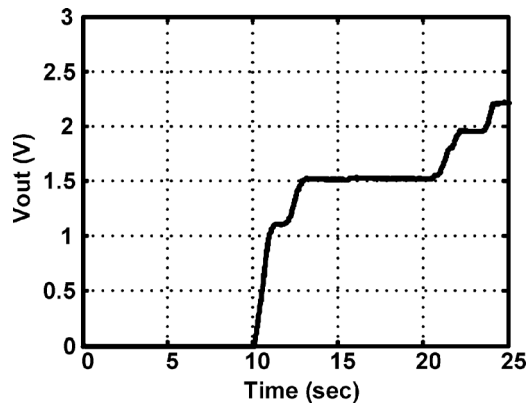


Fig. 26. Ambient RF energy harvesting from a GSM-900 mobile phone at 2 meter distance.

respectively 37% and 70% smaller than the ones used in [12] and [15], even though the operating frequency is lower.

VI. CONCLUSION

The co-design of a CMOS rectifier and a small loop antenna for a highly sensitive RF energy harvester has been presented. First, a design methodology is described to optimize the antenna-rectifier interface by using a low resistive and high-Q interface. Subsequently, a 5-stage cross-connected differential rectifier with complementary MOS diode in the last rectifying stage is designed that significantly improves the harvester's ability to store and hold energy over a long period of time. A control loop with 7-bit binary-weighted capacitor bank compensates variation at the interface while benefiting from the larger passive voltage boost to improve the sensitivity.

The chip is implemented in standard TSMC 90 nm CMOS technology, includes ESD protection and is directly mounted on the backside of the antenna. Measurements in an anechoic chamber at 868 MHz demonstrate an end-to-end maximum PCE of 40% and a sensitivity of -27 dBm to generate 1 V across a capacitive load. In an office corridor, 1 V could be generated from a 1.78 W RF source at 27 meter distance.

ACKNOWLEDGMENT

The authors would like to thank W. Straver and A. Kaichouhi for their help and suggestions during the antenna-chip integration. The help from P. Aubry and J. Zijderveld from the Delft University Chamber for Antenna Test (DUCAT) is also much appreciated.

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