Low-Dropout Regulators: Hybrid-Cascode Compensation to Improve Stability in Nano-Scale CMOS Technologies

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Abstract—**A modified circuit-level strategy to improve the speed/stability trade-off of low-dropout regulators is presented. The technique, called hybrid-cascode compensation, is applied to stabilize the regulation loop. When designed carefully, results prove the efficacy of this method in minimizing output settling time under various transient conditions. Equivalently, power consumption and/or die area can be minimized for the same settling time. Employing this technique, a 0.7V-10mA voltage regulator with a minimum line voltage of 1V has been designed in 90nm CMOS technology. With improved settling time, stability is guaranteed for load capacitors as low as 50pF. Power supply rejection is always better than -30dB for all frequencies.**

I. Introduction

Switching regulators can regulate an input supply voltage with power efficiencies reaching from 70 to 95 percent [1]. Nonetheless, the noise caused by the switching activity of the power switches aggravates the signal quality of sensitive analog circuits. To avoid assigning a major portion of the noise budget into that of noise injected by the power supply, switching regulators are often not considered as the main power source delivering energy into low-noise blocks. A low-dropout regulator (*LDO*) is thus employed to smoothen out the fluctuations of an unregulated input supply [1-4]. An important design criterion for LDOs is to guarantee loop stability under different loading conditions. In this paper, a modified technique, called hybrid-cascode compensation, is introduced to stabilize the loop. The results demonstrate that the technique can be advantageous in improving track bandwidth for the same power consumption and chip area.

The rest of the paper is organized as follows. Section II discusses the merits of the proposed technique to stabilize an *LDO*. Comparisons with previously known techniques are made to theoretically clarify the benefits of hybrid-cascode compensation. Using this technique in Section III, a low-noise architecture with improved track bandwidth is designed. Simulation results in 90nm CMOS technology are provided. Finally, conclusions are drawn in Section IV.

II. Stability and Transient Response of LDOs

Fig. 1 depicts the basic structure of an *LDO*. In this circuit, the main processing units are passing device M_P to steer the current from the input supply (V_{DD}) to the load, resistive feedback network R_1 and R_2 to scale the output voltage V_{out}, and an error amplifier to evaluate the difference between a reference voltage V_{ref} and a scaled version of V_{out}. An error signal is then generated by the error amplifier to control the current of M_P. In principle, a regulation loop contains at least two low-frequency poles. With parasitic poles taken into account, an *LDO* thus can be unstable if no frequency compensation technique is applied. A conventional method to stabilize *LDO*s is to implant a low-frequency zero into the transfer function. This counteracts the additional negative phase shift caused by the poles and increases the phase margin. As shown in Fig. 1, the zero can be realized using a load capacitor with an appropriate Equivalent Series Resistance (*ESR*). To improve the transient response of the regulated output, the capacitor should be selected as large as possible. With enough charge stored in it, the required load current in presence of high-frequency load current/line voltage changes can thus be provided. A large load capacitor also reduces output noise and improves power-supply rejection (*PSR*) at higher frequencies. Due to the size of the capacitor however, this technique cannot be considered as solution for

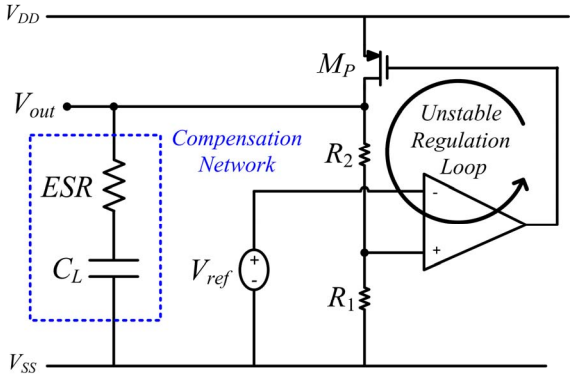


Figure 1. A typical *LDO*

an on-chip design.

Recently-proposed techniques to stabilize *LDO*s take advantage of the Miller effect of a small capacitor to virtually increase its value up to several hundred times larger. In its simplest form, although the problem of stability could be solved, it suffers from a poor transient response. Hence, a current buffer is usually placed in series with the Miller capacitor to efficiently decrease its loading effect on the circuit. This technique, called cascode compensation, proved to be useful in silicon implementation [4,5].

In this paper, with the aim to further improve the output settling time of an *LDO*, the efficiency of another method called hybrid-cascode compensation will be investigated. Fig. 2 illustrates a simple regulator either stabilized by cascode compensation or by hybrid-cascode compensation. As for the cascode compensation in Fig. 2a, common-gate device M_{i4} conveys the current of C_C into node *x*. Solving small-signal equations, the loop gain of this topology is

$$\frac{V_{fb}}{V_{in}} \approx \frac{LG_0(1+s^2/z^2)}{(1+s/\omega_0).(1+s(2\xi/\omega_n)+s^2/\omega_n^2)}, \quad (1)$$

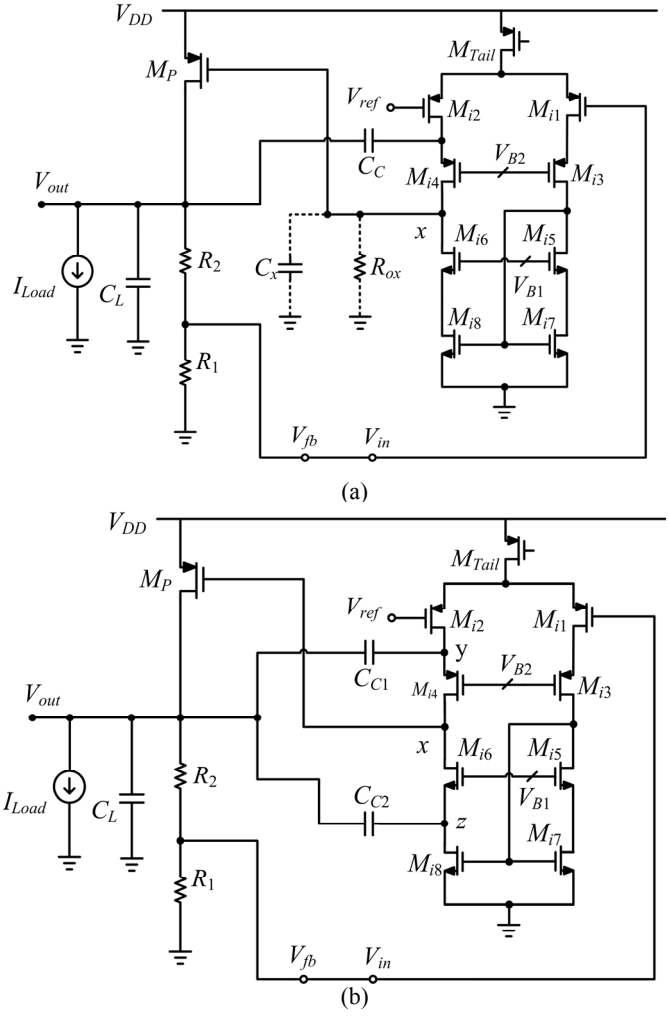


Figure 2. Topology of a simple voltage regulator either stabilized by
(a) cascode compensation
(b) hybrid-cascode compensation

where

$$LG_0 = \beta g_{mi1} g_{mP} R_i (r_{DS,p} \,||\, (R_1 + R_2)), \quad (2)$$

$$z = \sqrt{g_{mi4} g_{mP} / C_x C_C}, \quad (3)$$

$$\omega_0 = \frac{1}{R_{ox}(C_x + g_{mP}(r_{DS,p} \,||\, (R_1 + R_2))C_C)}, \quad (4)$$

$$\omega_n = \sqrt{\frac{g_{mi4} g_{mP}}{C_x (C_C + C_L)}}, \quad (5)$$

$$\xi\omega_n = \frac{1}{2}\frac{g_{mi4}}{C_C}. \quad (6)$$

In the above equations, the transconductance of each device is denoted by its corresponding g_m. β refers to the feedback factor. R_{ox} and $r_{DS,p}$ are respectively the output resistance of the first stage and of device M_P. Other circuit elements are illustrated in Fig. 2. ξ and ω_n, as shown in (1), are the damping factor and natural frequency of the non-dominant poles, the values of which can be evaluated from (5) and (6).

Similar to the feedback mechanism of cascode compensation, the role of M_{i4} and M_{i6} in Fig. 2b is to buffer the current of the two compensation capacitors C_{C1} and C_{C2} respectively. In this implementation, there are two separate *ac* paths to feed the output signal back into node *x*. To obtain an estimated loop gain function of this technique, and also to gain more insight into the advantages of Fig. 2b over Fig. 2a, the capacitive feedback network of Fig. 2b is shown in Fig. 3. Strictly speaking, a limiting factor to improve the transient response of this transfer function is a doublet appearing in the transfer function [6]. This doublet originates from the time constant difference of the two paths. Equating the time constants ($g_{mi4}/C_{C1} = g_{mi6}/C_{C2}$), one can conclude that if

$$C_{C1} = \frac{C_{C1} + C_{C2}}{1 + g_{mi6}/g_{mi4}}, \quad (7)$$

$$C_{C2} = \frac{C_{C1} + C_{C2}}{1 + g_{mi4}/g_{mi6}}, \quad (8)$$

the doublet will be completely eliminated and the transient response is optimized. When this happens, the transfer function of Fig. 2b would be the same as (1). Equations (2) to (6) are also valid if C_C and g_{mi4} are replaced by $C_{C1}+C_{C2}$ and $g_{mi4}+g_{mi6}$ respectively. For instance, if the total compensation capacitor is kept constant (i.e. $C_C = C_{C1}+C_{C2}$),

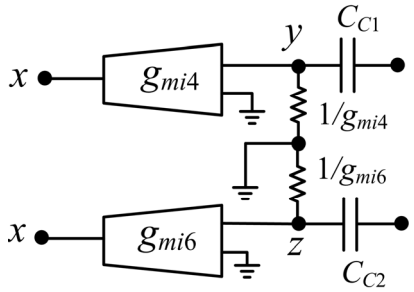


Figure 3. The capacitive feedback network of Figure 2b

by assuming $g_{mi4} = g_{mi6}$ the real part of the two non-dominant poles ($\xi\omega_n$ in (6)) becomes

$$\xi\omega_n = \frac{1}{2}\frac{g_{mi4}+g_{mi6}}{C_C} = \frac{g_{mi4}}{C_C} = 2(\xi\omega_n)_{Cascode}. \quad (9)$$

In contrast with cascode compensation, the real part of the non-dominant poles in hybrid-cascode compensation is about two times larger in magnitude.

According to (5), the absolute value of the non-dominant poles (ω_n) is also bigger

$$\omega_n = \sqrt{\frac{(g_{mi4}+g_{mi6})g_{mP}}{C_x(C_C+C_L)}} = \sqrt{2}(\omega_n)_{Cascode}. \quad (10)$$

Based on (9) and (10), for equal area and power consumption, the phase margin of a hybrid-cascode compensated *LDO* is larger than of a conventionally-designed cascode compensated *LDO* (larger bandwidth). If the required phase margin (stability) is considered constant, a design employing hybrid-cascode compensation achieves it with lower power consumption (smaller g_m's) and so forth.

From the point of large-signal transient response (the response to abrupt changes of the load current and line voltage), hybrid-cascode compensation is also a good choice. To demonstrate this, consider Fig. 2a when technology limitations impose the value of the load capacitor (C_L) to be a few tens of pico-farads. Under these circumstances, if I_{Load} abruptly increases, depending on the bandwidth, the regulation loop would need a considerable amount of time to damp the variation. During this time period, the current flow from M_P remains unchanged. Hence, V_{out} decreases quickly to provide the rest of the required I_{Load} via a charge stored on such a small C_L. As the voltage across C_C does not change abruptly, the change in V_{out} is transferred to the source of M_{i4}, resulting a lower source voltage. Hence, the input current into node x becomes smaller as well. The difference between this current and the current leaving node x (via M_{i6} and M_{i8}) discharges a parasitic local capacitance. Hence, the voltage of node x decreases to boost the current of M_P thereby minimizing the variation of V_{out}.

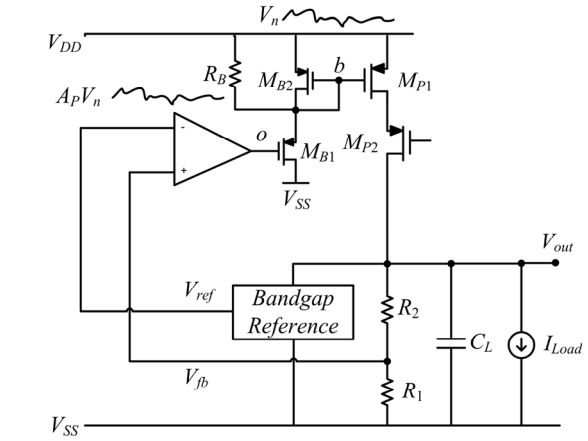
Unfortunately in Fig. 2a, even if M_{i4} completely switches off to account for a considerable decrease in V_{out}, the slew-rate of the voltage of node x would be limited to a certain value. Indeed, independent of V_{out} the current flow from M_{i6} is constant and imposes a limiting factor. This is not an issue when I_{Load} instantly reduces, as V_{out} and eventually the source voltage of M_{i4} increase to boost the input current into node x. Consequently, the voltage of this node pulls up to quickly decrease the current flow from M_P. Hence, the regulated V_{out} experiences a small variation.

Overall, Fig. 2a has a quick reaction to transient changes leading to an increase in V_{out} and a slow reaction to those leading to a reduction of V_{out} (this is obvious from the measurement data of [5]). Now, consider the architecture shown in Fig. 2b. In this circuit, the two compensation capacitors dynamically adjust the source voltages of M_{i4} and M_{i6}. Thus when V_{out} momentarily deviates from the desired value, one of these devices decreases its current whereas the other one increases correspondingly. Hence, irrespective of the direction of the change, node x dynamically responds, restoring the balance in the circuit again.

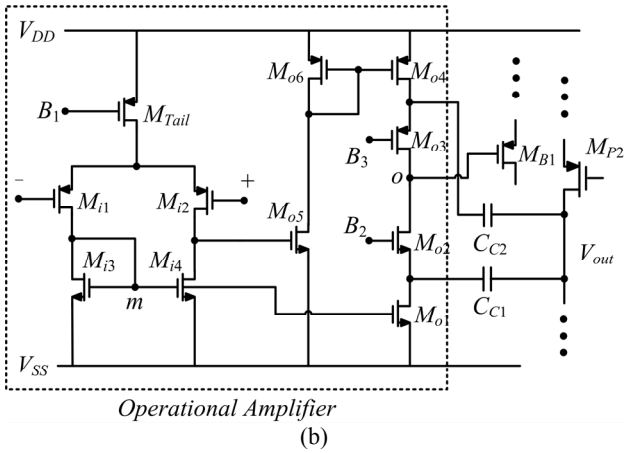
There is a serious issue to implement the circuits depicted in Fig. 2. For very small load currents, the voltage of node x must be close to V_{DD} in order to minimize the current of M_P. Employing three stacked transistors from node x up to V_{DD} requires the operating points of all these devices to be either cut-off or deep triode. For small load current, this seriously degrades the track bandwidth. It is therefore essential to revise the circuit in such a way that, in addition to exploiting the advantages of hybrid-cascode compensation, implementation is practically possible.

III. THE PROPOSED CIRCUIT AND SIMULATION RESULTS

Fig. 4 shows the proposed practical circuit architecture. As it is seen in Fig. 4a, two pass transistors (M_{P1} and M_{P2}) are used instead of one. This is done to provide more isolation between V_{DD} and V_{out}. Equivalently, this increases the output impedance and consequently the gain of the regulation loop. As a result, the overall sensitivity of V_{out} to V_{DD} will be reduced and *PSR* improves. To further improve *PSR*, the noise of the power supply is also injected into node b.



(a)



(b)

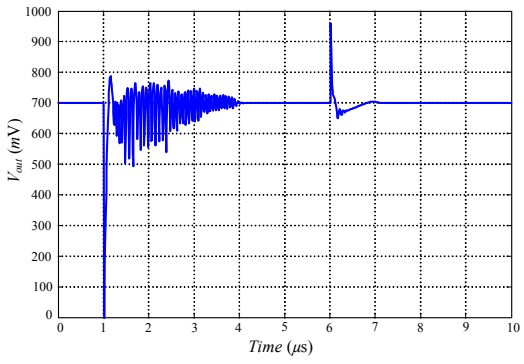
Figure 4. The proposed architecture
(a) techniques adopted to improve *PSR*
(b) error amplifier and hybrid-cascode compensation

Therefore, V_{SG} of M_{P1} and consequently its current is not affected by the corresponding noise. As it is also seen in Fig. 4a, to maintain an acceptable *PSR*, the bandgap reference of the circuit is also supplied from the regulated V_{out}. The topology of this reference is from [7]. Fig. 4b illustrates the compensation network of the architecture along with an error amplifier. It was pointed out earlier that the circuit of Fig. 2 suffers from reduced track bandwidth when the load current becomes small. This issue has been solved by using a voltage buffer comprising M_{B1}, M_{B2} and R_B. Suppose that I_{Load} is very small. The voltage of node *b* in Fig. 4a would therefore be close to V_{DD} and M_{B2} is cut-off. Under these circumstances, R_B can provide a minimum bias current to resume operation of the buffer. As the DC voltage of node *o* is one V_{GS} lower than the voltage of node *b*, devices M_{o3} and M_{o4} also have a minimum headroom to remain saturated. When I_{Load} increases, the voltage of node *o* reduces to switch on M_{B2}. Hence, the impedance of node *b* up to V_{DD} decreases from R_B to keep the gain from power supply to this node (A_P) close to unity. Circuit-level implementation of the error amplifier, as illustrated in Fig. 4b, is a push-pull network. This helps to increase the circuit speed and DC gain for the same power.

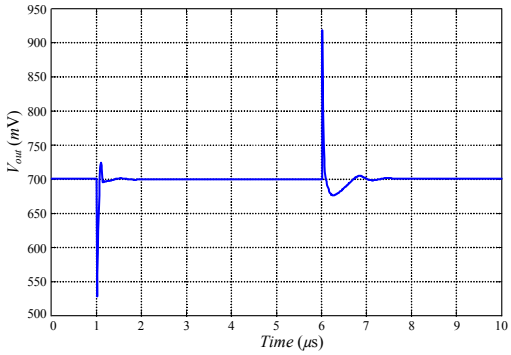
To demonstrate the efficiency of the proposed compensation technique, a regulator with 1V minimum line voltage, 0.7V output voltage, and 10mA maximum load current is simulated in 90nm CMOS technology. Fig. 5 depicts the transient load regulation for a load step of 0mA to 10mA. This Figure compares cascode compensation with hybrid-cascode compensation for equal chip area as the total compensation capacitance for both circuits is 100pF. However, hybrid-cascode compensation splits this capacitor into two. As it is seen, hybrid-cascode compensation shows a better response. Table I compares the two approaches in more detail. 0.1% positive and negative load regulation settling times decrease from 3.35µs and 1.31µs to 0.45µs and 1.16µs respectively when employing hybrid-cascode compensation.

I. CONCLUSIONS

In this paper, a modified compensation strategy namely hybrid-cascode compensation is employed to stabilize the regulation loop of a low-dropout regulator. As shown, the strategy has advantages in terms of power, area, and track bandwidth.



(a)



(b)

Figure 5. Transient load regulation vs. compensation type
(a) cascode compensation
(b) hybrid-cascode compensation

TABLE I. IMPROVEMENT WITH HYBRID-CASCODE COMPENSATION

Technology		90nm CMOS Process
Maximum Load Current		10mA
Output Value		700mV
***PSR* @ 1MHz**		-70.25dB
Load Capacitance		50pF
Average Quiescent Current		190µA
Transient Settling Time	Cascode Compensation	
	Load 0.1% error (0mA –10mA)	(V_{DD} = 1.0V) 3.35µs + 1.31µs -
	Line 0.1% error (0mA)	(V_{DD} = 1.0-1.3V) 2.00µs + 3.34µs -
	Hybrid-Cascode Compensation	
	Load 0.1% error (0mA –10mA)	(V_{DD} = 1.0V) 0.45µs + 1.16µs -
	Line 0.1% error (0mA)	(V_{DD} = 1.0-1.3V) 1.25µs + 2.25µs -

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