A Design Methodology for Low-Power Active Analog Filters for Wireless Communications

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***Abstract* — A design methodology for low-power analog filters is reported. In order to reduce the power consumption, power optimization is included at three different levels of the filter design flow. First, an appropriate transfer function is selected fulfilling the required input-output relation specifications. Then, an orthonormal ladder filter structure is chosen as it offers the best filter topology choice. Finally, a low-power circuit implementation of the transconductor cell, the main building block in g_m-C filters, is devised. The design procedure is illustrated by the design of a baseband filter required in a wireless receiver for WLAN (IEEE 802.11g standard).**

I. INTRODUCTION

Filtering blocks are indispensable elements in many signal processing systems. Filters can be used either for *selecting* the desired signal based on its different energy-frequency spectrum or for *shaping* the energy-frequency spectrum of the required signal. However, two main drawbacks appear when considering active filters. First, active elements introduce noise and distortion, leading to a limited dynamic range in filters. Second, active elements dissipate energy and thus, power has to be supplied to the circuit [1].

Achieving lower energy consumption is the key to the success of portable battery-operated equipment. If the power consumption can be reduced, battery life can proportionately be increased. Therefore, the dynamic range should be maximized and, at the same time, the power consumption of the filter should be minimized [2]. This optimization can take place at different levels of the filter design trajectory and involves:

- Transfer function synthesis,
- Topology choice, and
- Circuit implementation.

In this work, to illustrate the entire filter design procedure, a low-pass filter required in a wireless receiver for WLAN (IEEE 802.11g standard) is designed. First, the selection of the most adequate transfer function is justified, leading to a 4^{th}-order low-pass elliptic filter. Then, an orthonormal implementation is presented as the best choice for the filter topology with respect to dynamic range and related parameters. Finally, in the filter circuit design phase, the filter topology is mapped on a circuit. This includes the implementation of the integrators, the interconnection circuitry and their biasing subcircuits in a suitable IC technology. Falling in the category of g_m-C integrators, a novel CMOS transconductor for low-power g_m-C filters will be introduced. The resulting design targets 90 nm IBM CMOS process with 1.2 V power supply. Simulations demonstrate an excellent approximation of the baseband filter transfer function and, as a consequence, the design methodology presented is well suited for the design of low-power active analog filters.

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II. FILTER DESIGN METHODOLOGY

The power optimization required in analog filters can be done at different levels of the design process. In this section, the methodology towards the optimized filter design and implementation will be shown.

A. Transfer function design phase

In the filter transfer function design phase, the goal is to generate a transfer function that satisfies all the desired specifications (magnitude/phase response, group delay, cutoff frequency, passband/stopband loss/edges, distortion, etc). In this case, the requirements of the filter are determined by the targeted IEEE 802.11g WLAN standard.

Trade-offs between attenuation, slope and circuit complexity are taken into consideration prior to choosing the order of the low-pass filter. An elliptic filter gives the steepest slope for any given order and is therefore the appropriate choice compared to other possibilities as Chebyshev, Cauer, Butterworth, etc. On the other hand, power consumption and dynamic range are directly and inversely proportional to the order of the filter, respectively. Therefore, the joint optimization of power consumption and dynamic range means trying to find a low-order approximation of the transfer function.

As a consequence, to accomplish all the requirements associated with the IEEE 802.11g WLAN standard, a 4th-order elliptic low-pass filter has been selected as the core of this work. The resulting transfer function is depicted in Eq. (1), and was generated using Matlab. The cut-off frequency is set at 10 MHz. The stop-band attenuation is at least 50 dB and the pass-band ripple is less than 0.5 dB.

$$H(s)=\frac{0.003164\cdot s^4+1.937\cdot 10^{-7}\cdot s^3+3.882\cdot 10^{14}\cdot s^2+1.376\cdot 10^{9}\cdot s+6.35\cdot 10^{30}}{s^4+7.455\cdot 10^{7}\cdot s^3+6.859\cdot 10^{15}\cdot s^2+2.631\cdot 10^{23}\cdot s+6.726\cdot 10^{30}} \quad (1)$$

B. State-space synthesis: orthonormal ladder structure

Once the desired transfer function is formulated, it is time to design the topology and its state-space description. The filter transfer function is mapped on a suitable topology, where the input node, the output node and the main building blocks, viz. the integrators, of the filter are interconnected.

A state-space description for a given transfer function is not unique, meaning that many state-space descriptions can implement the same transfer function. The state-space description of any filter transfer function should be optimized for dynamic range, sensitivity, sparsity and coefficient values [3, 4]. A low sensitivity suppresses the effect of component variations on the transfer function and the sparsity of the matrices directly determines the circuit complexity – state-space descriptions with more zero elements require less hardware and are likely to consume lower power. Moreover, if the filter is optimized for dynamic range, it is also optimized for sensitivity [5]. Therefore, we will concentrate on finding a filter topology that is optimized for both dynamic range and power consumption.

In the determination of the dynamic range, the controllability (K) and observability (W) gramians of the filter, which are derived from the state space description, play an important role. To maximize the dynamic range of the system, the objective functional F_{DR}, which represents the relative improvement of the DR and contains all parameters which are subject to manipulation by the designer, should be minimized. The dynamic range is optimized when the output swing without distortion is maximized and the overall noise contribution is minimized. The first step (maximum output swing) leads to a diagonal matrix for the K-gramian with equal diagonal entries. In the second step (optimization with respect to noise contribution), the W-gramian also becomes a diagonal matrix [4].

The drawback of a dynamic-range optimal system is that its state-space matrices are generally fully dense, i.e., all entries are filled with nonzero elements, resulting in a complex circuit with a large number of interconnections. Among the standard state-space descriptions, such as the canonical, the diagonal and the modal, the orthonormal ladder form is notable since it is by definition semi-optimized for dynamic range due to the specific structure of the matrices. Furthermore, since it is derived from a ladder structure, it is intrinsically less sensitive [6]. Thus, to improve the sparsity, the dynamic range optimized matrices can be transformed into an orthonormal ladder filter description, which is significantly sparser than the fully dense matrix of the DR optimal system and still presents a good behavior with respect to sensitivity.

In respect to a fully optimized and fully dense state-space description, the resulting semi-optimal orthonormal filter structure differs only by about 2 dB in dynamic range. The matrices A, B, C and D of the selected transfer function are defined as follows:

$$A=1.0\cdot 10^{7}\cdot\begin{bmatrix} 0 & 4.4945 & 0 & 0 \\ -4.4945 & 0 & 3.8854 & 0 \\ 0 & -3.8854 & 0 & 5.7703 \\ 0 & 0 & -5.7703 & -7.4553 \end{bmatrix} \quad (2)$$

$$B=1.0\cdot 10^{3}\cdot\begin{bmatrix} 0 \\ 0 \\ 0 \\ 4.8714 \end{bmatrix} \quad (3)$$

$$C=1.0\cdot 10^{4}\cdot\begin{bmatrix} 1.1384 & 0 & 0.1304 & -0.0048 \end{bmatrix} \quad (4)$$

$$D=0.003164 \quad (5)$$

C. Noise Scaling: Capacitance and Coefficient Values

The drawback of this orthonormal structure is that the system is not optimized with respect to noise contribution. However, a filter topology can be obtained that is not too complex and has a dynamic range close (within a few dBs) to the optimal (minimum F_{DR}) if an optimal capacitance distribution is applied to this system (since the relative noise contribution of an integrator decreases when the capacitance and the bias current increase).

Transconductor-capacitance integrators will form the basic building blocks to implement the state-space description of the filter. The integrators are implemented with normalized capacitors of 1 F. The corresponding matrices A, B, C and D have extremely large coefficients corresponding to large g_m values, which are not physically feasible at circuit level. By scaling down the capacitors, matrices A and C are consequently scaled. Coefficients of matrices B and D can too be down scaled by α_1 and α_2 respectively, without affecting the response of the filter.

$$A^*=cap\cdot A \quad (6)$$

$$B^*=\alpha_1\cdot B \quad (7)$$

$$C^*=\alpha_2\cdot cap\cdot C \quad (8)$$

$$D^*=\alpha_1\cdot\alpha_2\cdot D \quad (9)$$

After applying the adequate noise scaling, the optimal capacitance distribution is:

$$cap=[C_1, C_2, C_3, C_4]=C'\cdot[0.2242, 0.2849, 0.2735, 0.2173] \quad (10)$$

where C' represents the unit-less value of the total capacitance. The block diagram of the state-space filter is shown in Fig. 1 and has 12 non-zero coefficients (c_2=0 as can be seen from Eq. (4)).

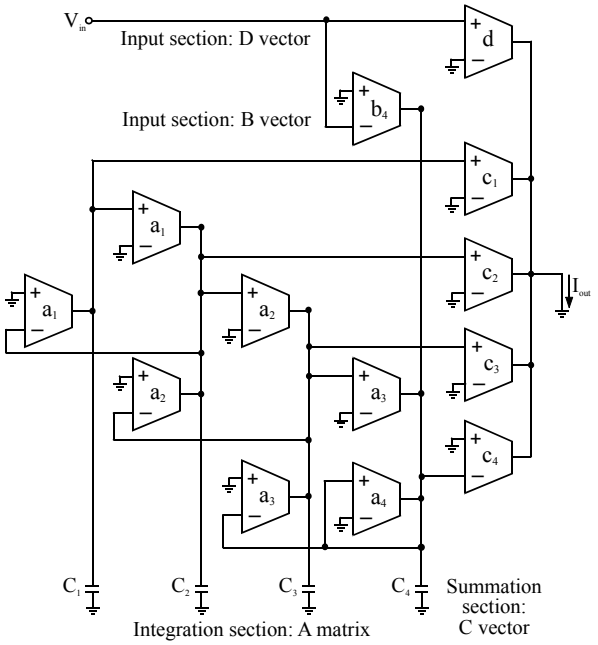

Figure 1. Complete State-Space filter structure.

Once the block diagram has been recognized, a specific transconductance block implements every coefficient.

III. Main Active Block: Transconductor Topology

Once the optimal filter topology has been selected together with the appropriate coefficients, the filter circuit, or more specifically, the integrator as the main building block of the filter has to be designed. Since the g_m-C technique is the considered option to implement the filter, a specific transconductor has to be designed with the aim of achieving the minimum power consumption [7].

The orthonormal structure has both positive as well as negative coefficients. In order to implement positive coefficients, a differential topology is used. Another advantage of using the latter is the cancellation of even order distortion terms that may arise from the actual nullor implementation, thus improving linearity.

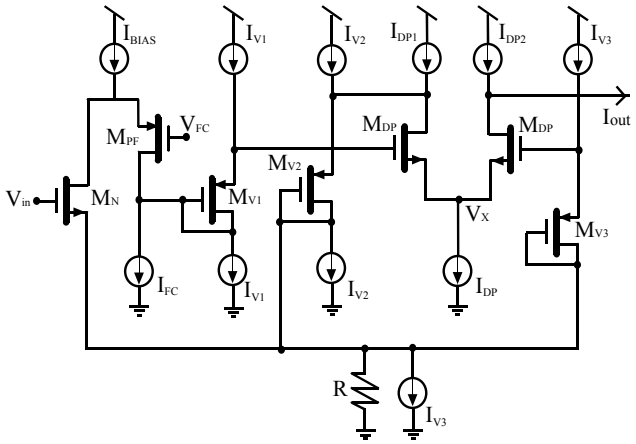

Figure 2. Negative feedback transconductor.

As compared to a single-stage implementation, a 2-stage nullor improves the loop gain, which yields higher linearity as well as bandwidth at the expense of power consumption [8].

The transconductance amplifier is implemented using a negative feedback structure consisting of an active circuit, which implements a nullor and a passive feedback network. The nullor is realized using a folded-cascode stage formed by transistors (M_N-M_{PF}) at the input, and a non-inverting differential pair (M_{DP}) at the output. The feedback network is made up of a resistor R (Fig. 2).

Special care has been taken in the biasing of the transconductor cell. Stages M_{V1}, M_{V2} and M_{V3} generate the adequate bias voltages by implementing floating voltage sources. Input stage bias current I_{BIAS} is implemented with a simple current mirror and both the biasing of the differential pair (I_{DP1}, I_{DP2}) and the current source of the folded-cascode transistor M_{PF} (I_{FC}) have been implemented with cascode current mirrors.

Current source I_{DP}, however, requires special attention. The low supply voltage (1.2 V) and the requirement of a cascode mirror in the upper current sources of the differential pair make this node especially critical. Therefore, an ultra high-compliance CMOS current mirror for low-voltage requirements is needed. Its implementation is shown in Fig. 3 [9]. The drains of transistors M_1 and M_2 of the cascode mirror are held at the same voltage by means of a feedback loop. The implementation includes a low-power differential input servo amplifier, taking the input device as the reference. Transistors M_1 and M_2 are operating in the triode region.

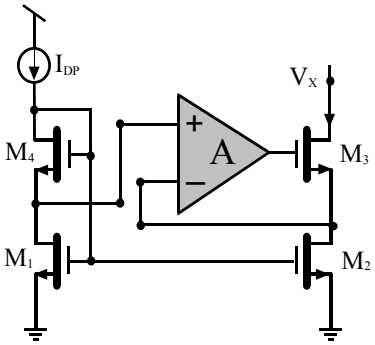

Figure 3. High compliance regulated cascode current mirror [9].

IV. Simulation Results

The 4th-order low-pass elliptic filter has been designed to be implemented in IBM 90 nm CMOS IC technology with a 1.2 V power supply and a nominal biasing current (I_{BIAS}+I_{DP}) of 250 μA per transconductor (600 μA including additional biasing circuits).

The high-frequency response of the entire filter is preserved, as shown in Fig. 4, considering a total external capacitance of 10 pF.

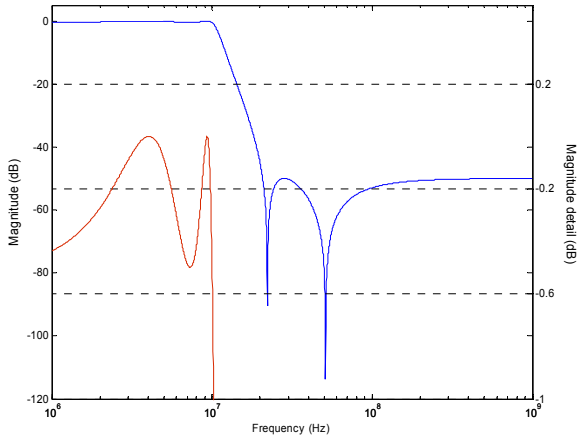

Figure 4. Transfer function of the 4th-order low-pass elliptic filter.

Finally, by randomly varying (i.e., 100 iterations) the component tolerances as well as the model parameters between their specified tolerance limits, a Monte Carlo analysis is run in order to estimate the sensitivity of the circuit. From Figs. 5 and 6, it is inferred that the transfer of the filter is relatively unlikely to show a substantial discrepancy as a result of process variations. The average value of the dc-gain is -0.4381 dB and for the cutoff frequency, a value of 10.69 MHz is obtained.

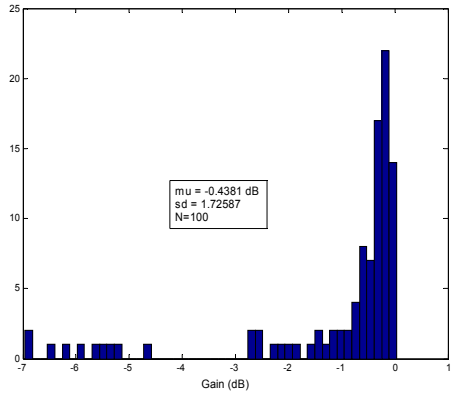

Figure 5. Sensitivity analysis – Monte Carlo: filter dc-gain.

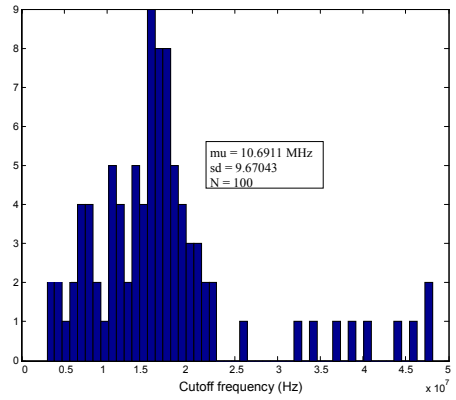

Figure 6. Sensitivity analysis – Monte Carlo: cutoff frequency.

Table I highlights the most important simulation parameters of the 4th-order elliptic low-pass filter.

TABLE I. SIMULATION RESULTS FOR THE FILTER

IC technology	IBM 90 nm CMOS
Power supply voltage	1.2 V
Cut-off frequency (-3dB)	10 MHz
Stop-band attenuation	50 dB
Pass-band ripple	< 0.5 dB
Power dissipation/pole	1.53 mW
Differential output noise	400 nV/√Hz
Max. output signal (1% THD)	750 mV
Dynamic range (1% THD)	52 dB

V. CONCLUSIONS

In this work, a filter design procedure is proposed, which deals with the reduction of energy consumption of the analog filtering block, being the main goal in the design of circuits for portable battery-operated equipment. This power optimization is considered at three different levels of the design flow and concerns: the filter transfer function synthesis, the choice of the best filter topology and low-power circuit design. In order to demonstrate the feasibility of the proposed technique, a low-pass filter required in a wireless receiver for WLAN (IEEE 802.11g standard) is designed, to be implemented in 90 nm IBM CMOS technology with a 1.2-V power supply. Simulations demonstrate an excellent approximation of the baseband filter transfer function and, as a consequence, the design methodology presented is well suited for the design of low-power active analog filters.

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