Multichannel current-mode stimulator with channel-specific regulated power supply

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***Abstract*—Developing neuroprosthetic bioelectronic devices requires wirelessly-powered implantable stimulator systems with hundreds to thousands of output channels. Power efficiency optimization is crucial for scaling up the number of output channels. Current-mode electrical stimulation is favored for safety but is power-inefficient in conventional designs, particularly in multichannel stimulators. An adaptive voltage supply can improve power efficiency, but implementing channel-specific voltage supplies in large-scale systems is challenging. Conventional power management suffers from losses and low efficiency due to multiple conversion stages. This work proposes a multichannel current-mode stimulator with a parallel, adaptive ac/dc power management strategy using single-stage phase-controlled converters to prevent cascaded losses. This allows for generating channel-specific supply voltages within a small area for high power efficiency and high-density electrical stimulation. The proposed circuit was designed and simulated using TSMC 180 nm technology and demonstrates an improvement in the power efficiency of up to 45% with respect to a conventional power-management strategy using a fixed supply voltage.**

***Index Terms*—electrical stimulation, neuromodulation, regulating rectifier**

I. Introduction

Bidirectional brain-computer interfaces and implantable cortical visual prostheses are promising brain-stimulation applications that demand large-scale multichannel stimulator systems. For example, it is estimated that hundreds to thousands of stimulation channels are needed in a cortical visual prosthesis to provide useful vision to a blind patient [1]. Such implantable devices should be powered through a wireless link to avoid infections that wired solutions would otherwise cause. However, the amount of power that can be transferred is limited due to safety regulations. This poses a challenge to the demand for increasing the number of stimulation channels.

Current-Mode Stimulation (CMS) is often the preferred method for stimulation, as it offers better control over the amount of charge delivered to the neural tissue, an essential requirement to ensure the patient's safety [2]. In this method, pulse trains of biphasic current pulses are applied to the tissue to activate nearby neurons. To apply the pulses to the tissue, a bipolar electrode configuration can be used. This configuration uses a unidirectional current source combined with a switch structure (H-bridge) that reverses the current direction to achieve biphasic pulses, as shown in Fig. 1a.

In CMS, each channel has a different electrode-tissue-interface impedance [3] and different current requirements for activating neurons, which leads to different voltage drops over the tissue. This, in turn, leads to different requirements for the ideal power supply voltage in each channel. As illustrated in Fig. 1b, a mismatch between the voltage drop over the tissue and the voltage supply results in an excessive voltage drop over the current source, which leads to power losses. Traditionally, the voltage supply has to accommodate the channel with the highest tissue-voltage requirements, which leads to power losses in all other channels. A scalable voltage supply can reduce overhead losses and increase power efficiency (Fig. 1b) [4]–[9]. Some designs use a feedback loop that includes the external wireless power transmitter to regulate the output voltage by the transmitted power signal [4]. This implementation would require multiple power links to support multi-output voltage regulation, which is not a scalable solution. Alternatively, on-chip DC/DC converters are used [5]–[8], which typically use bulky capacitors or inductors, limiting the scalability. A possible solution is to implement a multi-output DC/DC converter and utilize it for multiple channels [9], [10]. However, another disadvantage of on-chip DC/DC converters is the cascaded inefficiencies in the multiple stages of rectification and regulation of the incoming signal. To overcome this problem, single-stage regulating rectifiers can be used [11]–[13]. A limitation of existing single-stage regulating rectifier implementations is that the output voltage is regulated according to a programmed reference voltage. In order to explore the high energy efficiency of single-stage regulating rectifiers while automatically adapting to the unpredictability of the electrode-tissue interface load conditions, this work proposes a new feedback regulation topology with a compliance monitor based on a phased-controlled regulating rectifier. This allows the current-mode stimulator to have a power supply matched to the needs of the load, hence maximizing the

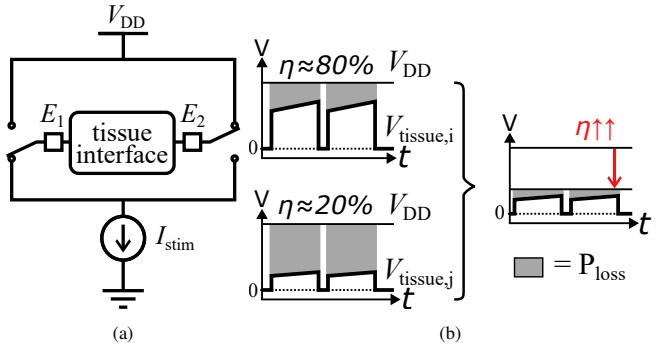

Fig. 1: (a) Bipolar electrode configuration, using unidirectional current source and H-bridge to create biphasic current pulses through the tissue. (b) Losses in conventional CMS output driver for different V_{tissue} properties (left) and possible efficiency improvement by scaling of the voltage supply (right)

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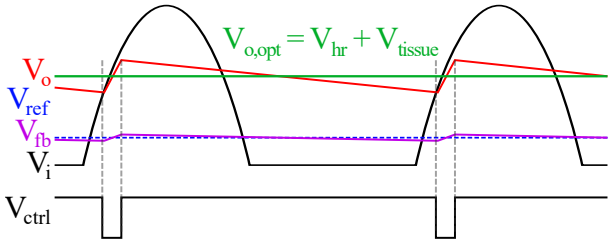

Fig. 2: Timing diagram of the proposed regulating rectifier circuit

power efficiency. Furthermore, the proposed design aims to achieve scalability for high-channel-count systems, allowing for efficient and precise regulation of the output voltage in each module.

II. Circuit Design

A. System-level design and requirements

In a wirelessly powered implant, the input signal to the system is often an alternating voltage generated by the power-receiving elements. For each channel, to minimize the voltage overhead on the current source and hence optimize the power efficiency, a channel-specific power supply is needed. As illustrated in Fig. 2, the alternating input signal crosses the optimal output voltage, $V_{o,opt}$, in each period. Our proposed idea is to design a regulating rectifier that charges a storage capacitor whenever the input signal crosses the optimal output supply voltage.

The proposed modular multichannel stimulator architecture is shown in Fig. 3a. Each module contains a current mode stimulator with an individually regulated voltage supply. The proposed regulating rectifier topology consists of a rectifying PMOS transistor, M_P, a phase-controlling feedback loop, and a storage capacitor, C_o. The phase controller is enabled when the current source is active. When the phase controller is active, it controls the conduction time of M_p to regulate the headroom voltage of the current source, V_{fb}, to a set reference, V_{ref}. As a result, V_o is regulated to the appropriate voltage required to deliver the current to the load.

The timing diagram of the circuit is shown in Fig. 2. Because the rectifiers are designed to operate in parallel in multiple modules, each rectifier only receives a half-wave rectified voltage at the input. This omits copies of the control circuits to rectify the other half of the input signal, reducing the circuit's size. To extract power from the complete input signal, it will be equally divided over the available modules. The output power of each rectifier is low since it only supplies one current driver. Therefore, C_o is small compared to a rectifier that needs to supply full-system loads.

The proposed implementation of the phase controller is illustrated in Fig. 3b; The comparator decides the turn-on time by comparing the input voltage, V_i, and the output voltage, V_o, and the duration of the pulse is controlled using a voltage-controlled delay line (VCDL). The control voltage for the VCDL, V_b, is produced by the error amplifier, which has a frequency compensation network adding two poles and one zero to its transfer function to boost the phase margin of the feedback loop. When the phase controller is disabled, the output multiplexer configures M_P as a diode-connected

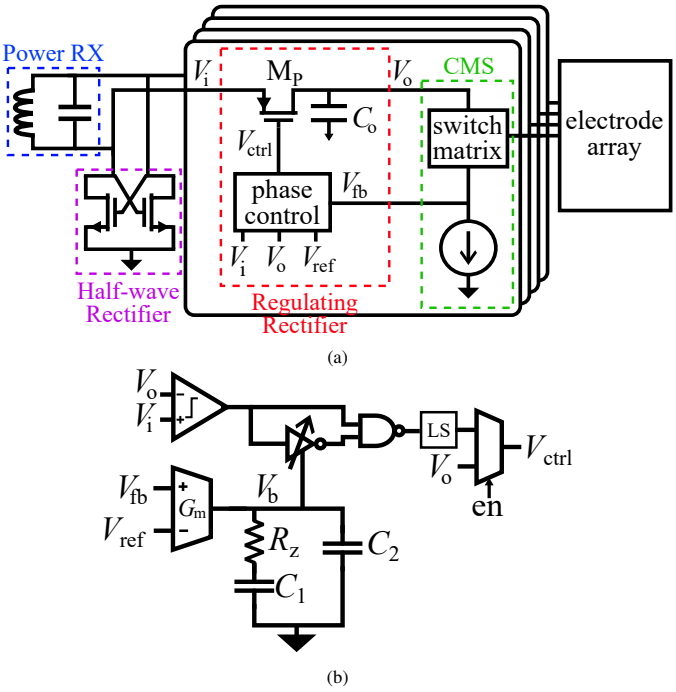

Fig. 3: (a) Proposed system architecture. Each module connects to a half-wave rectified input voltage. (b) Proposed implementation of the phase control feedback circuit.

transistor by connecting its gate to V_o, and the circuit operates as a passive rectifier.

The circuit is designed for the application of an intracortical visual prosthesis. In this application, a supply voltage of a few volts can be expected [14], [15]. Therefore, the circuit is designed to operate with an input signal with a peak voltage of 5 V. Only at the output, this voltage is required. The rest of the system operates from a 1.8 V supply to reduce power consumption. Because of this, a level shifter (LS) is needed between the control circuit and M_P. The electrode impedance is in the order of 50 kΩ while threshold currents between 30μA and 100μA can be expected [14]. In order to support the clinically relevant range, the output current source can be configured between 20 μA and 95 μA with 4 bits (LSB = 5 μA) resolution. The circuit is designed to operate from a 13.56 MHz input signal, a carrier frequency in the ISM band commonly used for powering biomedical implants. In the presented design, the saturation voltage of the current source is approximately 200 mV. The presented results are simulated with a reference voltage of 250 mV to ensure that the current source is operating in saturation region in steady-state. This work focuses on the implementation of the phase controller and current source. Additional global and local control and power management blocks are needed to complete the system but are left out of Fig. 3a to focus on the scope of this work.

B. Transistor-level design

The output voltage of the driver stage does not have strict voltage-ripple requirements as the current source controls the current through the tissue. This relaxes the size of the filter capacitor C_o. Changes in the output voltage V_o will reflect to some degree in the produced output current, depending on the output impedance of the current source, which can

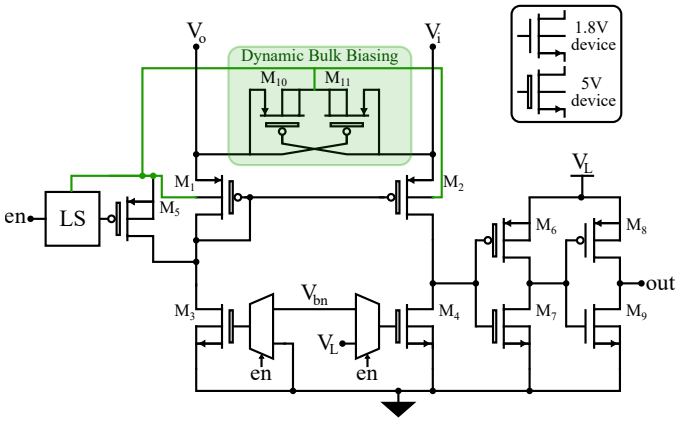

Fig. 4: Circuit implementation of the comparator. V_{bn} is the bias voltage for M_3 & M_4 when the comparator is enabled.

lead to unbalanced current pulses. However, even perfectly matched current pulses can lead to residual charges on the electrode-tissue interface [2]; thus, charge-balancing circuits will be required to ensure the device's long-term safety. As mentioned in Section I, the required output voltage, depending on the current amplitude and the (unknown) electrode-tissue impedance, is unpredictable and varies for each channel and over time. Therefore, the proposed circuit regulates the voltage over the current source instead and produces an output voltage accordingly. Furthermore, using the voltage on the current driver as the input voltage of the control circuit omits the necessity of a voltage divider used by other designs that use V_o as an input [11], [12], which saves energy and area.

The comparator is implemented using a common-gate input pair, as depicted in Fig. 4. This omits the requirement of a steady HV supply for the correct circuit operation. A dynamic bulk biasing circuit, consisting of 2 PMOS devices, ensures correct biasing of the input devices to the highest input voltage. It also acts as the voltage supply for the level shifter and M_5, which turns off M_1 and M_2 when the comparator is disabled, by pulling up their gate voltages. Furthermore, two multiplexers are used at the gates of M_3 and M_4, controlled by the enable signal, '*en*'. When the comparator is enabled, the gates are connected to a bias voltage, V_{bn}, and when the comparator is disabled, the gate voltages prevent any static current.

The voltage-controlled delay line is implemented using a current-starved inverter, shown in Fig. 5. The bias voltage V_b limits the maximum current of the input inverter through the current mirror. The inverter consisting of M_7 and M_8 is sized to have a considerable input capacitance. By limiting the inverter's current, the discharge time of this gate capacitance is controlled. The charge time of the capacitor is not limited as this is not relevant for the correct operation of the phase controller.

III. Results

The proposed circuit is implemented in a 180 nm CMOS TSMC process to validate the voltage-regulating operation. The implemented circuit consists of two identical channels, each receiving half of the AC input signal and producing an individually regulated output voltage. The layout of the

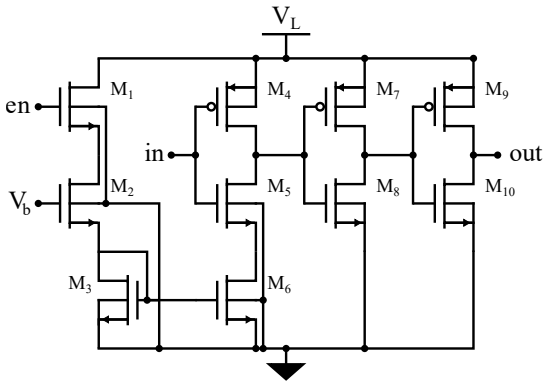

Fig. 5: Circuit implementation of the voltage-controlled delay line.

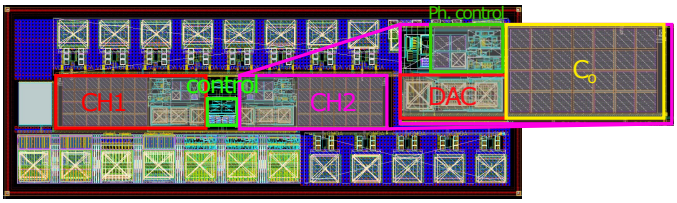

Fig. 6: Layout of the designed system with two channels

circuit is depicted in Fig. 6. The design has a channel area of 320 μm $\times$ 110 μm, of which the output capacitor occupies 62%. Fig. 7 shows the start-up process, with the regulators configured as passive rectifiers. Due to the voltage drop over the diode-connected PMOS, the maximum output voltage in passive mode is approximately 4.2 V. Fig. 8 shows the output voltages and currents for a 50 μA, 100 μs current pulse on both channels, while the load impedance of Channels 1 and 2 are 30 kΩ and 50 kΩ, respectively. It can be seen that V_{fb} of both channels is regulated to the set reference voltage, while the output voltage for both channels is different due to the difference in load impedance. The spikes observed at the output current are due to the switching and resulting ripple on V_o and V_{fb}. The regulation speed depends on the output current, discharging the storage capacitor, but both channels settle within 6 μs after the onset of the pulse to their regulated output level.

The efficiency of the regulator is calculated for both the schematic design and post-layout simulations by averaging the in- and output power of a 20 μs current pulse for a range of current amplitudes and load impedances. The resulting efficiencies are depicted in Fig. 9a. The output current range is limited for higher impedances due to the maximum output

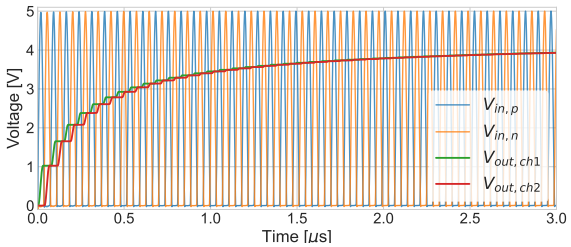

Fig. 7: Post-layout simulated start-up sequence with diode-connected rectifying switches.

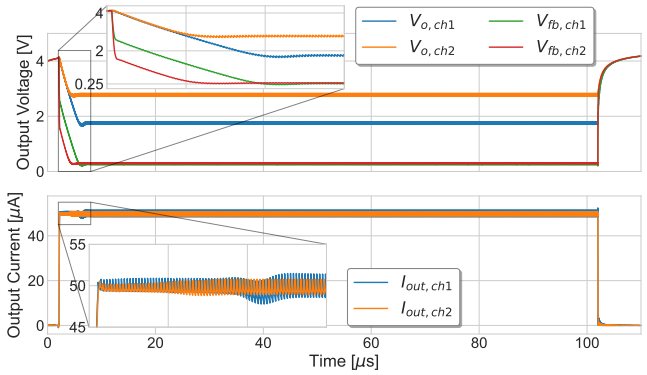

Fig. 8: Post-layout simulated output signals for a 100μs (starting at t=2μs) current pulse of 50μA and $R_{load,1}$=30kΩ, $R_{load,2}$=50kΩ

voltage the circuit can produce. The reported efficiencies do not account for the additional power dissipation in the OTA and digital blocks of the phase controller: the OTA has a static power dissipation of 1.8 μW, while the VCDL and other logic only have dynamic switching losses. The 5 μA bias current of the comparator is drawn from V_i and V_o due to the common-gate structure. Therefore, its power consumption is already considered in the presented efficiency values.

To compare the current design with a conventional power management strategy, we calculated the power efficiency of a system with a fixed output voltage of 5 V using (1). Note that this calculation assumes an ideal regulator without any losses. The efficiency improvement of the proposed circuit is calculated with (2), and the results are shown in Fig. 9b.

$$\eta_{fixed} = \frac{I_{stim}^2 R_{load}}{V_{supply} I_{stim}} \cdot 100\% \quad (1)$$

$$\text{Efficiency improvement} = \frac{\eta_{proposed} - \eta_{fixed}}{\eta_{fixed}} \cdot 100\% \quad (2)$$

IV. Discussion

The presented design shows an improvement of the power efficiency by up to 45% for low-impedance channels compared to a fixed supply voltage in post-layout simulations. Several opportunities exist to improve it even further:

- The phase controller has no compensation for the on- or off-timing of the pulse. A delay at the onset of the pulse leads to a voltage difference over M_p, causing conduction losses. Furthermore, when the required output voltage is near $V_{i,peak}$, off-switching delays also cause degradation in the power efficiency due to reverse currents [16], [17]. Several offset-compensation techniques exist to account for the delays of the phase controller, which would result in improved efficiency [17]–[23].
- In the current design, the phase controller triggers during each period of the input signal. When the output current is small, the conduction pulses become short, which degrades the power efficiency as switching losses are high compared to the energy transferred to C_o. To improve the efficiency for low currents, additional pulse-frequency modulation (PFM) could be applied [12]. The PFM regulates how often the phase controller is triggered; this increases the pulse duration and hence improves the power efficiency.
- The reference voltage determines the power consumption of the current source. For the presented results, the reference voltage was 250 mV. Improving the current source design to require less voltage headroom for a well-defined output current would allow to decrease V_{ref}.

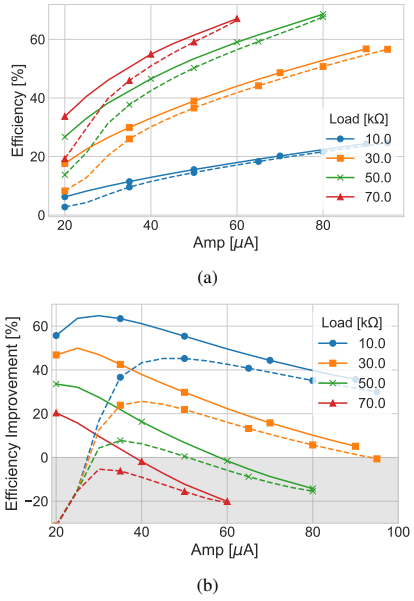

Fig. 9: (a) Simulated schematic (solid) and post-layout (dashed) efficiency of the proposed circuit as a function of output current for 4 load impedances, (b) Efficiency improvement of the proposed circuit with respect to a fixed 5V-voltage supply

As seen in Fig. 9, the post-layout simulations' efficiency is lower than that of schematic simulations, particularly for low-current outputs. This is mainly due to increased delay of the phase controller caused by parasitic capacitances. Furthermore, the minimum pulse width that the phase controller can produce is also affected by parasitic capacitances, which limits the regulating capability of the circuit for low currents. Next to the possible improvements listed above, careful redesign of the critical nodes in the phase controller could improve the post-layout results.

V. Conclusion

Power efficiency plays an important role in developing large-scale multichannel stimulator systems. Each channel should have an individually regulated supply voltage for optimal efficiency. This work presented a regulating rectifier topology specifically designed for output stages of current-mode stimulator systems. Designed to supply low-power outputs of single-channel stimulators and operate in parallel in a multichannel system, the proposed design enables channel-specific voltage regulation with a scalable design. The current design improves the power efficiency by up to 45% with respect to that of conventional output drivers with a fixed voltage supply, and several improvements are proposed to increase the power efficiency further.

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