Ultra Low-Power Low-Voltage Analog Integrated Filter Design

Wouter A. Serdijn Sandro A.P. Haddad and Jader A. De Lima

Abstract

Filtering is an indispensable elementary signal processing function in many electronic systems. In many critical applications, e.g., in portable, wearable, implantable and injectable devices, one should maximize the dynamic range and, at the same time, minimize the power consumption of the filter. This joint optimization can take place in different phases, the filter transfer function design phase, the filter topology design phase, and the filter circuit design phase.

In the filter transfer function design phase, the filter's functional input-output relation is mapped on a suitable filter transfer function. Two approximation techniques are introduced: the Padé approximation and the L_2 approximation. The Padé approximation is employed to approximate the Laplace transform of the desired filter transfer function by a suitable rational function around a selected point. The L_2 approximation offers a more global approximation, i.e., not concentrating on one particular point, and has the advantage that it can be applied in the time domain as well as in the Laplace domain.

In the filter topology design phase, the filter transfer function is mapped on a suitable filter topology. For this, the filter transfer function is written in the form of a state-space description, which subsequently is optimized for dynamic range, sparsity and sensitivity. In the determination and optimization of the dynamic range the filter's controllability and observability gramians play an important role. Dynamic range optimization boils down to transforming the controllability gramian such that it becomes a diagonal matrix with equal diagonal entries, transforming the observability gramian such that it also becomes a diagonal matrix, and capacitance distribution. To improve the state-space matrices' sparsity the dynamic-range optimized matrices can be transformed into a form that describes an orthonormal ladder filter. After applying capacitance distribution, a filter topology is found that is not too complex and has a dynamic range that is close (i.e., within a few dBs) to optimal.

Finally, in the filter circuit design phase, the filter topology is mapped on a circuit. A classification of integrators is presented. Falling in the category of transconductance-capacitance (gm-C) integrators, a novel nA/V CMOS transconductor for ultra-low power low-frequency gm-C filters is introduced. Its input transistors are kept in the triode-region to benefit from the lowest g_m/I_D ratio. The g_m is adjusted by a well defined (W/L) and V_{DS}, the latter a replica of the tuning voltage $V_{\rm TUNE}$. The resulting design complies with V_{DD}=1.5V and a 0.35μm CMOS process. Its transconductance ranges from 1.1nA/V to 5.5nA/V for 10mV $\leq V_{\rm TUNE} \leq$ 50mV.

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To illustrate the entire filter design procedure, a dynamic translinear Morlet filter is designed. Simulations and measurements demonstrate an excellent approximation of the Morlet wavelet base. The circuit operates from a 1.2-V supply and a bias current of 1.2μA.

Index Terms

Filters, Integrators, Analog Integrated Circuits, Low Voltage, Low Power, Dynamic Translinear, Log-Domain, Gm-C, State Space Optimization, Dynamic Range, Sensitivity, Sparsity

I. Introduction

FILTERING is an indispensable elementary signal processing function in many electronic systems. Filters are either used for *selection*, i.e., to separate desired signals from other signals and noise by making use of their differences in energy-frequency spectra, or for *shaping*, i.e., to change the energy-frequency spectrum of a single, desired signal. In practice, a piece of electronic apparatus that does not contain at least one rudimentary filter can hardly be found.

Traditionally, filters operated in the continuous-time domain and have been designed as resistively terminated lossless discrete inductor-capacitor (LC) filters. When we wish to realize the filter on chip, however, often, at least for most sub-gigahertz applications, this implies giving up the use of inductors. The Laplace transform of filter transfer functions that can be realized with capacitive and resistive elements only have real poles in the left half of the complex Laplace plane, while often transfer functions with complex poles are called for. These are only realizable if active circuits are added.

With the introduction of active circuits in filters, resulting in active filters, two fundamental problems are introduced. First, unlike passive reactances, active elements produce noise and distortion. For this reason, active filters are bound to exhibit a limited dynamic range, defined as the ratio of the largest and the smallest signal level that the filter can handle. Second, unlike passive reactances, active elements dissipate energy. Thus power has to be supplied. In many critical applications, e.g., in portable, wearable, implantable and injectable devices, one should maximize the dynamic range and, at the same time, minimize the power consumption of the filter. This joint optimization can take place in different phases:

1. the filter transfer function design phase,
2. the filter topology design phase, and
3. the filter circuit design phase.

In the first phase, the *filter transfer function design phase,* the filter's functional input-output relation is mapped on a suitable filter transfer function, whose Laplace transform can be described by a strictly proper rational function of low order. For

obvious reasons only the implementation of a causal stable filter is feasible, meaning that it will have a proper rational transfer function that has all its poles in the complex left half plane and the degree of the numerator polynomial does not exceed the denominator degree.

In Section II, two approximation techniques will be introduced: the *Padé approximation* and the L_2 *approximation*. The Padé approximation is employed to approximate the Laplace transform of the desired filter transfer function by a suitable rational function around a selected point. The L_2 approximation offers a more global approximation, i.e., not concentrating on one particular point, and has the advantage that it can be applied in the time domain as well as in the Laplace domain.

In the second phase, the *filter topology design phase*, the filter transfer function is mapped on a suitable filter topology. In such a topology, the input node, the output node and the filter's main building blocks, the integrators[1], are interconnected. An equivalent method for describing the topology of the filter is the state space description, in which matrices are used to describe the connectivity of the integrators and the coupling of the input and the output. An n-th order filter can always be constructed by means of n integrators.

In Section III, the filter's state-space description will be optimized for dynamic range, sparsity and sensitivity. It will be shown that dynamic range optimization boils down to transforming the controllability gramian such that it becomes a diagonal matrix with equal diagonal entries, transforming the observability gramian such that it also becomes a diagonal matrix, and capacitance distribution. To improve the state-space matrices' sparsity the dynamic-range optimized matrices can be transformed into a form that describes an orthonormal ladder filter. After applying capacitance distribution, a filter topology is found that is not too complex and has a dynamic range that is close (i.e., within a few dBs) to optimal.

Finally, in *the filter circuit design phase*, the filter topology is mapped on a circuit. This includes the implementation of the integrators, the interconnection circuitry and their biasing subcircuits in a suitable IC technology. In Section IV, a novel nA/V CMOS transconductor for ultra-low power low-frequency gm-C filters will be introduced, employing transistors operating in strong inversion and in the triode region. Contrary to previous designs, its transconductance depends on the size of the input transistors and a control voltage only.

To illustrate the entire filter design procedure, in Section V a 10th-order dynamic translinear *Morlet* filter will be presented. Simulations and measurements will demonstrate an excellent approximation of the Morlet wavelet base. The circuit operates from a 1.2-V supply and a bias current of 1.2μA.

[1] Although there is no preference for either a differentiator or integrator from a transfer-function or topological point of view, at circuit level, the use of differentiators often gives rise to high-frequency problems or instability. Therefore, in a filter, almost always integrators are employed.

II. Designing the filter transfer function

In the filter transfer function design phase, the aim is to generate a transfer function that satisfies the desired specifications, which may concern, in the frequency domain: the amplitude (or magnitude) response, the phase response — together with the amplitude response grouped in the two so-called Bode plots —, the group delay, the cutoff frequency, the passband/stopband loss, the passband/stopband edges, the amplitude/phase/delay distortion; and in the time domain, the impulse/step responses (including the overshoot, delay time and rise time).

The available methods for generating the filter transfer function can be classified as *closed-form* or *iterative*. In closed-form methods, the transfer function is derived from a set of closed-form formulas or transformations. Some classical closed-form solutions are the so-called Butterworth, Chebyshev, Bessel-Thompson and elliptic approximations. Iterative methods entail a considerable amount of computation but can be used to design filters with arbitrary responses.

If the desired filter transfer function does not have an explicit expression, then the splines interpolation method [1] can be used to generate the desired (idealized) filter transfer function that can be used as a starting point for the filter design process.

Taking into account that in active filters the power consumption and the dynamic range are proportional and inversely proportional to the order of the filter, respectively, in this phase, the joint optimization of power consumption and dynamic range means finding a low-order approximation of the Laplace transform of the desired filter transfer function. In the sequel we will deal with two, relatively unknown, techniques to come to such an approximation: the Padé approximation and the L_2 approximation.

A. Padé approximation

The Padé approximation [2] is employed to approximate the Laplace transform of the desired filter transfer function $G(s)$ by a suitable rational function $H(s)$ and is characterized by the property that the coefficients of the Taylor series expansion of $H(s)$ around a selected point $s = s_0$ coincide with the corresponding Taylor series coefficients of $G(s)$ up to the highest possible order, given the pre-specified degrees of the numerator and denominator polynomials of $H(s)$. If we denote the Padé approximation $H(s)$ at $s = s_0$ and of order (m, n), with $m \leq n$, by

$$H(s) = \frac{p_0(s - s_0)^m + p_1(s - s_0)^{m-1} + \cdots + p_m}{(s - s_0)^n + q_1(s - s_0)^{n-1} + \cdots + q_n}, \tag{1}$$

then there are $n + m + 1$ degrees of freedom, which generically makes it possible to match exactly the first $n + m + 1$ coefficients of the Taylor series expansion of $G(s)$ around $s = s_0$. As this matching problem can easily be rewritten as a system of

$n+m+1$ linear equations in the $n+m+1$ variables $p_0, p_1, \cdots, p_m, q_1, \cdots, q_n$, a unique solution is obtained that is easy to compute. Moreover, a good match is guaranteed between the given function $G(s)$ and its approximation $H(s)$ in a neighborhood of the selected point s_0.

However, there are also some disadvantages which limit the practical applicability of this technique [3]. One important issue concerns the selection of the point s_0. Note that a good approximation of $G(s)$ around one point in the (complex) Laplace domain is not a requirement *per se*. A second important issue concerns stability, which does not automatically result from the Padé approximation technique. For example, if emphasis is put on obtaining a good fit for a particular s_0, it may easily happen that the resulting approximation becomes unstable. The trade-off between a good fit near a certain point $s = s_0$ and stability is a non-trivial problem. A third issue concerns the choice of the degrees m and n of the numerator and denominator polynomials of the rational approximation $H(s)$. An unfortunate choice may yield an inconsistent system of equations or an unstable approximation.

B. L_2 approximation

An alternative to the Padé approximation is the so-called L_2 approximation, which offers a number of advantages [3]. First, on the conceptual level, it is quite appropriate to use the L_2 norm to measure the quality of an approximation $H(s)$ to the function $G(s)$. Another advantage of L_2 approximation is that it can be applied in the time domain as well as in the Laplace domain. According to Parseval's equality, minimization of the squared L_2 norm of the difference between $G(s)$ and $H(s)$ over the imaginary axis $s = j\omega$ is equivalent to minimization of the squared L_2 norm of the difference between $g(t)$ and $h(t)$.

Particularly in the case of low order approximation, the L_2 approximation problem can be approached in a simple and straightforward way using standard numerical optimization techniques and software.

III. Designing the filter topology

After we have completed the design of the filter transfer function, it is time to design the filter topology. As there are many possible state-space descriptions for a certain transfer function, there are many possible filter topologies. We will concentrate on finding a filter topology that is optimized for both dynamic range and power consumption.

As is well known from linear systems theory (see, e.g., [4]) any causal linear filter of finite order n can be represented in the Laplace domain as a state-space system (A, B, C, D) described by a set of associated polynomial equations of the form:

$$sX(s) = AX(s) + BU(s), \tag{2}$$

$$Y(s) = CX(s) + DU(s), \tag{3}$$

where $U(s)$ denotes the scalar input to the filter, $Y(s)$ the scalar filter output and $X(s)$ the state vector. The transfer function of the filter is given by:

$$H(s) = C(sI - A)^{-1}B + D. \tag{4}$$

A system's dynamic range is essentially determined by the maximum processable signal magnitude and the internally generated noise. It is well known that the system's controllability and observability gramians play a key role in the determination and optimization of the dynamic range [5], [6]. The controllability (K) and observability (W) gramians are derived from the state space description and are computed by solving the equivalent Lyapunov equations

$$AK + KA^T + 2\pi BB^T = 0, \tag{5}$$

$$A^T W + WA + 2\pi C^T C = 0. \tag{6}$$

As the dynamic range of a circuit is defined as the ratio of the maximum and the minimum signal level that it can process, optimization of the dynamic range is equivalent to the simultaneous maximization of the (distortionless) output swing and the minimization of the overall noise contribution. In [7], Rocha gives a geometric interpretation of the optimization of the dynamic range. A visualization of the optimization procedure can be seen in Fig. 1, for a system with three state variables. The output swing is related via the controllability gramian to the space of 'occurring' state-space vectors. Under the assumption of a random input signal, the shape of this space is generally a multidimensional ellipsoid. The constraint that each integrator has a maximum representation capacity (M) defines a multidimensional cuboid, which, for a distortionless transfer, should contain the former mentioned ellipsoid completely. As the mean square radius of the ellipsoid is equivalent to the maximum output swing, the output swing is maximal when the mean square radius is. This can occur if and only if the ellipsoid becomes a spheroid. In that case the controllability gramian is a diagonal matrix with equal diagonal entries, which means that all axes of the ellipsoid have equal length. Thus, the first optimization step boils down to a similarity transform, such that the controllability gramian of the new system becomes a diagonal matrix with equal diagonal entries. In the second step of the optimization procedure, the system is optimized with respect to its noise contribution. Rocha defines another ellipsoid, which describes the noise that is added to the state vector in each direction. While preserving the result of the first optimization step, it is possible to rotate the state space, such that the observability gramian becomes a diagonal matrix as well. In that case, the axes of the noise ellipsoid are aligned with the 'system axes'.

In [7] it is shown that, in order to maximize the dynamic range of the system, one should minimize the objective functional, which represents the relative improvement of the dynamic range and contains all parameters which are subject to manipulation by the designer. The objective functional is given by

$$F_{DR} = \frac{\max_i k_{ii}}{(2\pi)^2} \sum_i \frac{\alpha_i}{C_i} w_{ii}, \tag{7}$$

where k_{ii} and w_{ii} are the main diagonal elements of K and W, respectively, $\alpha_i = \sum_j |A_{ij}|$ is the absolute sum of the elements on the i-th row of A, and C_i is the capacitance in integrator i.

Finally, profiting from the well-known fact that the relative noise contribution of an integrator decreases when the capacitance and bias current increase, we apply noise scaling, i.e., we match an optimal capacitance distribution to the noise contributions of each individual integrator, viz. the diagonal entries of W combined with the coefficients in matrix A, resulting in [7]

$$C_i = \frac{\sqrt{\alpha_i w_{ii} k_{ii}}}{\sum_j \sqrt{\alpha_j w_{jj} k_{jj}}} \cdot C_{tot} \, . \tag{8}$$

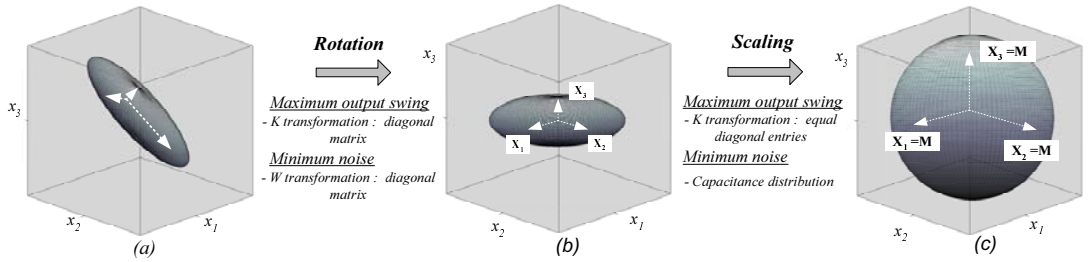

Fig. 1. Dynamic range optimization based on the similarity transformation of K and W and capacitance distribution. The coordinate axes represent the state variables and the cuboid represents the maximum signal amplitude (M) that the integrators are able to handle. (a) The initial state space representation (ellipsoid) is usually not well adapted to the integrator's representations capacity bounds (cuboid). (b) The (rotated) ellipsoid's principal axes are now aligned to the coordinate axes, as a result of the diagonalization procedure to the matrices K and W. (c) Finally, the optimized state representation is obtained by scaling the state variables and the noise. Note that the sphere represents the maximum possible mean square radius which can be fitted into the integrator's capacity cuboid.

The drawback of a dynamic-range optimal system is that its state-space matrices are generally fully dense, i.e., all the entries of the A, B, C matrices are filled with nonzero elements. These coefficients will have to be mapped on circuit components and will result in a complex circuit with a large number of interconnections. For high-order filters it is therefore necessary to investigate how a realization of the desired

transfer function having sparser state-space matrices would compare to the one having maximal dynamic range. Also, when designing high-order filters, it is very desirable to concentrate on circuits that are less sensitive to component variations. It is known that an optimal dynamic range system will also have optimal, i.e., minimal, sensitivity [8]. For a less complex circuit, it is possible, for instance, to reduce A to upper triangular by a Schur decomposition and by this reducing the number of non-zero coefficients in A. However, this transformation leads to an increase in the system noise and consequently to an increase in the objective functional (7). Another possibility is the *orthonormal ladder structure* [9], which is significantly sparser than the fully dense A matrix of the dynamic-range optimal system and the Schur decomposition and still presents a good behavior with respect to sensitivity. Fig. 2 shows a block diagram of a general orthonormal ladder filter [9]. As shown in the block diagram, the filter output is obtained from a linear combination of the outputs of all integrators.

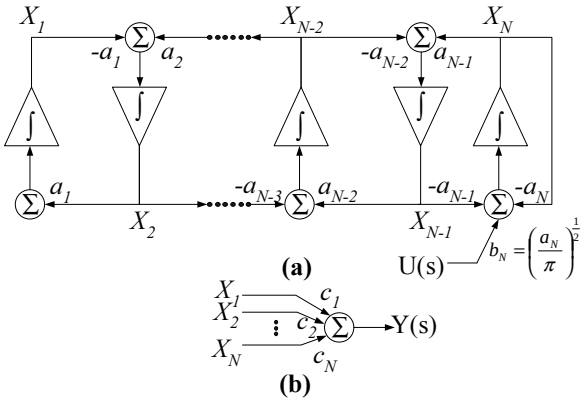

Fig. 2. Block diagram of an orthonormal ladder filter, (a) Leapfrog structure; (b) Output summing stage

The A matrix of an orthonormal ladder filter is tridiagonal and is very nearly skew-symmetric except for a single nonzero diagonal element. The B vector consists of all zeros except for the Nth element. Another property of orthonormal ladder filters is the fact that the resulting circuits are inherently state scaled, i.e., the controllability gramian is already a identity matrix. The drawback of this structure is that the system is not optimized with respect to its noise contribution. However, if an optimal capacitance distribution is applied to this suboptimal system, it can still yield some extra gain compared to the case of equal capacitances. Often this leads to a filter topology that is not too complex and has a dynamic range that is close (i.e., within a few dBs) to optimal.

IV. Designing the filter circuit

After an optimal filter topology has been selected and the appropriate coefficients have been chosen, it's time to design the filter circuit, or more specifically, design the filter's main building block, viz. the integrator.

A. Four integrator classes

In order to be able to construct the filter topology, the transfer of the integrators should be dimensionless. On a chip, the integrating element is a capacitor, which can be employed as a (passive) capacitance or as part of an active transcapacitance (amplifier) and whose transfer has a dimension equal to [Ω]. To realize a dimensionless integrator transfer function, we thus need an additional (trans)conductance. Hence, four types of integrators can be distinguished:

a conductance-capacitance integrators,
b conductance-transcapacitance integrators,
c transconductance-capacitance (gm-C) integrators, and
d transconductance-transcapacitance integrators.

Fig. 3 depicts the four integrator types that implement a voltage-to-voltage integration.

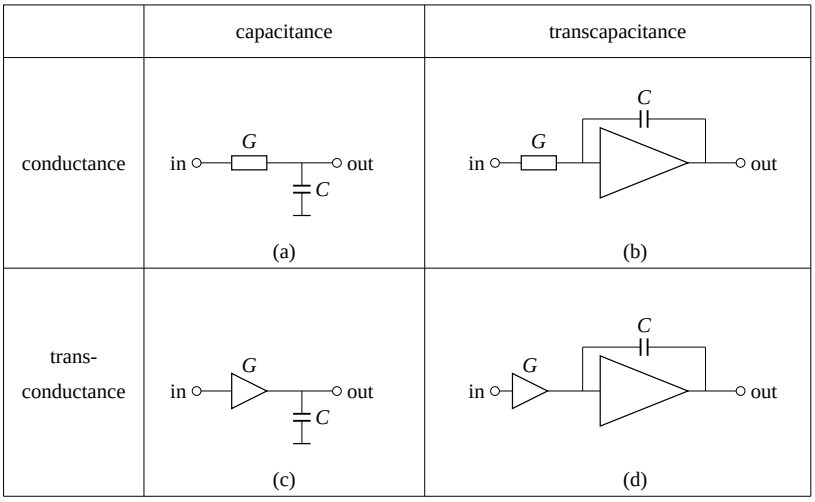

Fig. 3. Four classes of integrators

The *conductance-capacitance* integrator does not use active components. Both the required conductance and integration are implemented passively. As a result, using this type of integrator, it is not possible to implement filter transfer functions with complex poles.

The second type of integrator, the *conductance-transcapacitance* integrator, does not have this drawback and is thus used more often. In this type of integrator, the realization of the actual integration function is an active transcapacitance, often comprising an operational amplifier (op amp) having a capacitor in its (shunt) feedback path. The opamp can be designed to operate rail-to-rail at the output terminals, so full advantage is taken of the supply voltage, which entails an optimal dynamic range. The conductance can be integrated as a diffused resistor, but it could also be implemented as an MOS transistor in the triode region thus yielding a *MOSFET-C* integrator [10].

The third integrator type, the *transconductance-capacitance* (gm-C) integrator, makes use of active conductances, i.e., transconductances. The advantage of transconductors is that they are able to operate at relatively high frequencies, because their parasitic capacitances are in parallel with the integrator capacitors. Thus, they can be accounted for easily in the dimensioning of the required capacitor [11]. A major drawback, however, is that it is very difficult to implement transconductors with rail-to-rail input capability.

The fourth type of integrator is the *transconductance-transcapacitance* integrator. This integrator has no advantages over the second and third integrators mentioned. An important disadvantage is the use of two active parts, both adding to the distortion, the power consumption and the noise production.

In conclusion, the second and third type of integrators are preferred when designing filters. For both types of integrators an active part is required.

B. ELIL and ELIN

As integrators consist of two parts, a (trans)conductance and a (trans)capacitance, based on the relation of the intermediate quantity to the input and/or output quantity, linear integrators, our main filter building blocks, can be further classified into two categories [12]:

- externally linear, internally linear (ELIL), and
- externally linear, internally non-linear (ELIN).

Most of the known integrator types fall into the first category, being ELIL. In ELIL integrators the intermediate quantity is linearly related to the input and output quantities. Among them are the integrator topologies that are commonly referred to as *gm-C*, *MOSFET-C*, *opamp-RC*, *RC* and even (albeit discrete time rather than continuous time) *switched-capacitor (SC) integrators*. As in ultra low-power (i.e., nano- and micro-power) applications, resistors would become too large for integration on chip, occupying a large chip area, having a small bandwidth or have large absolute tolerances, and MOSFET conductances are bound to a limited dynamic range, we will not deal with these any further in the sequel. Instead, we will introduce a novel type

of transconductor, employing MOSFETs operating in the triode region as (active) transconductors.

For the second category, that of ELIN integrators, it holds that their external behavior is precisely linear, yet the intermediate quantity is non-linearly related to its input and output quantities. In here we find the subcategory of instantaneous companding[2] integrators, i.e., the degree of compression/expansion at a given instant depends only on the value of signals at that instant [12], [13]. Belonging to this subcategory, the class of *dynamic translinear* [13] (also known as *log-domain* [14], [15], [16] or *exponential state-space* [17]) is probably the most well known. To the subcategory of companding integrators, albeit discrete-time rather than continuous-time, also belong *switched current* [18] and *switched MOSFET* [19], [20] integrators. We will give an example of a dynamic translinear wavelet filter for biomedical applications in the next section.

But first, as promised, we will introduce a transconductor employing MOSFETs operating in the triode region.

C. A compact CMOS triode transconductor

On-chip realizations of large time constants are often required to design low cutoff-frequency (in the Hz and sub-Hz range) continuous-time filters in applications such as integrated sensors, biomedical signal processing and neural networks. To limit capacitors to practical values, a transconductor with an extremely small transconductance g_m (typically a few nA/V) is needed.

Previous works on low-voltage low-power CMOS techniques for obtaining very-low transconductances essentially concentrated on the combination of voltage attenuation at the input, source degeneration in the transconductor core and current splitting at the output [21], [22], [23], [24], keeping the transconductor input transistor(s) in saturation; whereas the lowest g_m/I_D ratio is obtained in strong-inversion triode-region (SI-TR).

In [25], a low-g_m pseudo-differential transconductor based on a four-quadrant multiplication scheme is presented, in which the drain voltage of a triode-operating transistor follows the incoming signal. Nevertheless, because triode operation needs to be sustained, the input-signal swing is rather limited. Moreover, this solution only applies to balanced structures. Although triode-transconductors, in which the signal is directly connected to the input-transistor gate, have been successfully employed in high-frequency gm-C filters [26], [27], their potential for very-low frequency filter design has not been addressed as yet.

Here we present a novel SI-TR transconductor for application in ultra low-power low-frequency gm-C filters, in which, contrary to previous approaches, the transcon-

[2] Companding is a combination of *com*pressing and ex*panding*

ductance, g_m, is being controlled by a voltage rather than by a current. In a SI-TR MOSFET, by connecting the source terminal to one of the supply rails, a control voltage applied to the drain linearly adjusts g_m, as the latter scales with the drain-source voltage V_{DS}. Since (W/L) offers a degree of freedom in the design of a particular transconductance, V_{DS} values well above the equivalent noise and offset of the bias circuit can be set, while still obtaining a very-low g_m. Consequently, filters with more predictable transfer functions can be implemented. Owing to its extended linearity, the SI-TR transconductor also handles larger signals, with no need for linearization techniques.

The proposed transconductor is depicted in Fig. 4 [28]. Input transistors M_{1A}-M_{1B}

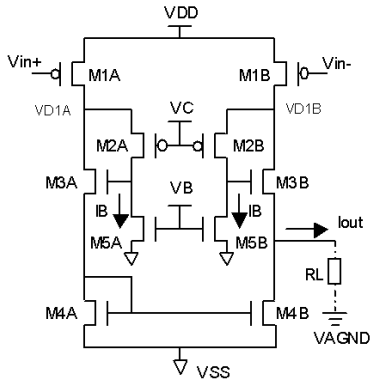

Fig. 4. Proposed triode-transconductor

have their drain voltages regulated by an auxiliary amplifier that comprises M_{2A}-M_{2B}, M_{3A}-M_{3B} and bias current sources M_{5A}-M_{5B}. A simple current mirror M_{4A}-M_{4B} provides a single-ended output. All transistors are assumed to be pair-wise matched. Although the gate-source voltages of M_{3A} and M_{4A} are stacked, their values are below the threshold voltages, so that the circuit still complies with low-voltage requirements. The gate-voltage of M_{2A}-M_{2B} is set to $V_C = V_{\mathrm{TUNE}} - V_{GS_2}$, whereas V_B imposes a bias current I_B through M_{5A}-M_{5B}. Both voltages V_B and V_C are generated on chip. Referring V_{TUNE} to V_{DD}, the transconductance of the entire circuit becomes:

$$g_m = g_{m_1} = \beta_1 V_{\mathrm{TUNE}}, \tag{9}$$

with $\beta_1 = (W/L)_1 \mu_p C_{\mathrm{ox}}$.

P-type input transistors were chosen because of their lower mobility and 1/f-noise coefficients as compared to similar parameters of n-MOSFETs. Except for M_{1A}-M_{1B} that stay in SI-TR, all remaining devices work in weak inversion and saturation. Assuming M_{5A} and M_{5B} to be ideal current sources, the transconductor output resistance

r_{out} is given by

$$r_{\text{out}} \approx r_{ds1}(1 + g_{m_2} r_{ds_2}) \tag{10}$$

Even though a common-drain configuration (M_{3B}) is seen from the output node, the transconductor still exhibits a relatively high output resistance, as the loop gain around M_{2B} and M_{3B} is relatively large.

Internal voltages V_B and V_C are derived from the circuit shown in Fig. 5. The generator is structurally alike the transconductor, with M_{1G}, M_{2G} and M_{3G} matched to their counterparts. An opamp equates the drain voltage to external voltage V_{TUNE}, so that $V_C \approx V_{\text{TUNE}}$ $|V_{GS_{2G}}|$. Since $V_{GS_{2G}} = V_{GS_{2A}} = V_{GS_{2B}}$, the expected value of V_C is achieved. A low-voltage OTA, with a topology similar to the one in [27], is employed as opamp. A proper setting of the current gain B ($B > 1$) in current mirror M_{4G}-M_{5G} guarantees an optimal signal swing at both input and output, ensuring class-A operation of the transconductor.

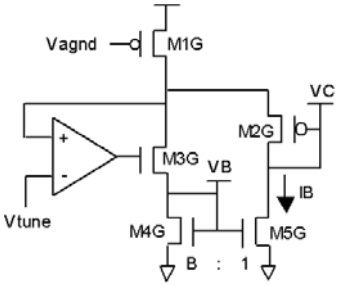

Fig. 5. Bias generator

Analysis of the noise performance of the proposed transconductor reveals that, as $g_{m_1} r_{ds_1} \ll 1$, the noise is dominated by the noise contributions of M_{2A} and M_{2B}. Their equivalent input noise voltage power spectral densities $S_{v_n,2A/B,\text{eq}}$, in [V^2/Hz] equal

$$S_{v_n,\text{eq}} = \frac{2kT/g_{m_2}}{(g_{m_1} r_{ds_1})^2} \tag{11}$$

which is the minimum one can achieve from an SI-TR transconductor.

As the gate length of M_1 is chosen considerably long to obtain a very-low g_{m_1}, its 1/f noise is naturally minimized.

To back up the theoretical analysis, a SI-TR transconductor with g_m in the order of nA/V was designed. The design complies with $V_{DD} = 1.5$V and a standard 0.35μm n-well CMOS process, with typical parameters V_{T_n} = 0.50V, V_{T_p} = -0.60V, g_n = 0.58$V^{1/2}$, g_p = 0.45$V^{1/2}$, μ_n = 403cm^2/Vs, μ_p = 129cm^2/Vs and C_{ox} = 446nF/cm^2. Flicker-noise coefficients are KF_n = 2.81e-27A^2s/V, KF_p = 1.09e-27A^2s/V, AF_n = 1.40, AF_n = 1.29 and $EF_n = EF_p = 1$.

The tuning interval ranges from 10mV to 50mV, which implies 1.1nA/V $\leq g_{m_1} \leq$ 5.5nA/V. The optimal V_{AGND} is 0.6V, theoretically limiting the signal amplitude to 185mV. Transistor sizes (in μm/μm) are $(W/L)_1$ =(1.2/600), $(W/L)_2$ = (10/100), $(W/L)_3$ = (12/2.4) and $(W/L)_4 = (W/L)_5$ = (40/40). These dimensions maximize the signal swing at both input and output and trade off 1/f-noise and layout area. At nominal $V_{\mathrm{TUNE}} = 20$mV, the calculated g_{m_1} and common-mode current $I_{D_{1,\mathrm{CM}}}$ are 2.2nA/V and 0.63nA, respectively. Setting B=1.5 results in $I_B \approx 0.25$nA, a good compromise between signal swing, 1/f-noise, thermal noise and auxiliary-amplifier power consumption.

Simulations were carried out using PSPICE 9.2 with Bsim3v3 models. For a 1kΩ load, fixing $V_{\mathrm{in}-}$ at V_{AGND} and sweeping $V_{\mathrm{in}+}$, the g_{m_1} dependence on the tuning voltage (10mV $\leq V_{\mathrm{TUNE}} \leq$ 50mV) is plotted in Fig. 6. The transconductance remains almost constant in the linear region, scaling linearly with V_{DS_1}.

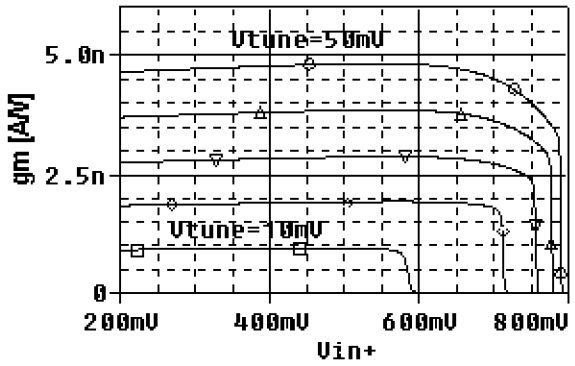

Fig. 6. Dependence of g_m on signal level and tuning

Transconductor noise figures from PSPICE are in excellent agreement with the performed noise calculations. The transconductor equivalent noise voltage for a 100mHz–10Hz bandwidth is 260$\mu\mathrm{V_{RMS}}$. Similarly, the input-referred noise of the V_C generator is 42$\mu\mathrm{V_{RMS}}$, so that for the lowest V_{TUNE} of 10mV, a tuning-to-noise ratio (TNR) of 47dB is obtained. Given that transistor geometries are well defined in modern fabrication processes, g_m can be controlled to a good extent, as it relies on $(W/L)_1$ and V_{TUNE} only.

V. A 10th-order ultra low-power low-voltage dynamic translinear wavelet filter

This last section illustrates the design procedure outlined in the previous sections for implementing a filter whose impulse response is a Morlet [29]. The real part of this particular wavelet is of special interest for the local analysis of non-stationary signals as can be found in electrocardiograms. Its application in pacemaker frontends makes

an ultra low-power implementation mandatory. In the coming subsections, we first derive a suitable Morlet filter transfer function. Subsequently, we optimize the Morlet filter state-space description. Finally, we implement the optimized (orthonormal) ladder structure with log-domain integrators as main building blocks. Simulations and measurements that prove the correctness and robustness of the proposed design methodology will be provided as well.

A. Designing the Morlet filter transfer function

The design of the Morlet filter transfer function takes off with the (real part of the) desired impulse response $g(t)$ of the Morlet filter, i.e., a Gaussian-windowed sinusoid:

$$g(t) = \cos(5\sqrt{2}t)e^{-(t-3)^2},\ t \geq 0. \tag{12}$$

Since only causal filters can be implemented, this function is truncated at $t = 0$ and a time shift $t_0 = 3$ is introduced. The choice of this time shift involves an important trade-off that has to be made with care. If t_0 is chosen too small, the truncation error becomes too large. On the other hand, if t_0 is chosen too large, the function to be approximated will become very flat near $t = 0$. This effectively introduces a time-delay, which implies that a good fit can only be achieved with a filter of high order and thus compromises the power consumption.

The Laplace transform of (12) is not yet a suitable rational function and thus a low-order approximation has to be made. A [8/10] Padé approximation yields [30]:

$$H(s) = \frac{0.9s^8 - 13s^7 + 177s^6 - 618s^5 + 345s^4 + 7{\cdot}10^4 s^3 - 4{\cdot}10^5 s^2 + 2{\cdot}10^6 s - 3{\cdot}10^6}{s^{10} + 13s^9 + 336s^8 + 3{\cdot}10^3 s^7 + 4{\cdot}10^4 s^6 + 2{\cdot}10^5 s^5 + 2{\cdot}10^6 s^4 + 8{\cdot}10^6 s^3 + 4{\cdot}10^7 s^2 + 9{\cdot}10^7 s + 3{\cdot}10^8}. \tag{13}$$

Fig. 7 depicts the ideal ($g(t)$) and the approximated ($h(t)$) Morlet filter impulse responses, respectively. A good fit can be observed.

B. Designing the Morlet filter topology

Applying the state-space optimization method described in Section III, we find that the objective functional F_{DR} becomes equal to 96.98. This is the absolute minimum value of the objective functional associated with this transfer function.

To improve the state-space matrices' sparsity without compromising the dynamic range and sensitivity to parameter variations too much, an orthonormal ladder structure is implemented. The A, B, C and D matrices of this structure for the defined transfer function are given by:

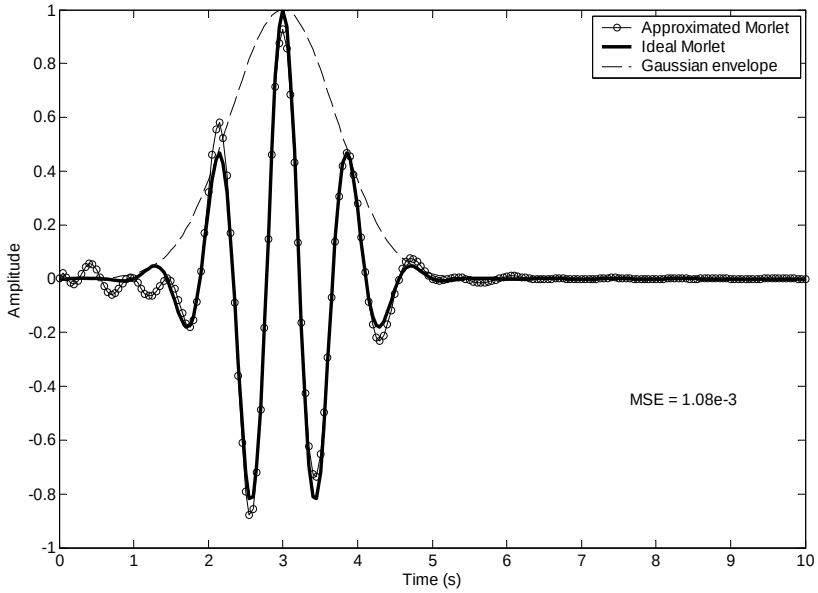

Fig. 7. Impulse response of the Morlet filter: the ideal impulse (dashed line) and the approximated impulse (solid line)

$$
A = \begin{bmatrix}
0 & 6.54 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-6.54 & 0 & 1.83 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -1.83 & 0 & 6.59 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -6.59 & 0 & 2.72 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -2.72 & 0 & 6.37 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -6.37 & 0 & 3.89 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -3.89 & 0 & 6.27 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -6.27 & 0 & 5.88 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -5.88 & 0 & 10.47 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -10.47 & -13.31
\end{bmatrix},
$$

$$
B = \begin{bmatrix}
0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 2.05
\end{bmatrix},
$$

$$
C = \begin{bmatrix} 0.75 & -1.34 & 0.75 & 0.68 & -0.57 & 0.44 & -0.002 & -0.10 & 0.04 & 0 \end{bmatrix},
$$

$$
D = \begin{bmatrix} 0 \end{bmatrix} \tag{14}
$$

In order to minimize the noise contribution, an optimal capacitance distribution is applied, resulting in a normalized capacitance distribution $(C_1, ..., C_{10}) = C'$(0.142, 0.162, 0.110, 0.117, 0.086, 0.091, 0.073, 0.080, 0.073, 0.061) , where C' represents the unit-less value of the total capacitance expressed in F. This leads to an objective functional $F_{DR} =$ 147.90, which is not so far from the optimum case. The dynamic range has decreased by only 1.83dB.

C. Designing the Morlet filter circuit

A simple bipolar multiple-input low-power log-domain integrator [31] will be used as the basic building block for the implementation of the above state space description. This log-domain integrator is shown in Fig. 8 [31]. A pair of log-domain cells with opposite polarities and an integrating capacitor form the core of the integrator. V_{ip} and V_{in} are the noninverting and inverting input voltages, respectively, and the input currents are I_{ip} and I_{in}, which are superimposed on the dc bias currents. The output voltage V_o is given by the voltage across the capacitor. The circuit is composed of two identical log-domains cells, a voltage buffer and a current mirror. The log-domain cells Q_1-Q_2 and Q_3-Q_4 generate the log-domain currents I_{c2} and I_{c4}, respectively. A voltage buffer realized by Q_5-Q_6 is inserted between them. Therefore, the output log-domain voltage V_o at the emitter of Q_2 also appears at the emitter of Q_4. Finally, to obtain a log-domain integrator equation, we use a current mirror Q_7-Q_8 to realize the difference between the two log-domain currents on the capacitor node. The connection from the bases of transistors Q_7 and Q_8 to the collector of Q_6 closes the feedback loop around Q_6 and Q_7. This connection is convenient because it ensures that the overall voltage headroom is minimized. The equation that relates the input and output voltages to the current flowing in the integrating capacitor becomes

$$C_i \frac{dV_o}{dt} = (I_o + I_{ip}) e^{\frac{V_{ip} - V_o}{V_T}} - (I_o + I_{in}) e^{\frac{V_{in} - V_o}{V_T}}. \tag{15}$$

Notice that the input and output voltages of the integrator are at the same dc level. Therefore log-domain filter synthesis can easily be achieved by direct coupling of these integrators.

D. Synthesis of the log-domain state-space filter

By applying a simple mapping to the linear state-space equations (14), we can obtain the corresponding log-domain circuit realization which employs the above log-domain integrator.

The block diagram of the log-domain implementation of (14) is illustrated in Fig. 9, using the universal log-domain cell symbol described in [32] and shown in Fig. 8b.

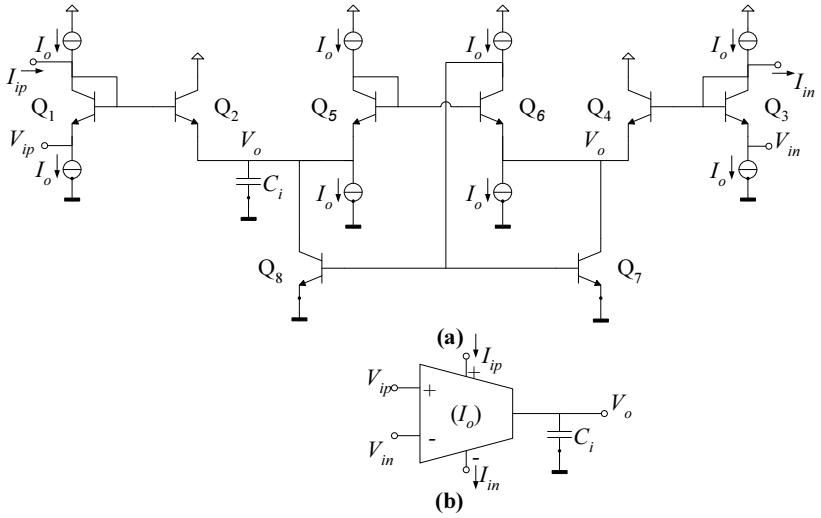

Fig. 8. a) The multiple-input low power log-domain integrator, and (b) its symbol [30]

Note that each column of the filter structure corresponds to a row in the state-space formulation. The parameter A_{ij} is implemented by the corresponding log-domain integrator with bias current $I_{A_{ij}}$, defined by a current matrix A_I

$$A_I = V_T C_i \cdot A \tag{16}$$

The input section, as governed by the state-space vector B, is realized by the first row from the top of Fig. 9. The parameter B is related to the current by

$$B = \frac{I_o}{V_T C_i} \tag{17}$$

Consequently, the B coefficients are not individually controllable by bias currents, and they have to be set equal to each other or to zero. Fortunately, this is the case in (14), where only one non-zero parameter of the B vector is present, as then it is not necessary to transpose the state-space system. The bias current vector C_I, which controls the vector C, is defined as

$$C_I = I_o \cdot C \tag{18}$$

E. Simulation and measurement results

To validate the circuit principle, we have simulated the log-domain state-space filter using models of IBM's $0.18\mu m$ BiCMOS IC technology. The circuit has been designed to operate from a 1.2V supply. Fig. 10 shows the impulse response of the wavelet

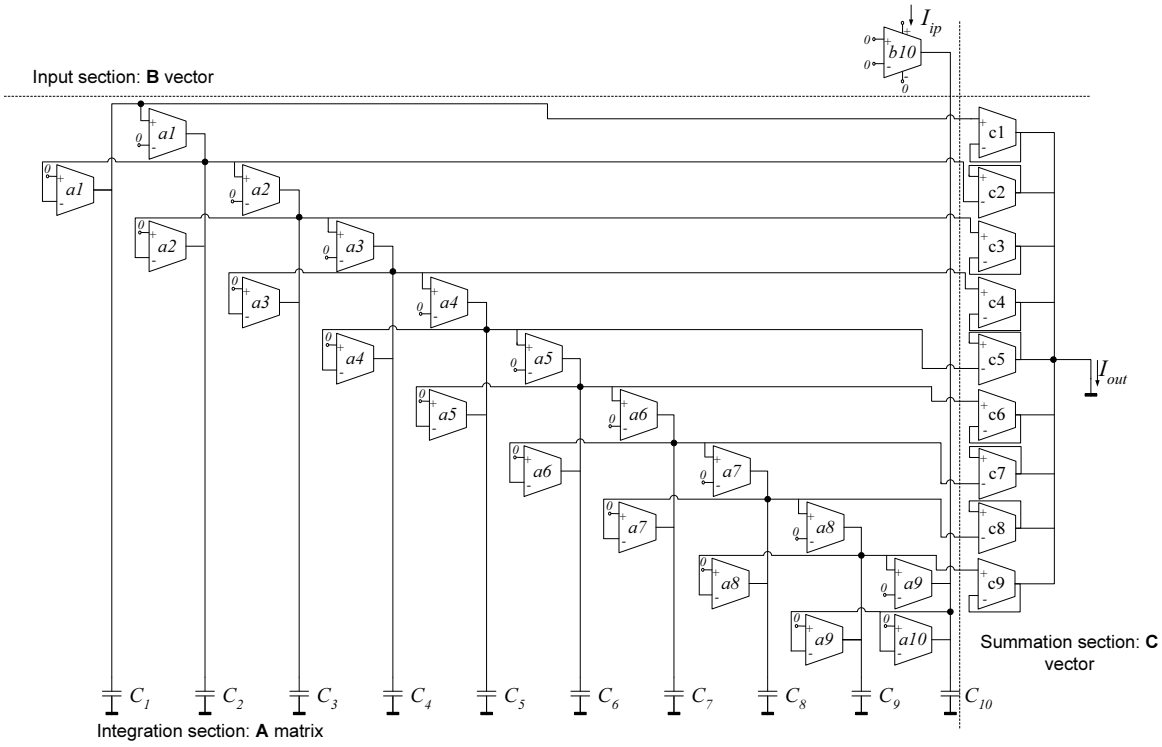

Fig. 9. Complete state-space filter structure

filter. The excellent approximation of the Morlet wavelet can be compared with the ideal Morlet function to confirm the performance of the log-domain filter. Fig. 11 shows the Monte Carlo analysis for process and mismatch variation of the technology in use. As evident from the Monte Carlo simulation (i.e. after 100 runs), the system characteristics show insensitivity towards both absolute and relative variations in the process parameters. Even though the impulse response may be slightly affected, the targeted wavelet analysis will be preserved.

Subsequently, the Morlet filter was implemented in the same IC technology. Fig. 12 shows a photomicrograph of the chip. The 10 integrator capacitors are clearly visible. Fig. 13 shows the measured impulse response. An excellent agreement with both the simulated impulse response and the ideal Morlet function (Fig. 10) can be observed.

The total filter's current consumption is 1.5μA with a 100pF total capacitance. The output current presents an offset of approximately 46.61pA. The rms output current noise is 66.97pA, resulting in a DR at the 1-dB compression point of approximately 30dB. The power efficiency of any bandpass continuous-time filter is a figure of merit to be able to compare various filter topologies and can be estimated by means of the power dissipation per pole, center frequency (f_c), and quality factor (Q) defined as

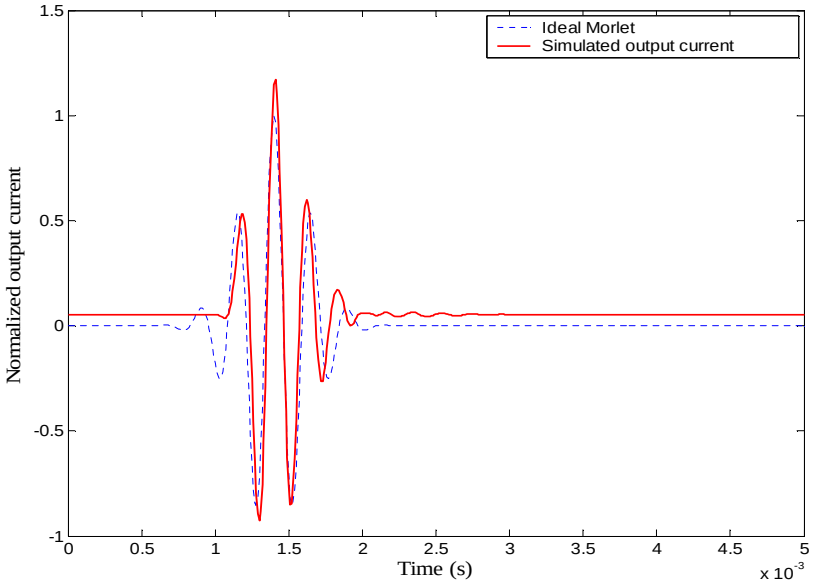

Fig. 10. Simulated impulse response

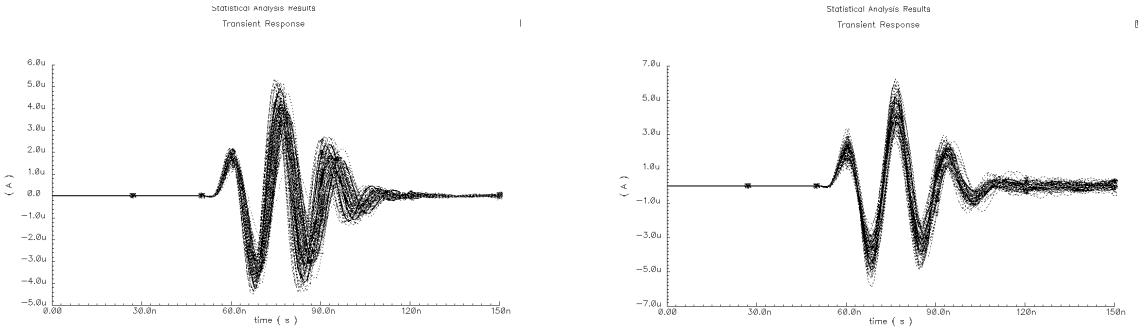

Fig. 11. Monte Carlo analysis (a) process variation, (b) mismatch variation

[33]

$$\text{Power per pole \& bandwidth} = \frac{P_{diss}}{n \cdot f_c \cdot Q}, \tag{19}$$

where P_{diss} is the total power dissipation and n is the order of the filter. The power efficiency of this filter equals 11.83pJ.

By changing the values of the bias currents along a dyadic sequence, one can obtain the impulse responses of a dyadic scale system, as illustrated in Fig. 14. Alternatively, one also may change the capacitance values, C_i. To implement a wavelet system, which usually consists of 5 dyadic scales, one needs to implement a filter bank (a parallel

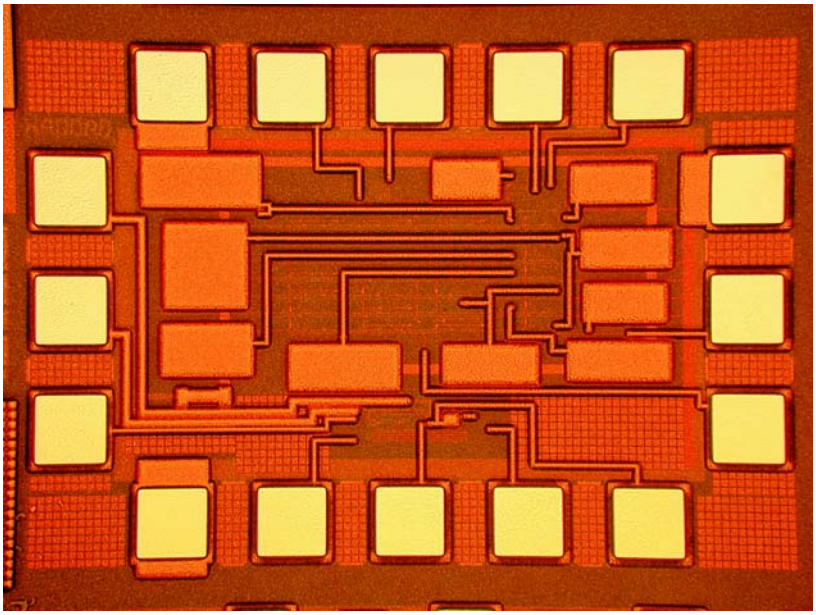

Fig. 12. Photomicrograph of the implemented Morlet filter

structure) with a total capacitance of 193.75pF, preserving the same bias current. This result indicates that a wavelet system is feasible.

Finally, in order to show that the same procedure can be applied for high frequency applications, we tuned the frequency response of the filter by varying the bias current over about four decades with center frequencies ranging from 5.8kHz to 58MHz, while preserving the impulse response waveform. Again, one can obtain the wavelet scales around this frequency (i.e. 58 MHz) by either scaling the current or the capacitance value accordingly. The performance of the filter is summarized in Table I.

VI. Conclusions

Filtering is an indispensable elementary signal processing function in many electronic systems. In many critical applications, e.g., in portable, wearable, implantable and injectable devices, one should maximize the dynamic range and, at the same time, minimize the power consumption of the filter. This joint optimization can take place in different phases, the filter transfer function design phase, the filter topology design phase, and the filter circuit design phase.

In the filter transfer function design phase, the filter functional input-output relation is mapped on a suitable filter transfer function. Two approximation techniques were introduced: the Padé approximation and the L_2 approximation. The Padé approximation is employed to approximate the Laplace transform of the desired filter

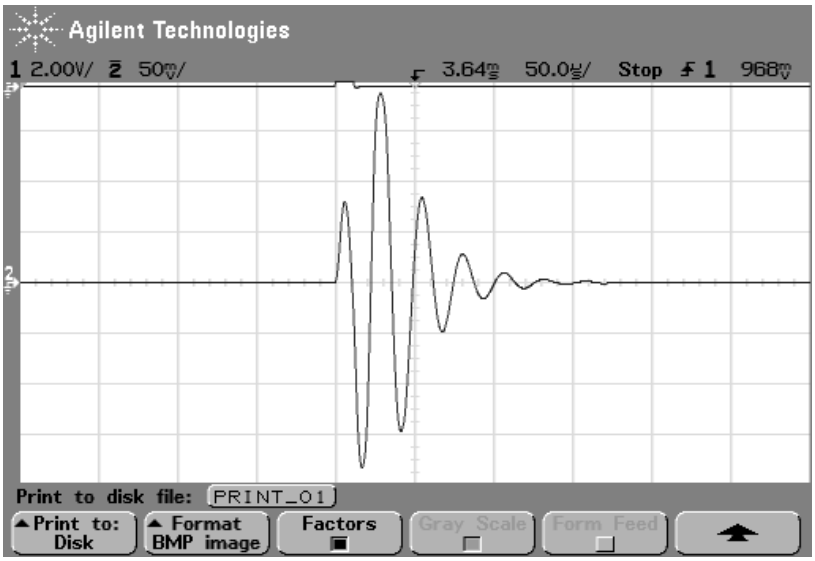

Fig. 13. Measured impulse response

transfer function $G(s)$ by a suitable rational function around a selected point. The L_2 approximation offers a more global approximation, i.e., not concentrating on one particular point, and has the advantage that it can be applied in the time domain as well as in the Laplace domain. It is based on the minimization of the squared L_2 norm of the difference between the desired transfer function and the approximation $H(s)$ over the imaginary axis $s = j\omega$, which is equivalent to minimization of the squared L_2 norm of the difference between $g(t)$ and $h(t)$.

In the filter topology design phase, the filter transfer function is mapped on a suitable filter topology. For this, the filter transfer function is written in the form of a state-space description, which subsequently is optimized for dynamic range, sparsity and sensitivity. In the determination and optimization of the dynamic range the filter's controllability and observability gramians play an important role. Dynamic range optimization boils down to transforming the controllability gramian such that it becomes a diagonal matrix with equal diagonal entries, transforming the observability gramian such that it also becomes a diagonal matrix, and capacitance distribution. To improve the state-space matrices' sparsity the dynamic-range optimized matrices can be transformed into a form that describes an orthonormal ladder filter. After applying capacitance distribution, a filter topology is found that is not too complex and has a dynamic range that is close (i.e., within a few dBs) to optimal.

Finally, in the filter circuit design phase, the filter topology is mapped on a circuit. A classification of integrators was presented. Falling in the category of transconductance-capacitance (gm-C) integrators, a novel nA/V CMOS transconductor for

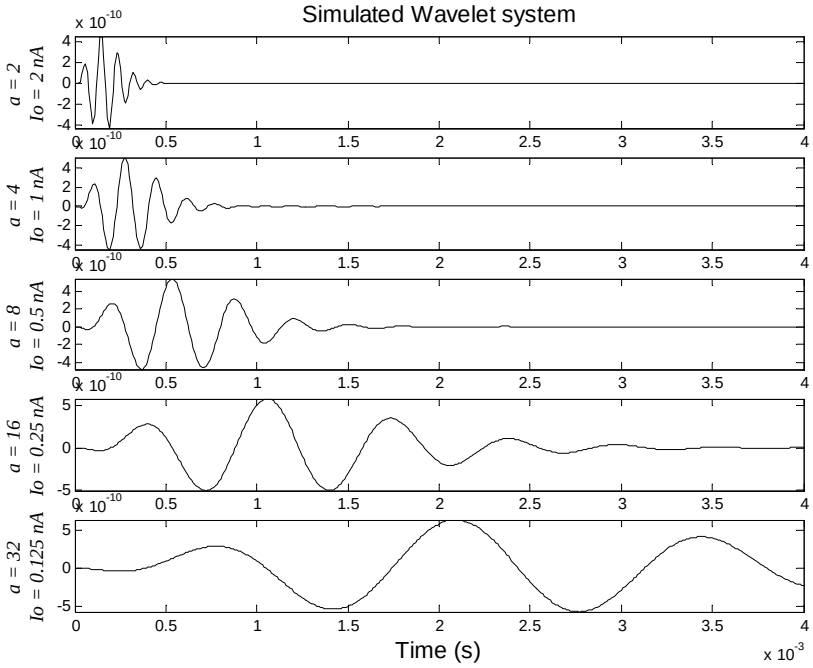

Fig. 14. Simulated impulse responses of a Morlet-based wavelet system with 5 scales. The scales are obtained by varying the current (from 0.125nA to 2nA) or the capacitance (from 100pF to 6.25pF).

ultra-low power low-frequency gm-C filters was introduced. Its input transistors are kept in the triode-region to benefit from the lowest g_m/I_D ratio. The g_m is adjusted by a well defined (W/L) and V_{DS}, the latter a replica of the tuning voltage V_{TUNE}. The resulting design complies with V_{DD}=1.5V and a 0.35μm CMOS process. Its transconductance ranges from 1.1nA/V to 5.5nA/V for 10mV $\leq V_{\mathrm{TUNE}} \leq$ 50mV.

To illustrate the entire filter design procedure, a dynamic translinear Morlet filter has been designed. Simulations and measurements demonstrate an excellent approximation of the Morlet wavelet base. The circuit operates from a 1.2-V supply and a bias current of 1.2μA.

Acknowledgement

The author would like to acknowledge the many contributions to this work made by Sumit Bagga, Igor Filanovsky, Gert Groenewold, Joel Karel, Cleber Marques, Bert Monna, Jan Mulder, Ralf Peeters, Daniel Rocha, Pietro Salvo, Arie van Staveren, Nanko Verwaal and Ronald Westra, D. Harame and IBM Microelectronics for fabrication access and fabrication of the testchip, and the financial support of part of this work by FAPESP, The State of São Paulo Research Foundation, CNPq, the Brazilian National Counsel of Technological and Scientific Development, and STW, the Dutch

Technology	0.18μm BiCMOS	
Bias current	$I_o = 1$nA	$I_o = 10\mu$A
Total capacitance	100pF	100pF
Supply voltage	1.2V	1.8V
Center frequency (f_c)	5.8kHz	58MHz
Power dissipation	1.5 μW	24.3mW
Dynamic Range (1-dB)	30 dB	30 dB
Noise current (rms)	66.97pA	481.3nA
Supply voltage range	1V - 1.6V	1.7V - 2.1V
Power dissipation per pole f_c and Q	11.834pJ	13.96pJ

TABLE I

PERFORMANCE PER SCALE FOR TWO DIFFERENT OPERATING FREQUENCIES

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