A Self-Calibrating RF Energy Harvester generating 1V at -26.3 dBm

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Abstract

This paper presents a self-calibrating RF energy harvester capable of harvesting at lower input power levels than current state-of-the-art RF harvesters. A 5 stage cross-connected bridge rectifier is brought at resonance with a high-Q loop antenna by means of a 7-bit binary weighted capacitor bank. A control loop compensates any variation in the antenna-rectifier interface and passively boosts the antenna voltage to enhance the sensitivity. The rectifier and capacitor bank have been implemented in standard 90nm CMOS technology, includes ESD protection and are integrated on the antenna. Measurements in an anechoic chamber at 868 MHz show a -26.3 dBm sensitivity for 1V output and 25 meter range for a 1.78 W RF source in an office corridor. The maximum power efficiency of the complete harvester is 31.5%.

Introduction

The ever decreasing power consumption of integrated circuits provides the opportunity of using an energy harvester to power simple sensor nodes. Dedicated or ambient RF energy sources can be used in many applications where energy sources such as light, vibrations and thermal gradients are not available.

Apart from designing for efficient power transfer, the harvester can be designed for superior sensitivity leading to an increased area that can be covered by an RF source. This also allows the possibility to harvest ambient RF energy. However, it proves to be very challenging to design an RF harvester with good performance for an input power of -20 dBm or less. Today's RF harvesters either have poor sensitivity [1] or require calibration [2], a special technology process [3] or a large chip/antenna area [4]. In this work we present a small self-calibrating and highly sensitive RF energy harvester in standard CMOS technology.

RF rectifier

The first concern of designing a large range RF harvester is to reduce the turn-on power threshold. Passive voltage boosting is an effective way to increase the input voltage by combining a high-Q inductive antenna with the capacitive rectifier. However, a conventional 50Ω conjugate-matched antenna interface like in [4] and [5] will severely limit the voltage boost at low power levels. Therefore, we use a mismatched and highly reactive interface with a small antenna radiation resistance of 10Ω [6].

The core of the harvester consists of a conventional cross-connected bridge rectifier (Fig. 1). Different from other published harvesters, here, a control loop is added to tune the impedance such that a resonance is created with the antenna. The loop consists of a 7-bit binary weighted capacitor bank that is controlled by an up-down counter. The harvester initially charges the storage capacitor to the turn-on voltage of the loop. Then the energy transfer to the off-chip capacitor is optimized by maximizing the slope of the load voltage with the capacitor bank.

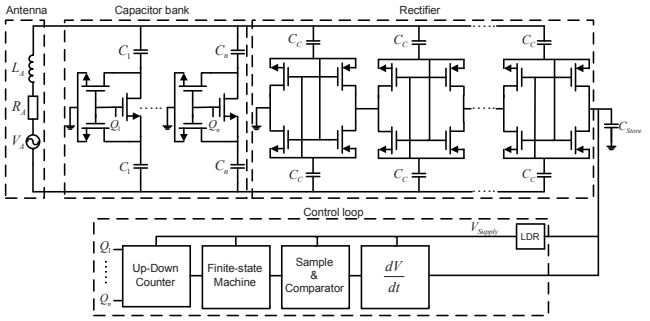


Fig. 1: Multi-stage RF energy harvester with control loop

Any impedance variation in the interface that may occur in a realistic environment will be compensated for by the control loop, making the RF energy harvester very robust while fully benefiting from the passive voltage boost obtained from the high-Q antenna. Once the loop is calibrated, it can be turned off so that it is not loading the rectifier for very low power levels.

A 5 stage rectifier and 7-bit capacitor bank have been implemented in TSMC 90nm CMOS technology and are ESD protected. Fig. 2 shows an active die area of only 0.029mm². Each stage is sized for maximum efficiency and high input impedance. More stages will not significantly improve the performance due to the body effect, the power loss in each additional stage and the decreasing input impedance that lowers the passive voltage boost.

The capacitor bank consists of 128 unit capacitor switches, where each unit consists of a main switching transistor, two small biasing transistors to enhance the Q-factor and two custom designed metal-metal capacitors. The unit capacitor switch shown in Fig. 2 uses metal 6 and 7 stacked together with minimum width and spacing to minimize parasitics. Post layout simulations show a 4 fF capacitance for an area of 2.4x2.5µm.

As a proof of principle, the control loop is implemented off-chip. However, preliminary simulation results show that a similar mainly digital control loop can be implemented on-chip. When optimizing for low leakage current, the average power of the control loop can be in the order of 30 nW due to the relaxed requirements on the clock speed and accuracy (~kHz range). The loop can be activated around 300 mV, meaning that the storage capacitor should not be discharged lower than this voltage to ensure continuous operation.

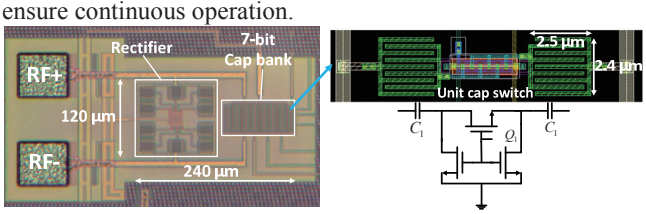


Fig. 2: Chip microphotograph and unit capacitor switch layout

Antenna-rectifier co-design

The antenna of the harvester needs to be highly inductive. Considering the tradeoffs between radiation efficiency, sensitivity and tuning range, an antenna impedance of 10+j400Ω was chosen. The proposed antenna structure in Fig. 3 allows enough freedom to tune the real and imaginary part. The chip is integrated on the backside of the antenna to minimize its effect on the antenna performance. The RF inputs are bond wired to vias that connect to the antenna feed point. The other signals are connected to a control logic & measurement board. As a first prototype, the antenna is fabricated on 1.6 mm FR4 substrate. The simulated antenna impedance is 11+j398.8 Ω with a radiation efficiency of 46.5%.

Measurement results and conclusions

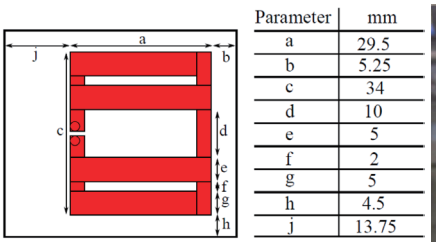
The RF energy harvester is measured in an anechoic chamber at the 868 MHz European ISM band. The setup is calibrated using two identical broadband antennas separated by 3.6 meter to ensure far-field conditions. Since the antenna dimensions (a= λ/11.3 and c= λ/9.8) are much smaller than a wavelength, the antenna performance is included in the measurement by defining the input power as the maximum power available from an isotropic antenna (0 dBi). As the control loop is off-chip, its power consumption during calibration is not included in the measurements.

The measured output voltage for closed and open loop scenarios is shown in Fig. 4a, where Rload=1 MΩ and Pin=-20 dBm. In the open loop scenario, the control loop is continuously counting from the minimum to maximum capacitance value. Clearly, an optimum capacitance exists that corresponds to maximum power. In the closed loop scenario, this maximum performance is obtained. The charging time vs. Pin for a 450 nF load capacitance is shown in Fig. 4b.

The measured output voltage vs. input power in Fig. 5a shows an excellent sensitivity for low power levels. A capacitor can be charged to 1V with only -26.3 dBm input power and takes approximately 2 seconds for a 450 nF capacitor. As the charging time scales linearly with the capacitor size, these graphs give a good indication of the available energy as a function of input power and time. Figure 5b shows that the power efficiency (η=Pload/Pin) peaks around -15 dBm with a maximum of 31.5%. This includes all losses of the antenna, interface and rectifier.

To test the harvester in a realistic environment, a 1.78W Effective Isotropic Radiated Power (EIRP) RF source was used to measure the line-of-sight distance in an office corridor. In this experiment, 1V could be generated from 25 meter distance, corresponding well with -26.3 dBm sensitivity.

Table I shows a comparison with state-of-the-art RF energy harvesters that have been measured with an antenna. This work shows superior wireless range performance with respectively 1.4x and 1.8x smaller antenna area compared to [2] and [7] while operating at a lower frequency. Moreover, the rectifier and capacitor bank are implemented in standard CMOS technology, occupies only 0.029 mm² and requires no calibration procedure. To our knowledge, this work demonstrates the largest range RF energy harvester to date.



Parameter	mm
a	29.5
b	5.25
c	34
d	10
e	5
f	2
g	5
h	4.5
j	13.75

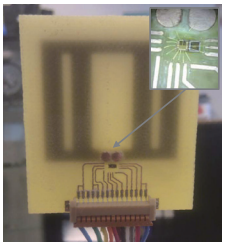
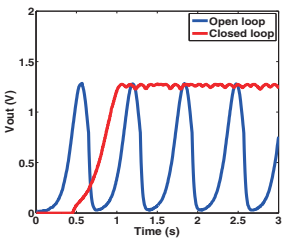
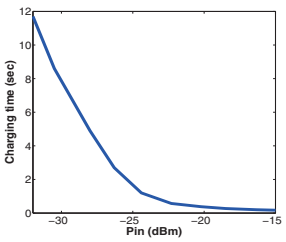


Fig. 3: Antenna dimensions and chip integration

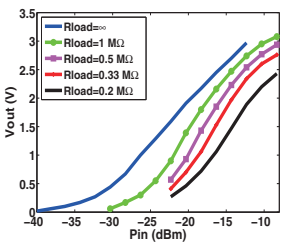


(a)

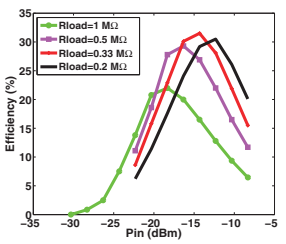


(b)

Fig. 4: (a) Optimizing control loop (b) 10-90% charging time vs. Pin



(a)



(b)

Fig. 5: (a) Vout vs. Pin (b) Power efficiency vs. Pin.

Table I: Performance summary and comparison with previous work

Parameters	This work	[2] 2008 JSSC	[3] 2007 TCAS I	[4] 2006 JSSC	[7] 2007 TCAS I
Technology	**90nm**	0.25µm	0. 18µm	0.25µm	0. 18µm
Die area	**0.029 mm²**	0.4 mm²	0.084 mm²	n.a.	n.a.
Antenna area	**20.9 cm²**	30 cm²	n.a.	n.a.	37.4 cm²
Frequency	**868 MHz**	906 MHz	900 MHz	450 MHz	970 MHz
Requirement	**Control loop**	External pre-charge	Zero V_{TH} transistors	Low V_{TH} transistors	-
Sensitivity (Rload=∞)	**-26.3 dBm 1V**	-22.6 dBm 2V	n.a.	-19.58 dBm 1V	-17.7 dBm 0.8V
Max Efficiency	**31.5% -15 dBm**	30%[(a)] -8 dBm	26.5% -11dBm	10.9% -12 dBm	37%[(a)] -18.7 dBm
Measured Distance	**25 meter @ 1.78W**	15 meter @ 4W	1.1 meter @ 0.32 W	1.65 meter @ 55 mW	n.a.

(a): Calculated from graph

References

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