A 2.4 GHz Power Amplifier With 40% Global Efficiency at −5 dBm Output for Autonomous Wireless Sensor Nodes

Mark Stoopman, *Student Member, IEEE*, Kathleen Philips, *Member, IEEE*, and Wouter A. Serdijn, *Fellow, IEEE*

***Abstract*—Energy scavenged Wireless Sensor Nodes (WSNs) usually require a small output power (<0 dBm) due to their short-range application and limited power budget. This makes the RF Power Amplifier (PA) design differ from conventional PAs as the output power becomes comparable to the PA driver's power consumption. In this letter, a 2.4 GHz tuned switching PA and driver is proposed with an on-chip duty cycle calibration loop to enhance efficiency. A prototype is fabricated in 40 nm CMOS technology and supports On-Off keying (OOK). Measurements show a global efficiency of 40% when delivering −5 dBm to a 50 Ω load.**

***Index Terms*—Calibration, duty cycle, efficiency, power amplifier (PA), wireless sensor node (WSN).**

I. Introduction

THE power balance between an energy harvester and a sensor node is one of the main reasons why autonomous wireless sensor nodes are not yet widely commercialized into products. The limited power budget and short-range application makes the RF power amplifier design differ from conventional power amplifiers (PAs) with >10 dBm output as the output power becomes comparable to the power consumed by the PA driver. The combined power consumption of the PA and the PA driver thus becomes critical for relatively low output power levels as the global efficiency is defined as

$$\text{Global efficiency} = \frac{P_{RF\text{out}}}{P_{\text{PA,DC}} + P_{\text{Driver,DC}}}. \qquad (1)$$

A 2.4 GHz switching mode PA with 200 fF input capacitance and 1.1 V nominal supply would require a substantial 580 μW of driving power when considering that the switching power of a CMOS inverter scales with $C_{\text{PA}}V_{\text{DD}}^2 f$. For an output power of 300 μW, this would result in a maximum global efficiency of only 34%, even when assuming 100% drain efficiency. This becomes evident when looking at Fig. 1, which shows a performance survey of recently published 2.4 GHz CMOS PAs [1]–[9]. As expected, a clear reduction in efficiency is observed with decreasing output power. Class-E PAs can have good efficiency at high output power, but are challenging to design for <0 dBm due to the complex matching network. For <0 dBm output power, class-D PAs are frequently used as they can provide good drain efficiency, but also require a large driving power which reduces the global efficiency. This issue is solved in [3] by adding an on-chip inductor to resonate with the PA input capacitance at the expense of increased chip area.

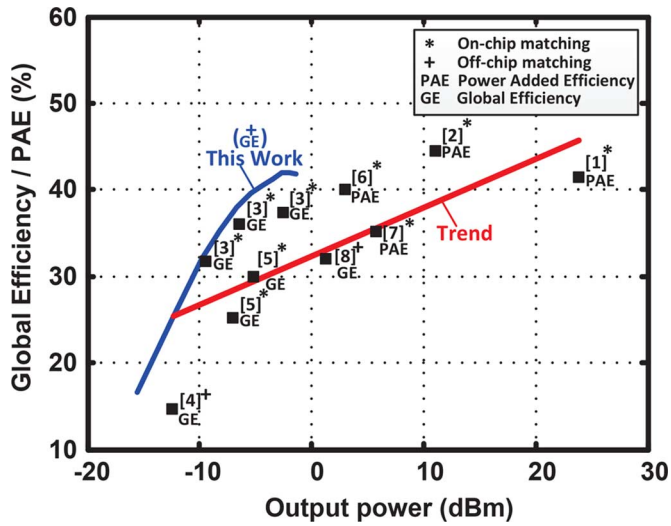

Fig. 1. Survey of 2.4 GHz CMOS PA global efficiency/power added efficiency versus output power.

This letter presents an alternative approach to the design of a 2.4 GHz switching PA using an on-chip duty cycle calibration loop to increase the global efficiency at <0 dBm output power.

II. Tuned Switching Power Amplifier

The core of the PA consists of a single-ended inductively loaded NMOS cascode transistor (Fig. 2). Transistor M1 is strongly driven by a rail-to-rail input voltage with duty cycle $d = W/T$ and thus acts as a switch. The output matching network is tuned at the fundamental RF frequency and provides impedance transformation to 50 Ω. The cascode transistor M2 limits the maximum voltage swing of M1 to improve reliability and also reduces the effective input capacitance C_{PA} by suppressing the Miller effect.

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M. Stoopman and W. A. Serdijn are with the Section Bioelectronics, Delft University of Technology, Delft 2628 CD, The Netherlands (e-mail: mark.stoopman@gmail.com, w.a.serdijn@tudelft.nl).

K. Philips is with IMEC-NL, Holst Centre, Eindhoven 5605 KN, The Netherlands (e-mail: kathleen.philips@imec-nl.nl).

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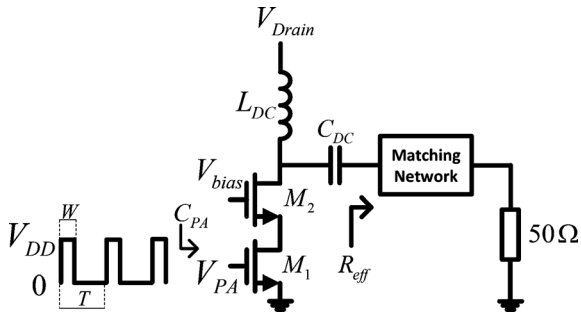

Fig. 2. CMOS tuned switching power amplifier with cascode transistor.

When assuming a high-Q matching network and sinusoidal drain voltage, the drain efficiency can be approximated by [9]

$$\text{Drain efficiency} = \frac{P_{RF\text{out}}}{P_{\text{PA,DC}}} \approx \frac{\sin(\pi d)}{\pi d} \frac{R_{\text{eff}}}{R_{\text{eff}} + R_{\text{on}}} \qquad (2)$$

where R_{eff} is the effective loading resistance and R_{on} is the combined channel resistance of M1 and M2. The drain efficiency can thus be increased by reducing the duty cycle, but this simultaneously reduces the maximum output power. For small duty cycles, the PA input pulse shape is distorted by the limited speed of the PA driver and therefore drives the PA switching transistor less strongly, or even below its threshold voltage. This effect can be reduced by increasing the PA driver transistor width, but this in turn decreases the global efficiency. There therefore exists an optimum duty cycle, depending on the relative transistor sizes of the PA and its driver.

The contribution of R_{on} becomes less significant when the output power decreases as $R_{\text{eff}} \approx V_{\text{DD}}^2/2P_{RF\text{out}}$. This relaxes the required size of M1 and M2 for <0 dBm output power, thereby reducing the input capacitance.

The impedance transformation to the 50 Ω antenna requires a high-Q matching network, which limits the drain efficiency due to the parasitic losses associated with practical components. Therefore, an off-chip matching network is utilized using high-Q inductors and capacitors. The drain inductor is selected to be self-resonant at the operating frequency to provide maximum impedance. The gate width of M1 is crucial to obtain a high global efficiency, as it involves a tradeoff between R_{on} and input capacitance C_{PA}. The gate width of M2 however can be increased without increasing C_{PA}, although it also adds parasitic capacitance to the output matching network. With this in mind, M1 and M2 are sized 14 and 28 μm wide with minimum length to reduce the effect of M2 on R_{on} with acceptable parasitic capacitance at the output. This corresponds to $R_{\text{on}} = 220\ \Omega$ and an input capacitance of only $C_{\text{PA}} = 18$ fF.

III. Duty Cycle Calibration Loop

The RF input duty cycle is set using the duty cycle calibration loop shown in Fig. 3. The PA driver consists of a cascade of tapered inverters, where the first inverter has an additional PMOS transistor that controls the inverter's rise time. The second and third inverter act as a comparator and provide sufficient gain to drive the PA transistor. The voltage at the PA input is sensed with a small inverter and is fed to an RC low pass filter to obtain the DC component, which is an indication

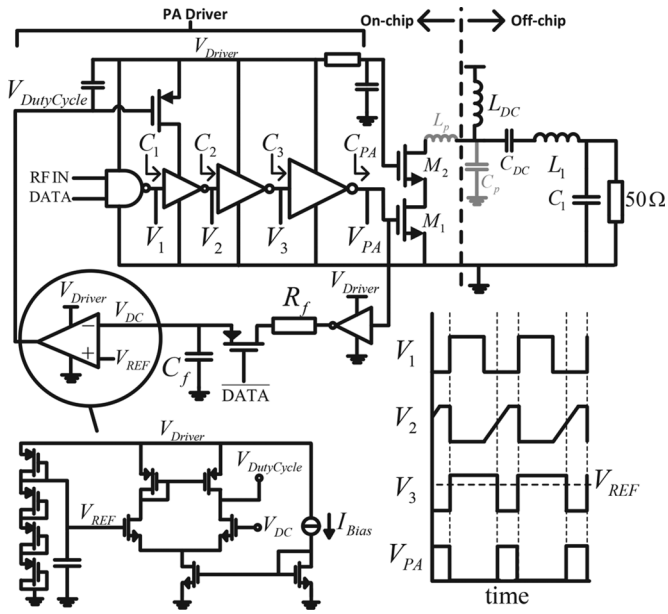

Fig. 3. Proposed PA and driver with on-chip duty cycle calibration loop.

for the duty cycle. Then, an NMOS differential pair compares the DC voltage to a reference voltage and subsequently controls the gate of the PMOS transistor. The reference voltage is set to $V_{\text{REF}} = 3/4V_{\text{DD,driver}}$ by means of four identical diode-connected PMOS transistors, resulting in 25% duty cycle at the PA input. The optimum duty cycle was found to be between 20% and 30%. Due to the negative feedback, the duty cycle is calibrated over PVT variations and therefore ensures robust operation.

The RF input is fed through a NAND gate which allows for On-Off Keying with near-zero power consumption during a logic '0' transmission (except for the opamp current $I_{\text{Opamp}} = 5\ \mu$A). A calibration memory is introduced by storing the loop control voltage on filter capacitor C_f during the OFF period in OOK modulation by means of a PMOS switch. This ensures fast start-up after a `0' → `1' transition and therefore allows for a high data rate.

The gate of the PA cascode transistor is decoupled with an on-chip capacitor and small filter resistor. The total post layout simulated gate capacitance of the PA and driver is 36 fF, resulting in 95 μW of switching power and 5.5 μW static power corresponding to the opamp power consumption.

IV. Experimental Results

The proposed PA is fabricated in TSMC 40 nm CMOS technology and is bondwired to a 14-lead QFN package. The layout area of the PA is $75 \times 75\ \mu\text{m}^2$ as illustrated in Fig. 4. After taking into account all parasitic components introduced by the pads, packaging and PCB (C_p and L_p), the matching network component values in Fig. 3 are given by $L_{\text{DC}} = 47$ nH, $L_1 = 3.9$ nH, $C_{\text{DC}} = 33$ pF and $C_1 = 2.4$ pF.

Fig. 5 shows the measured drain and global efficiency versus the PA drain voltage at 2.44 GHz. The drain efficiency shows a weak dependence on the drain voltage and decreases from 53.7% to 44.9%, which indicates slightly better matching at

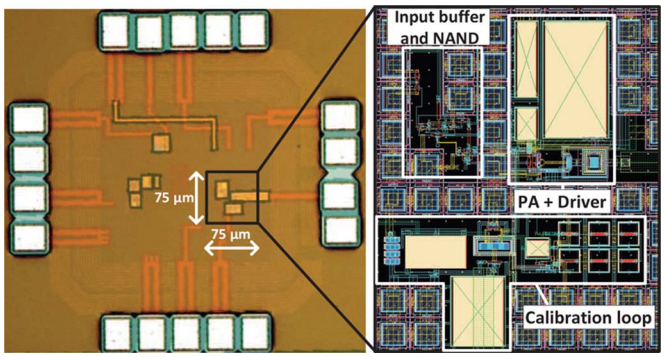

Fig. 4. Chip microphotograph and layout details.

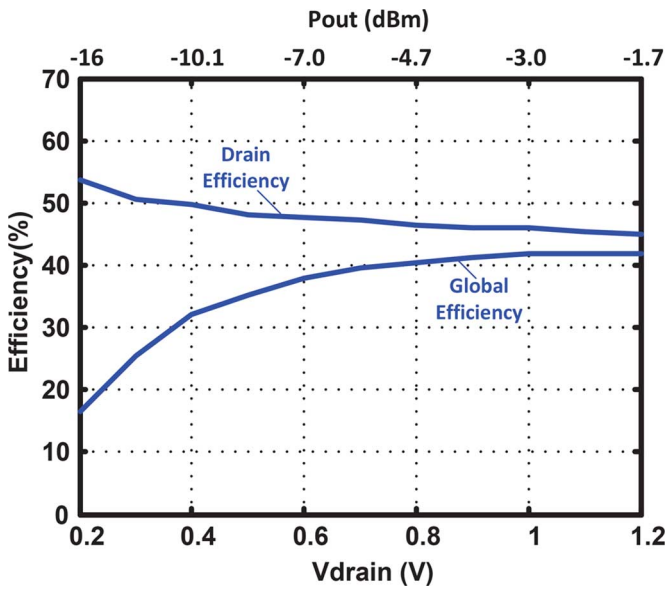

Fig. 5. Measured PA efficiency versus drain voltage (V driver $= 1.1$ V).

low drain voltage because of the smaller impedance transformation ratio. The global efficiency is 40% at -5 dBm and increases to 41.9% at -1.7 dBm, which compares favorably with other state-of-the-art PAs (Fig. 1). The measured power consumption of the PA driver including calibration loop is 115 μW from a 1.1 V supply. An output power variation of less than 0.25 dB is observed over the 2.4–2.48 GHz ISM frequency band. The second and third harmonic are respectively -51 dBc and -51.7 dBc.

A consecutive '0101' series is applied to the DATA input of the NAND gate to measure the OOK output in time and frequency domain. The transient waveform of a 40 Mbps OOK output is shown in Fig. 6. The 10–90% rise time is only 1.5 ns due to the fast start-up calibration memory of the loop, whereas the fall time is 3.3 ns. The measured average power consumption in this case is 646 μW at -2.84 dBm output power.

A performance comparison between state-of-the-art 2.4 GHz CMOS power amplifiers for low output power is given in Table I. The proposed PA shows the highest global efficiency for output power levels below 0 dBm. Also the data rate compares favorably due to the short rise and fall time. Furthermore, the die' area is significantly smaller than its competitors, but an external matching network is required.

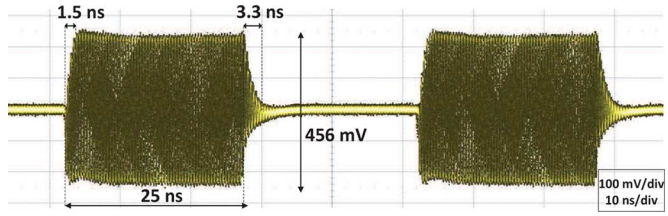

Fig. 6. Measured transient output of 40 Mbps OOK modulation.

TABLE I
PERFORMANCE COMPARISON OF 2.4 GHz CMOS POWER AMPLIFIERS

	This work	[3]	[4]	[5]	[6]	[8]
CMOS Process	40 nm	65 nm	90 nm	0.13 μm	65 nm	90 nm
P_{RFout} (dBm)	-5	-2.5	-12.5	-5.2	3	1.2
Drain efficiency (%)	45.4	40	-	-	47	39
GE/PAE (%)	40^{GE}	37.3^{GE}	14.7^{GE}	30^{GE}	40^{PAE}	32^{GE}
Modulation	OOK	OOK BPSK MSK	OOK	FSK	-	OOK
Data rate (Mbps)	40	1	5	-	-	10
Off-chip matching?	Yes	No	Yes	No	No	Yes
Die area (mm^2)	0.0056	0.324	-	-	0.18	0.055

GE: Global Efficiency, PAE: Power Added Efficiency

V. CONCLUSION

The design of a high-efficiency 2.4 GHz tuned switching PA has been presented to be used in low power WSN applications. The global efficiency is optimized by minimizing the capacitive switching losses of the PA driver and reducing the RF input duty cycle below 50% by means of a low power on-chip duty cycle calibration loop. The PA is implemented in 40 nm CMOS technology and supports OOK modulation. A global efficiency of 40% is achieved when delivering -5 dBm to a 50 Ω load. Due to the introduced memory in the duty cycle calibration loop, the rise and fall time are kept below 3.3 ns, making high data rate OOK modulation feasible.

REFERENCES

[1] K. Kim *et al.*, "A reconfigurable quad-band CMOS class E power amplifier for mobile and wireless applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 380–382, Jul. 2011.
[2] H. S. Oh *et al.*, "A power-efficient injection-locked class-E power amplifier for wireless sensor network," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 4, pp. 173–175, Apr. 2006.
[3] A. Paidimarri *et al.*, "A 2.4 GHz multi-channel FBAR-based transmitter with an integrated pulse-shaping power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1042–1054, Apr. 2013.
[4] G. Papotto *et al.*, "A 90-nm CMOS 5-Mbps crystal-less RF-powered transceiver for wireless sensor network nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 335–346, Feb. 2014.
[5] B. W. Cook *et al.*, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
[6] F. Jia *et al.*, "A digitally controlled PA with tunable matching network," *IEEE RFIT*, pp. 243–245, Nov. 21–23, 2012.
[7] M. M. El-Desouki *et al.*, "A fully integrated CMOS power amplifier using superharmonic injection-locking for short-range applications," *IEEE Sensors J.*, vol. 11, no. 9, pp. 2149–2158, Sep. 2011.
[8] X. Huang *et al.*, "A 0 dBm 10 Mbps 2.4 GHz ultra-low power ASK/OOK transmitter with digital pulse-shaping," in *Proc. IEEE RFIC Symp.*, May 23–25, 2010, pp. 263–266.
[9] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwell, MA, USA: Artech House, 2006, p. 178.