A Highly Linear, Sigma-Delta Based, Sub-Hz High-Pass Filtered ExG Readout System

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***Abstract*— Integrating time constants of the order of a few seconds is one of the main bottlenecks in the design of biomedical chips. To achieve a low cut-off frequency with 60 dB linearity, mixed-signal feedback utilizing the properties of a $\Sigma\Delta$ ADC is proposed. To verify the performance, a 10-bit $\Sigma\Delta$ modulator with the proposed technique is designed to be implemented in 0.18 μm CMOS AMS technology. The design is verified by means of simulations in Cadence using RF spectre.**

I. Introduction

There is a growing need to provide personalized and preventive healthcare solutions to reduce the burden on the existing infrastructure. This requires monitoring devices to be small and hence there is a need for fully integrated ExG solutions.

An important challenge in the design is integrating a large time-constant required for implementing the high-pass characteristic, needed to reject low frequency interference such as baseline wander. For example, for an electrocardiography (ECG) device, the high-pass cutoff frequency is usually specified to be < 1 Hz [1]. Moreover, a resolution of at least 10 bits is required to detect low amplitude signal variation [2].

Pseudo-resistors are widely used to integrate large time-constants [3], [4], [5]. However, they are inaccurate as their resistance is determined by leakage currents and they are also non-linear as the resistance depends on the voltage across them [6]. Since the cutoff frequency will vary with the momentary value of the input voltage, there will be distortion near the cutoff frequency, thereby limiting the resolution for frequencies in that region.

The switched capacitor technique can also been used for obtaining large time-constants. It is more accurate than pseudo-resistors. However, it will require high capacitor ratios and very low frequency clocks to achieve such a low cut-off frequency. Moreover, an anti-alias filter will also be needed which increases the overall system power [7].

Recently a mixed-signal feedback technique has been used to implement the high-pass characteristic [8], [9]. In this technique the signal is processed in the digital domain and fed back to the previous analog stage to achieve the required frequency characteristic. It utilizes the fact that in general, the objective of any front-end is to convert the physiological signal in to a digital one. Filtering can, in principle, be done in either the digital or the analog domain, as shown in Fig. 1. The choice for an analog or a digital filter would depend on the power budget and the DAC resolution. In [8] and [9] a 7-bit signal converted from a 8-bit one and a 1-bit signal converted from a 12-bit one, respectively, are used to obtain a low cut-off frequency. In both cases, similar to pseudo-resistors, the linearity of the signal near the cut-off frequency will be limited.

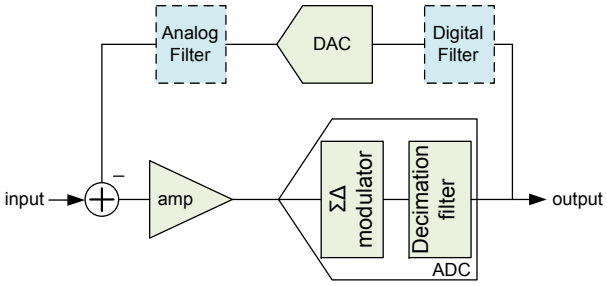

Fig. 1. Generalized block diagram for mixed-signal feedback technique. Output signal is fed back after decimation filter. Filtering can be done in analog or digital domain.

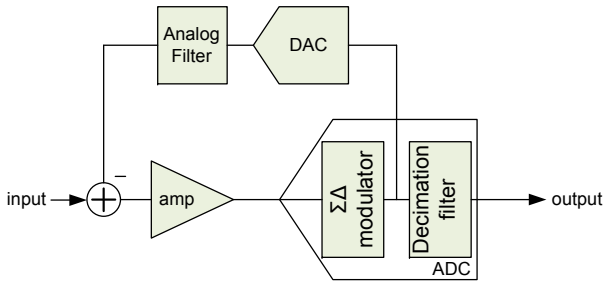

Fig. 2. Generalized block diagram for mixed-signal feedback technique. Signal is fed back after $\Sigma\Delta$ modulator. Filtering needs to be done in analog domain.

This paper proposes an ExG front-end with a 10-bit linear high-pass response using the mixed-signal feedback technique along with a $\Sigma\Delta$ ADC. Instead of feeding back the fully converted digital signal, the output of the $\Sigma\Delta$ modulator is fed back via a 1-bit DAC and an analog filter as shown in Fig. 2. Since a 1-bit DAC is inherently linear, the overall resolution and linearity depend on the oversampling ratio, the order of the $\Sigma\Delta$ modulator and the linearity of the filter in the feedback path, which can be designed to obtain the desired linearity.

The paper is organized as follows. In Section II the proposed $\Sigma\Delta$ architecture is discussed and the necessary transfer equations are derived. Section III presents a discussion on one of the possible circuit-level implementations of the system and corresponding non-ideal effects such as charge injection. The

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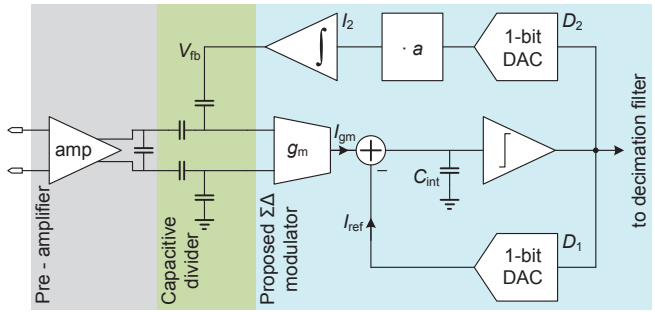

Fig. 3. System-level block diagram of the proposed technique.

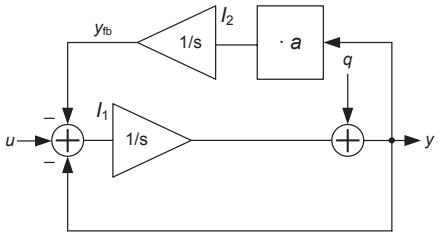

Fig. 4. Equivalent s-domain model of the ΣΔ modulator marked with the blue shadowed area in Fig. 3

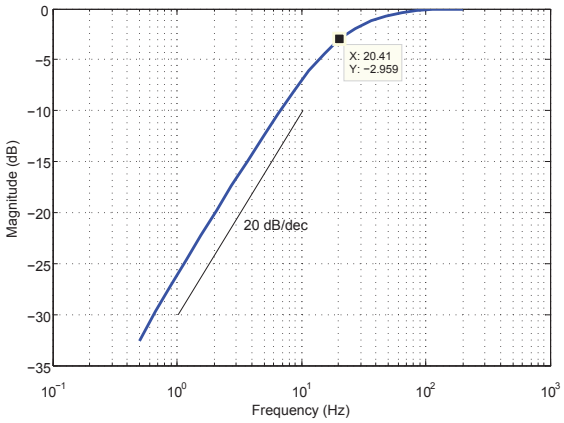

Fig. 5. Signal transfer function (STF) for f_s = 256 kHz, $a = 5 \cdot 10^{-4}$. f_{hpf} can be seen at 20 Hz.

circuit simulation results are shown in section IV. Finally, in section V, the conclusions are presented.

II. System-Level Design

Fig. 3 shows the proposed block diagram for an ExG system. It comprises a pre-amplifier followed by a capacitive divider and a ΣΔ modulator. The pre-amplifier is required to amplify weak biopotentials. The need for the capacitive divider will be discussed in the next section. A continuous-time ΣΔ modulator has been used to reduce power consumption since a sample-and-hold stage is not needed [10]. The ΣΔ modulator contains two feedback loops. The loop comprising integrating capacitor C_{int}, the comparator and the DAC D_1 forms a typical 1^{st} order modulator. A second feedback loop comprising DAC D_2, a scaling coefficient, a, and integrator I_2, has been added to implement the required high-pass characteristic. Since DAC D_2 has a 1-bit resolution, the feedback filter has to be implemented in the analog domain. The final digital signal is available after the decimation filter.

To discuss the proposed technique in more detail the equivalent linearised s-domain model as shown in Fig. 4 will be used. Herein, the output of the comparator, y, can be written as

$$y(s) = u(s) \cdot \frac{s}{s^2 + s + a} + q(s) \cdot \frac{s^2}{s^2 + s + a}, \qquad (1)$$

where u is the input signal and q is the quantization noise. Since this is just a conceptual model, g_{m} is not considered for now. In Section III it will be shown that the value of g_{m} will only scale the value of a.

From (1) it can be seen that the quantization noise, q, will be suppressed by 40 dB/dec for frequencies below f_{hpf} and by 20 dB/dec above it.

Furthermore, (1) shows that due to I_1 the signal transfer function (STF) has a zero at DC and two poles.

Since we are interested in the sub-Hz frequency range, the high pass cut-off frequency, f_{hpf}, is much smaller than the sampling frequency, f_{s}. Therefore, 's^2' can be neglected while calculating f_{hpf}. Thus f_{hpf} can be written as

$$f_{\text{hpf}} \approx \frac{f_{\text{s}} \cdot a}{2 \cdot \pi} \qquad (2)$$

From (2), it can be seen that f_{hpf} depends on f_{s} and scaling coefficient a.

As an example, Fig. 5 and Fig. 6 plot the signal and quantization-noise transfer functions respectively, for a system with an f_{hpf} at 20 Hz and f_{s} = 256 kHz. The required scaling coefficient, a, equals $5 \cdot 10^{-4}$. Both figures show that f_{hpf} is indeed located at 20 Hz.

The non-linearity and noise of I_2 and scaling stage will directly appear at the input of the modulator. The DAC does not contribute to the non-linearity since it has a single bit resolution, although it will contribute to the overall noise of the system. However, with proper design, as shown in the next section, it is possible to achieve a 10-bit resolution.

III. Circuit-Level Implementation

To discuss the circuit-level design issues, an ECG application with specifications as shown in Table I is assumed.

The front-end preamplifier (Fig. 3) is designed for a gain of 100. A high gain pre-amplifier is required to have a low input-referred noise. Techniques as those proposed in [3] have been used to design it.

Choosing a resolution of 12 bits, to meet 10 bits overall resolution, an oversampling ratio of 512 would be required for a 1^{st} order modulator [10], or in other words a sampling frequency of 256 kHz. The non-linearity of the g_{m} stage and charge injection from the switches will limit the ENOB. The rest of this section discusses the techniques employed to obtain the required linearity.

The non-linearity of the g_{m}-stage is dependent on the input and the output signal swing as it is implemented in open-loop configuration.

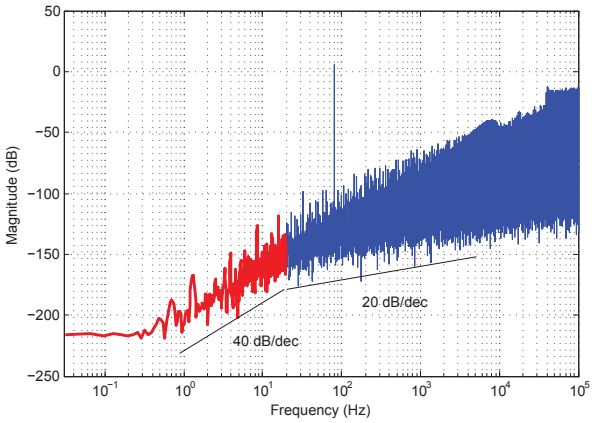

Fig. 6. Noise transfer function (NTF) for f_s = 256 kHz, $a = 5 \cdot 10^{-4}$. The transition from 40 dB/dec to 20 dB/dec is located at f_{hpf} = 20 Hz. The peak located at 101 Hz is the input signal.

TABLE I
ECG SYSTEM SPECIFICATIONS

Parameter	Specification
Input amplitude	1 mV
Bandwidth	1 Hz - 200 Hz
ADC resolution	10 bits
Supply voltage	1.5 V
Technology	0.18 μm CMOS

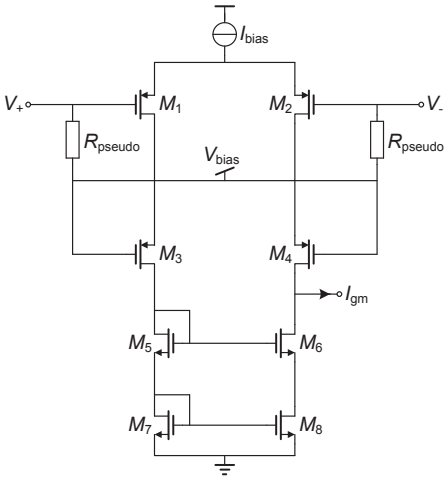

Fig. 7. Implementation of g_m stage

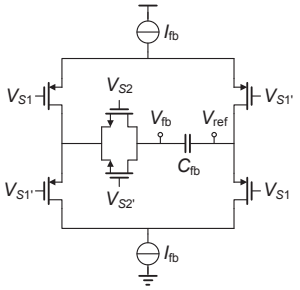

Fig. 8. Implementation of charge pump

To reduce the signal swing at its input, the g_m stage is brought outside the first loop formed by the comparator and DAC D_1, unlike in a conventional g_m-C $\Sigma\Delta$ architecture. A capacitive divider is needed to couple the voltage output of I_2 and the output of the preamplifier. It also functions to reduce the signal swing at the input of the g_m stage by 2.

The maximum output signal swing for the g_m stage can be written as

$$V_{\mathrm{int}} = \frac{I_{\mathrm{ref}}}{C_{\mathrm{int}} \cdot f_s}. \tag{3}$$

To obtain an amplitude of 20 mV, I_{ref} = 250 nA and C_{int} = 50 pF are chosen. A low reference current has been chosen to decrease the power consumption of the ADC. Decreasing it further would require decreasing the value of g_m which would require complicated g_m structures. A cascoded g_m structure has been used to further reduce the effect of the output signal swing. See Fig. 7. This structure also helps in reducing the effect of charge kick-back from the comparator.

A standard differential current DAC has been used to implement D_1. A differential topology is chosen to reduce the effect of charge injection.

For a cut-off frequency of 1 Hz and a sampling frequency of 256 kHz, scaling coefficient a will be $2.5 \cdot 10^{-5}$ according to (2). There are two possible ways to implement the scaling and integration function in the feedback loop. One is by performing scaling using a resistive divider and integration using a switched capacitor. Another is by utilizing a charge pump to implement the scaling and integration. A charge pump implementation is chosen since it has fewer components and therefore leads to a lower power consumption and an easier design for linearity.

The integrated voltage, V_{fb}, which is fed back, can be written as,

$$V_{\mathrm{fb}} = \sum \frac{\pm I_{\mathrm{fb}} \cdot t_{\mathrm{S2}}}{C_{\mathrm{fb}}}, \tag{4}$$

where t_{S2} is the time that switch S_2 remains on. V_{fb} should be such that

$$g_m \cdot \frac{V_{\mathrm{fb}}}{2} = a \cdot I_{\mathrm{ref}}. \tag{5}$$

The g_m block is designed for a value of 1.5 μS. Therefore, for obtaining $a = 2.5 \cdot 10^{-5}$, I_{fb} = 4 nA, C_{fb} = 40 pF and t_{S2} = 100 ns are chosen.

The linearity of the charge pump is mainly limited by the charge injection from the switches. Fig. 8 shows the implementation of the charge pump. A differential topology, similar to the 1-bit DAC, is used to reduce the effect of charge injection. S2' is used for the same reason. The switches are sized such that they cancel each others' charge injection. Although increasing I_{fb} helps to reduce the charge injection, I_{fb} needs to be small as otherwise the size of C_{fb} would be very large.

IV. Circuit Simulation Results

The Signal Transfer Function of the proposed system has been tested by applying signals with frequencies close to f_{hpf}.

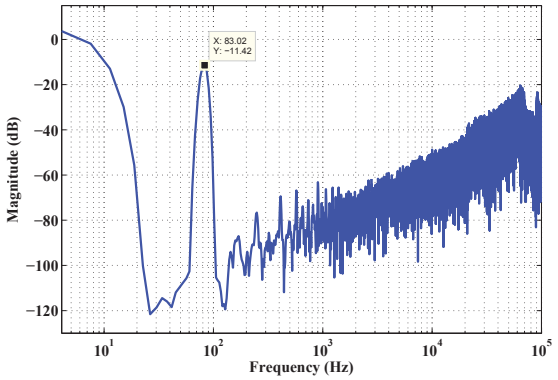

Fig. 9. FFT of the comparator output for $f_{\rm in} = 83.01$ Hz

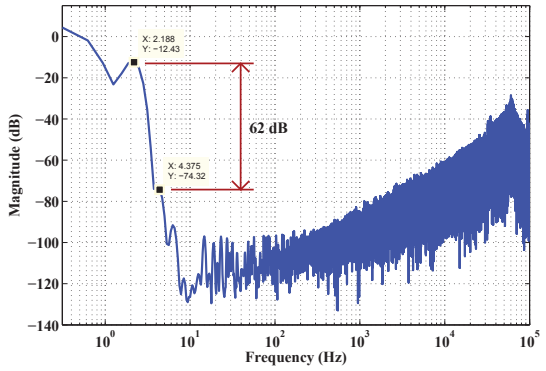

Fig. 10. FFT of the comparator output for $f_{\rm in} = 2.1$ Hz

As expected, the magnitude of the transfer is approximately 3 dB lower at 1 Hz than for frequencies higher than $f_{\rm hpf}$. Fig. 9 and Fig. 10 plot the frequency response of the output of the modulator for two input signal frequencies, 83.01 Hz and 2.1 Hz, each of 1 m$V_{\rm pp}$. $2^{\rm nd}$ and $3^{\rm rd}$ order distortion peaks are clearly higher in the 2.1 Hz frequency response. These originate from the non-linearity of the charge pump. However, they are more than 60 dB lower than the main signal component. These peaks are not seen in the 83.01 Hz frequency response, as the effect of the mixed-signal feedback loop is negligible at frequencies much higher than the cut-off frequency.

The accuracy of the cut-off frequency is dependent on the accuracy of the current references present in the charge pump. According to (4), the exact position of $f_{\rm hpf}$ mainly depends on the accuracy of the current source implementation in the charge pump (assuming that the error due to clock jitter is negligible and $g_{\rm m}$ and $C_{\rm fb}$ can be tuned). Current references in the nA current regime in 0.18 μm technology with temperature coefficients of 500 ppm/$^{\rm o}$C have been designed [11]. This would translate to an error of 4 % over a range of 0 - 80^{o}C, which is perfectly acceptable for most applications.

The power consumption of the mixed-signal feedback loop consists of the power consumed by the charge pump. It can be written as

$$P_{\rm fb} = V_{\rm dd} \cdot I_{\rm fb} = 9.7 \text{ nW}. \quad (6)$$

Thus the mixed-signal feedback is responsible for only a negligible increase in power consumption. The clock power is not considered as it is in any case needed for the rest of the system as well.

V. Conclusion

A mixed-signal feedback technique utilizing the properties of a $\Sigma\Delta$ modulator has been proposed to improve the linearity of the transfer at sub-Hz cut-off frequencies. A 10-bit $\Sigma\Delta$ modulator has been designed using this technique.

To implement the required high-pass transfer with maximum resolution and linearity, the output of the modulator, instead of the output of the decimation filter, is fed back. Since the decimation filter is left out from the loop, its noise will not appear at the input and affect the achievable resolution.

The distortion components are more than 60 dB lower than the main signal component. There has been no significant amount of increase in power consumption.

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