A Robust and Large Range Optimally Mismatched RF Energy Harvester with Resonance Control Loop

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***Abstract*—This paper presents the design of a robust and large range RF energy harvester with a control loop. The harvester is based on an optimally mismatched antenna-rectifier interface that offers a large passive voltage boost to increase the sensitivity of the energy harvester while still extracting energy from the antenna. A control loop is proposed that maximizes the voltage on the storage capacitor by keeping the rectifier at resonance during charging continuously. The basic principle of this loop has been implemented and verified with simulations. The loop is able to optimize the antenna-electronics interface for a $\pm$33% change in antenna reactance. A comparison with state-of-the-art RF energy harvesters shows major improvements in rectified output voltage at power levels lower than -25 dBm.**

I. Introduction

The interest in RF energy harvesting to power up a low-duty-cycled wireless sensor or active RFID (Radio Frequency Identification) tag has increased significantly the last few years since it offers a wide range of applications. Warehouse inventory management is a typical application that can benefit from RFID tags with an RF energy harvester to locate and track products. In these applications, devices can for example harvest for 99% of the time while the radio is in stand-by mode and use all stored energy for transmission at once.

These devices should be small, low cost and must cover a wireless range of several meters. Furthermore, it should maintain good performance when the environment of the device is changed. This is a challenging task since antenna characteristics such as impedance and radiation pattern can be very dependent on the surrounding environment.

In this paper we will investigate how the wireless range and robustness of RF energy harvesting circuits can be improved. A system overview is given in Section II, followed by an antenna-rectifier interface analysis that leads to the conclusion that an optimally *mismatched* interface should be used instead of the conventional conjugate matched interface. The circuit design of a rectifier and its control loop is discussed in Section IV and verified with simulation results in Section V. Finally, this paper ends with the conclusions.

II. RF Energy Harvesting

Figure 1 shows our proposed RF energy harvesting system. An antenna converts the electromagnetic energy of a (dedicated) RF source into electrical energy. A feedback controlled voltage boosting and tuning network increases the voltage to improve sensitivity and robustness of the RF rectifier. A voltage monitor determines when enough energy is stored in the off-chip capacitor. The main circuit is then connected and discharges the capacitor until the minimum voltage to activate the control loop is reached. This guarantees that the control loop can always be activated once the voltage on the capacitor has reached Vmin after the very first charging phase. The rectifier thus has a purely capacitive load during harvesting.

In this work we aim at a frequency band between 800MHz and 960MHz, which will cover most world-wide frequency Industrial, Scientific and Medical (ISM) bands and also offers more advantages compared to the 2.45 GHz band in terms of regulations, allowed power level and maximum range [1].

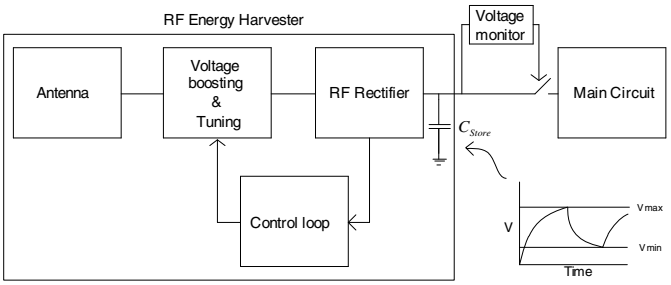

Figure 1. System overview of proposed energy harvesting principle

Wireless range limitations: The maximum wireless range of an RF energy harvester is determined by the rectifier turn-on voltage and the available input voltage. The turn-on voltage is related to the transistor threshold voltage and the implementation of the rectifier. The turn-on voltage can for example be decreased by using (near) zero V_{TH} transistors, but this is usually not a low-cost solution. Gate pre-biasing or trapping charge in floating-gate transistors is another effective concept to increase the wireless range [2], but this often requires external bias voltages and calibration, which makes it impractical and too expensive. An alternative V_{TH} self-cancellation scheme is reported in [3]. This low-cost rectifier shows good performance at low power levels, making it an interesting solution to increase the wireless range.

Another way to improve the wireless range is to increase the available input voltage by passively boosting the voltage with a high-Q resonating network. This can be realized by combining the inductive behavior of a high-Q loop antenna with the capacitive input impedance of the rectifier. This is a very attractive concept since it can offer a significant improvement in wireless range. The disadvantage is that high-Q networks are very sensitive to small impedance variations.

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These variations can be the result of process mismatch, input power level or environment changes. A robust RF energy harvester therefore requires a control loop that compensates for these effects.

III. Antenna-rectifier interface

The design of an RF energy harvester very often starts with the requirement of a conjugate matched interface without any further discussion. In this section we will investigate if this starting point can be justified. First the conventional conjugate matched interface will be discussed. Then, we analyze the proposed optimally mismatched interface. In both cases we assume a lossless and perfectly matched matching network and a rectifier with a capacitive load.

A. Conjugate matched interface

Consider the conjugate matched antenna-rectifier interface in Figure 2. The antenna model consists of a reactive part L_A that represents the energy stored in the near field of the antenna and a resistive part R_A that represents the radiation and loss resistance. The voltage induced by the electric field is represented by the Thévenin equivalent source V_A which is given by [5]

$$V_A = \sqrt{R_A G_A P_{EIRP}}\frac{\lambda}{2\pi r}\cos\theta \tag{1}$$

where G_A is the antenna directional gain, P_{EIRP} is the Equivalent Isotropic Radiated Power, λ is the wavelength, r is the range and θ is the angle of misalignment of the electrical field to the incoming wave with the antenna. In the remainder of this paper, we will assume a perfectly aligned antenna, i.e., $\theta = 0$.

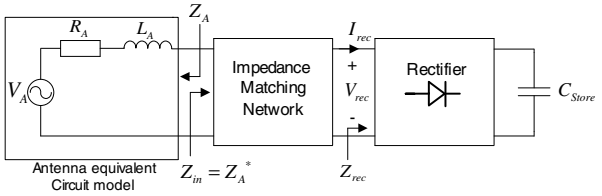

Figure 2. Conjugate matched antenna-rectifier interface

An impedance matching network transforms the impedance seen from the antenna such that the conjugate matching condition $Z_{in} = Z_A^*$ is obtained. We model the rectifier input impedance as a parallel combination of $R_{rec}//C_{rec}$. Furthermore, it is desired to simultaneously maximize the voltage at the rectifier input. The passive voltage boost for *any* conjugate matched interface is given by

$$G_{V,boost} = \left|\frac{V_{rec}}{V_A}\right| = \frac{1}{2}\sqrt{\frac{R_{rec}}{R_A}} \tag{2}$$

Note that $G_{V,boost}$ is independent of the matching network implementation. When we substitute Equation (2) into (1) we obtain

$$V_{rec} = \sqrt{R_{rec} G_A P_{EIRP}}\frac{\lambda}{4\pi r} \tag{3}$$

Intuitively, this makes sense; for a given antenna, power level, wavelength and range, the input voltage of the rectifier V_{rec} can *only* be increased by increasing R_{rec}. Hence, for an interface with a given source and load resistance, one *cannot* design for a desired voltage boost to increase wireless range if a conjugate match is required simultaneously.

B. Optimally mismatched interface

By intuitive reasoning one can conclude that adding resistance to an RF energy harvester to improve performance is fundamentally incorrect. Yet, it seems that this is exactly what is done in conjugate matching.

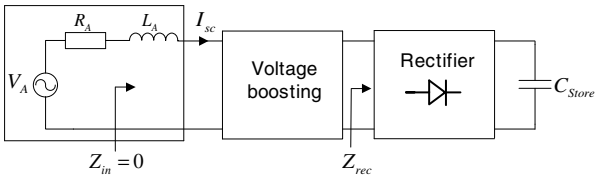

Figure 3. Optimally mismatched antenna-rectifier interface

First we note that the rectifier has a purely capacitive load during rectification. We therefore must maximize the charging current to charge this capacitor as fast and as efficient as possible. The maximum current that can be obtained is the antenna short-circuit current $I_{sc} = V_A/R_A$. This can be realized when the input impedance seen from the antenna resistance equals zero. If $\Re\{Z_{rec}\} \ll \Re\{Z_A\}$, we only have to bring the rectifier in resonance with L_A to obtain $Z_{in} \cong 0\,\Omega$. This means that the antenna should be mismatched! This conclusion can be confusing. After all, if the interface power efficiency is calculated using $\eta = 1 - |\Gamma|^2$, for $\Gamma = (Z_{rec} - Z_A^*)/(Z_{rec} + Z_A)$, $Z_{rec} = -jX$ and $Z_A = R_A + jX$, we come to the conclusion that $\eta = 0$. Apparently, no energy can be extracted from the antenna and stored in the capacitor. This is true for a purely capacitive load; energy is transferred back and forth between the capacitor and the antenna, causing the capacitor to be charged *and* discharged each cycle.

However, the antenna load in this interface is not just a capacitor, but a *rectifier* with capacitive input impedance. At resonance, the short-circuit antenna current flowing through the inductance causes a large boosted voltage that switches on the rectifier. The rectifier in essence flips the voltage and current polarity of the storage capacitor in each cycle and prevents the capacitor from discharging such that the charge on the capacitor can build up.

If the condition $Z_{in} = 0\,\Omega$ is satisfied, we can write the passive voltage boost in this interface as

$$G_{V,boost} = \left|\frac{V_{rec}}{V_A}\right| = \frac{\omega L}{R_A} \tag{4}$$

When combining Equation (1) and (4), we find

$$V_{rec} = \omega L\sqrt{\frac{G_A P_{EIRP}}{R_A}}\frac{\lambda}{2\pi r} \tag{5}$$

This equation shows that V_{rec} can be increased by choosing a small radiation resistance R_A or a large inductance L. Hence, we gained one extra degree of freedom since we only have to match the reactance in contrast to the conjugate matched interface which also requires resistance matching. The required

voltage boost can be set with L while the resonance frequency can for example be set with a parallel capacitor in the voltage boosting network.

IV. Circuit Design

In this section we will discuss the design of the rectifier and control loop that is based on the optimally mismatched interface topology. Also the requirements of the antenna will be discussed.

A. RF Rectifier

In the previous section it was concluded that the proposed optimally mismatched interface topology requires a rectifier with negligible $\Re\{Z_{rec}\}$ such that the reactance dominates the rectifier input impedance. The rectifier shown in Figure 4 meets this requirement.

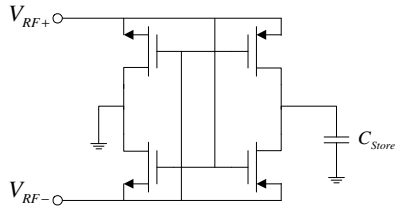

Figure 4. Rectifier circuit implementation with V_{TH} self-cancellation [3]

The input impedance is dominated by the rectifier's parasitic capacitance for $C_{store} \gg C_{par}$. The transistors are sized for maximum efficiency and minimum $\Re\{Z_{rec}\}$. The output voltage can be increased by adding more stages.

B. Control loop

The design goal of the control loop is to maximize the voltage on C_{store} during charging. This can be achieved by a feedback controlled tuning network that tries to maximize the slope of V_{Store} by adjusting the voltage boosting & tuning network. A possible control loop implementation in combination with a multi-stage rectifier is shown in Figure 5.

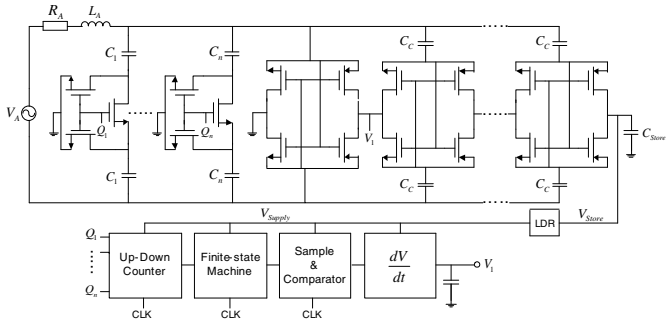

Figure 5. Multi-stage RF energy harvester with control loop

The feedback loop measures the voltage V_1 rather than V_{Store} since V_{Store} is a function of input power and C_{store}. Since C_{store} can be very large (>nF), this results in a very long charging time and small V_{Store} during start-up. If V_1 is used as input, the dependence on C_{store} is eliminated and the input voltage of the control loop during start-up is increased.

The slope information is obtained using a differentiating network. A sample & comparator stage compares the slope information of V_1 with the previous sample and determines if the slope has increased or decreased. This information is fed to a finite-state machine that determines if the up-down counter should keep counting or change count direction. The output of the n-bit up-down counter is used to control a capacitor bank. Each switch in the capacitor bank is implemented with one main switching transistors and two small bias transistors to maximize the Q-factor. The desired tuning range and accuracy can be set with the number of bits. A low-dropout regulator (LDR) offers a stable supply voltage for the control loop.

The up-down counter, finite-state machine and differentiator all have been implemented at circuit level and have a negligible power consumption compared to the harvested power. The clock generator, LDR and sample & comparator are not implemented yet and are simulated using ideal components. It is expected that these stages can also be designed with negligible power consumption. The required accuracy of the clock generator is low and it only needs to oscillate in the kHz range since the charging time of the rectifier is expected to be in the msec range. Likewise, the required bandwidth of the sample & comparator stage is also in the kHz range.

C. Antenna requirements

Our proposed RF energy harvester makes use of the high-Q properties of a small loop antenna. The antenna impedance accuracy is not very critical since the control loop will correct for impedance variations. To obtain a large voltage boost we aim for an inductive reactance around $X_A = 700\,\Omega$ at 900 MHz. The antenna resistance needs to be as low as possible while still maintaining an efficient antenna. In this work we assume that $10\,\Omega \leq R_A \leq 20\,\Omega$. An antenna with these flexible design specifications is considered to be practical. For example, an antenna with similar properties is proposed in [8].

The chip will be mounted directly on the antenna so that the physical length between antenna and rectifier is much smaller than the wavelength. The propagation effects can therefore be neglected since the voltage and current along the wire can be assumed constant.

V. Simulation results

A 4-stage RF energy harvester with 7-bit control loop is implemented in TSMC 90nm RF CMOS technology and is verified using Cadence RF Spectre. The tuning capacitors, main switching transisors and switch biasing transistors are binary scaled from 4-256 fF, 2.5-160 μm and 0.12-7.7 μm respectively. All rectifying transistors have a width of 6 μm for nMOS and 18 μm for pMOS. All transistors have minimum length. Furthermore we set $C_c = 1\,pF$, $L_A = 120$ nH and $R_A = 10\,\Omega$.

Furthermore we set $C_{store} = 10$ pF and $f_{CLK} = 2$ MHz. Note that these two values are only used to reduce simulation time. In reality, C_{store} is in the nF range and f_{CLK} in the kHz range, but these realistic values result in a very long and impractical simulation time. The rectifier performance does not change for a longer charging time.

The LDR is modelled with an ideal voltage source of 700 mV. Simulations showed that the average power supplied by this source is approximately 400 nW. Note that this will be reduced significantly when the clock frequency is reduced from 2 MHz to 2 kHz due to the dynamic power consumption of $P = C_{load} f_{CLK} V_{DD}^2$ for each inverter.

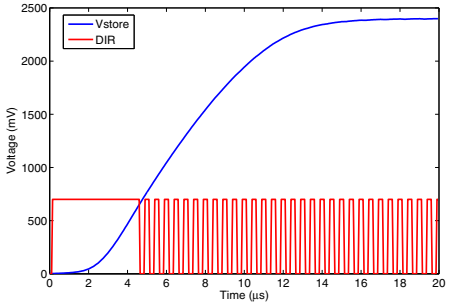

Figure 6. V_{store} and 'DIR', $P_{in} = -20\,dBm$, $L_A = 120\,nH$

The simulated output voltage for $P_{in} = -20\,dBm$ is shown in Figure 6. The binary signal 'DIR' is the output signal of the finite-state machine that controls the up-down count direction. The control loop keeps counting up or down (depending on the initial direction) as long as the slope of V_{store} keeps increasing. The slope decreases when the capacitor bank has passed the optimum capacitance. In this case, 'DIR' turns from '1' to '0' and the loop inverts the counting direction.

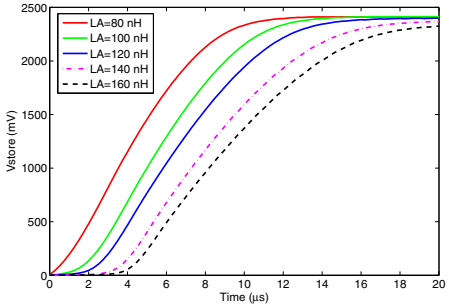

Figure 7. V_{store} for variations in L_A, $P_{in} = -20\,dBm$

The robustness is verified by varying the antenna inductance between $80\,nH \leq L_A \leq 160\,nH$ to simulate antenna environment changes. Figure 7 demonstrate that this RF energy harvester is able to cope with these large variations despite the high-Q antenna network. The control loop is able to maximize V_{Store} in each scenario.

A comparison with state-of-the-art RF energy harvesters over a wide range of input power levels is depicted in Figure 8. All rectifiers are designed for 900 MHz and we compared the unloaded (or highest reported resistive load) performance in each paper. Our proposed RF harvester shows excellent performance over the entire power level range. Especially at low input power levels (<-25 dBm) it outperforms other designs. It even outperforms the design of [2], which uses a 36 stage rectifier with floating gate transistors that need to be calibrated. Our 4-stage rectifier is implemented with standard CMOS transistors ($V_{TH} \cong 450\,mV$) and doesn't require any calibration.

Some rectifiers perform better at -25 dBm or higher since our proposed rectifier suffers from large reverse current leakage at high input power levels. This is caused by the large common-mode gate voltage that prevents the rectifying transistors from switching off entirely. If this reverse current can be reduced, it is expected that the performance can be increased even further for high power levels.

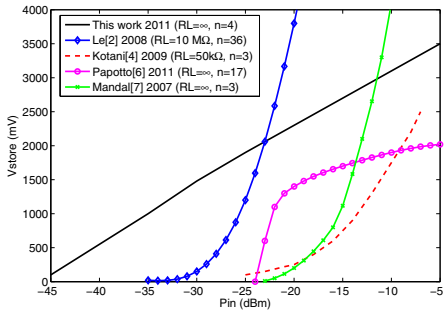

Figure 8. Performance comparison with state-of-the-art RF energy harvesters. The number of stages is indicated by 'n'.

VI. Conclusions

An optimally mismatched antenna-rectifier interface has been proposed. It has been shown that energy can still be extracted from a completely mismatched antenna. A large passive voltage boost is obtained by using a high-Q loop antenna to reduce the effective rectifier turn-on voltage.

A 4-stage RF energy harvesting circuit is designed in standard TSMC 90nm RF CMOS technology and verified using Cadence RF Spectre. The basic principle of a 7-bit control loop has been implemented. The loop is able to optimize the antenna-electronics interface for a $\pm 33\%$ change in antenna reactance. The control loop power consumption is negligible compared to the harvested power since the loop is mainly digital and the required bandwidth is very small.

A comparison with state-of-the-art RF energy harvesters shows major improvements in rectified output voltage at power levels lower than -25 dBm.

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