A Continuous-Time Level-Crossing ADC with 1-Bit DAC and 3-Input Comparator

Yongjia Li* and Wouter A. Serdijn†
Biomedical Electronics Group, Electronics Research Laboratory
Delft University of Technology, the Netherlands
*y.li-1@tudelft.nl, †w.a.serdijn@tudelft.nl

***Abstract* — A novel continuous-time level-crossing analog-to-digital converter (LC-ADC) for biomedical application is proposed. Lower power consumption and less design complexity with respect to the conventional designs are achieved due to 1) replacing the n-bit digital-to-analog converter (DAC) with a 1-bit DAC; 2) introducing a 3-input comparator and switching off the idle branches in the following stages when possible; 3) utilizing the opposite polarity of the differential input signals and fixing the comparison window with only one reference level; 4) splitting the level-crossing detections. Designed to be implemented in 0.18 µm CMOS technology, the proposed ADC achieves 8 bits of resolution with much lower power consumption than conventional LC-ADCs.**

I. INTRODUCTION

ADCs are widely used in wearable and implantable biomedical data acquisition systems. There is a growing demand to integrate wearable health monitoring systems into telemedicine systems, which makes early detection of abnormal conditions from patient possible [1]. In such systems, the power consumed from the wireless transmission usually dominates and is proportional to the overall data rate. Nevertheless, many bio-signals are sparse in the time domain, comprising both long periods of low frequency content and short periods of high frequency information. In this case, uniform sampling constantly generates the samples from the sensed signal, resulting in a waste of system energy. Conventional ADCs are based on the uniform sampling mechanism, with the sampling frequency determined by the highest expected spectral frequency. From a system point of view, they are less power-efficient for sparse signal recording as the conversion is triggered by the sampling clock periodically regardless of input signal variations.

A promising alternative ADC for biomedical data acquisition is based on so called level-crossing sampling, which results in non-uniform sampling. Samples are generated by the signal crossings of the threshold levels, while the time in between two consecutive samples is measured by a timer. Its advantages are well stated in [2]-[7]. For example, low-frequency and low-amplitude inputs are sampled less densely in time than high-frequency and high-amplitude inputs, no aliasing occurs, etc. Hence, a much lower average sampling rate is achievable for biomedical applications. Furthermore, in LC-ADCs, magnitude quantization shifts to time quantization, which can be more precise when using advanced technology and lower power supply voltage.

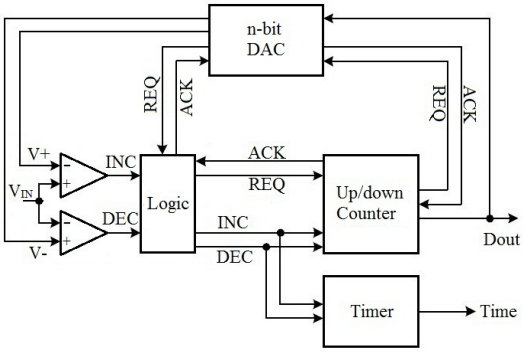

Fig. 1 Block diagram of a conventional LC-ADC

A few LC-ADCs have been reported in recent years [3]-[6]. They usually consist of two comparators, an n-bit DAC, an up/down counter, a timer and control logic, as is shown in Fig. 1. But they are still not mature in comparison with their uniform sampling counterparts such as successive-approximation register (SAR) ADCs. Basically, most of the power is consumed by the n-bit DAC and comparators. This is due to that: 1) an n-bit DAC is realized by either resistor strings or capacitor arrays with opamps; 2) in order to guarantee the required short decision time when the input signal moves in between the full-scale input range, the comparators with adequate performance usually consume a lot of power as comparators adopted in the LC-ADCs are usually comprised of cascades of continuous-time amplifiers.

To solve the above problems, a novel way of detecting the level-crossings at system level and new structures of the DAC and the comparators at circuit level are proposed, respectively. The power consumption of the LC-ADC is thus reduced dramatically. More details of the proposed LC-ADC are discussed in the following sections.

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II. SYSTEM STRUCTURE OF LC-ADC

A. Discussion on architecture of conventional LC-ADC

The operation of a conventional LC-ADC was summarized in [3]-[7]. As is shown in Fig. 1, as long as the input signal is in between the two levels (V+, V-), the outputs of both comparators are low and no sample is generated. Once the input signal moves outside this range, one of the comparators will detect the level crossing, outputs a logic "1" on INC (increment) or DEC (decrement) and a conversion is triggered. The up/down counter then outputs the previous digital code and increases (or decreases) by 1. Meanwhile, the timer outputs the duration of the previous sample, then resets and starts to count for the next sample. The DAC converts the new digital code from the up/down counter to analog voltages, which set newly refreshed levels to track the input. Conventional LC-ADCs, however, suffer from the following drawbacks.

Firstly, the up/down counter outputs the digital codes, which are then converted by the n-bit DAC to analog voltages to track the input voltage. Apparently, it is not that power-efficient to use an n-bit DAC to convey the delta information of only 1 LSB each time.

Secondly, two identical comparators are used in order to obtain a comparison window with upper and lower levels. Considering the number of comparators' inputs, one input should be for the input signal and two inputs should be for the two reference levels, so three inputs in total are enough to detect crossings of the upper and lower levels.

Thirdly, the output voltages of the DAC track the input voltage over the full-scale range, which means the input operating common-mode voltage of the comparators varies a lot. Even when the two reference levels are fixed as in [6], the operating comparison levels for the upper and lower comparator are still different. Therefore, input common-mode related offsets generate different time offsets and hence distortion.

Fourth, when the input signal is close to a level and moves up and down around the level a lot, the output of the comparator will toggle a lot as well. Corresponding conversion will thus be triggered, consuming lots of energy.

To mitigate the above shortcomings, we propose: 1) a 1 bit DAC, only converting delta information of 1 LSB; 2) a 3-input comparator, cutting off the idle branches when possible; 3) to utilize the opposite polarities of the differential input signal to do the comparison; 4) to split the level-crossing detection into two parts.

B. Architecture of proposed LC-ADC

The system structure of the proposed LC-ADC is shown in Fig. 2 (a). The 1-bit DAC tracks the input differential signals V_{IP} and V_{IN}, performs subtraction or addition on the tracked differential inputs when there is a level crossing, and outputs two single-ended signals V_{OP} and V_{ON}. They are then applied to the comparator inputs, since V_{OP} and V_{ON} are always with opposite polarity, so one fixed reference voltage level instead of two is able to detect level crossings from up or down directions. The input common-mode voltage of the comparator is thus fixed to V_{REF}.

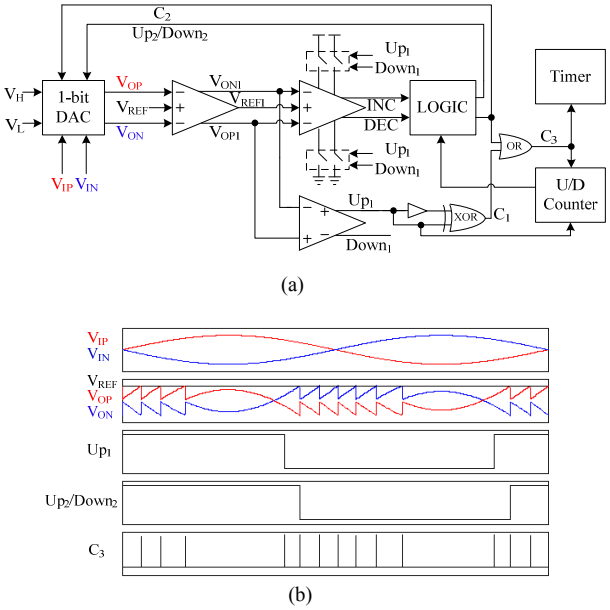

Fig. 2 (a) Proposed LC-ADC (b)Example waveforms

The 1-bit DAC injects a ± 0.5 LSB voltage offsets to the tracked signals after each level crossing, and V_{OP} and V_{ON} will be set to a level that is 0.5 LSB lower than V_{REF} after injection. For example, when the input signal increases, V_{OP} and V_{ON} will move up and down, respectively. Once V_{OP} becomes higher than V_{REF}, a -0.5 LSB and a +0.5 LSB offset will be added to V_{OP} and V_{ON}, respectively, setting them both at a level that is 0.5 LSB lower than V_{REF}. A similar situation applies when the input signal goes down. This mechanism goes on throughout the whole conversion. See Fig. 2 (b).

The information of increment and decrement is converted into "C_X" and "Up_X/$Down_X$". "C_X" is the level crossing information while "Up_X/$Down_X$" indicates the direction of the level crossing. The detection of level crossings is different from previous works. It is split into two parts, namely, detection of consecutive crossing and transition crossing. Here, two comparators with different structures sharing the same input stage are employed. The upper one is responsible for detecting consecutive level crossings when the signal keeps increasing (or decreasing) while the lower one is only for detecting the first level crossing after the signal changes its direction. In other words, V_{OP} (or V_{ON}) is compared with V_{REF} by the upper comparator, while it is compared with the other signal V_{ON} (or V_{OP}) by the lower comparator. So the situation that V_{OP} and V_{ON} cross each other indicates the first level crossing after the signal changes its direction.

So there are two groups of information for level crossing and its direction, namely, "C_1, Up_1/$Down_1$" and "C_2, Up_2/$Down_2$". Up_1/$Down_1$ always lags behind Up_2/$Down_2$. C_3 is the logic OR of C_1 and C_2. Note that C_1 and C_2 can never be generated simultaneously. When V_{OP} (or V_{ON}) crosses V_{REF}, a pulse "C_2" will be generated by the LOGIC, which will trigger both the DAC and up/down counter to work. When V_{OP} and V_{ON} cross each other, the outputs of the lower comparator will toggle, and a pulse "C_1" will be generated by the XOR gate, only the up/down counter will be trigger.

Suppose that the input signal begins to move up and down around a level a lot, V_{OP} and V_{ON} will cross each other a lot, but only the up/down counter will be triggered, the possible power consumption is thus minimized.

III. CIRCUIT BLOCKS

A. Control logic

The LOGIC block is the same as the one in [3]. Basically, it translates the upper comparator outputs of INC and DEC to C_2 and $Up_2/Down_2$, which then control the conversion of the DAC and up/down counter. The additional control signals are C1, C3, Up1/Down1 and they can be represented by:

$$C_1 = Up_1 \oplus Up_{1\_delay} \quad (1)$$

$$C_3 = C_1 + C_2 \quad (2)$$

B. 1-bit DAC

The main requirement of the DAC for the proposed system is injecting the offset voltage without affecting tracking the continuous-time input. The proposed 1-bit DAC is able to do so and is shown in Fig. 3(a). The upper capacitor array for V_{IP} is identical to the lower one for V_{IN} except for switches connecting to V_H and V_L. The waveform in Fig. 3(b) depicts how the DAC works. There are two identical branches in each capacitor array, the right one is for tracking the input while the left one is for offset injection (OI). Two capacitors in each branch are connected in series in order to achieve an AC-coupled input and share charge without affecting the input. nMOS transistors are utilized as switches.

For the sake of clarity, we only discuss the upper capacitor array for V_{IP}, it works as follows: assuming V_{IP} increases, V_{OP} will increase until it crosses a level. As a consequence, "$Up_2/Down_2$" becomes logic high, a "C_2" pulse is generated and converted to Φ_1-Φ_3 to control the charge sharing process to inject negative offset to the capacitor arrays. As is shown in Fig. 3(b), S_1 is switched off first to disconnect the OI branch from the tracking branch while the latter one still keeps tracking the input. All the voltage variations during that period are stored on tracking branch. S_2 is then switched on to connect the OI branch to V_L to discharge. After a short while (depending on the settling time) S_2 is switched off and the two branches are reconnected by switching on S_1. V_{OP} are then decreased by 0.5 LSB by charge sharing. The charging process is similar to the discharging process, but uses S_3 instead to charge OI branch to V_H.

Φ_1 and Φ_2 (Φ_3) are non-overlapping to avoid directly connecting the tracking branch to the voltage reference V_H or V_L. C_D is the unit capacitor while C_U is 10 times larger, so that 10/11 of the input variation falls on the upper plate of C_D.

The advantages of the proposed 1-bit DAC include: 1) the input voltage range is not limited, as the tracked input voltage is shifted up or down within the input dynamic range as soon as it reaches the fixed level. In other words, the input signal swing can be higher than in conventional structures; 2) there is no information loss during offset injection, unlike the scheme proposed in [6]; 3) the power consumption of the capacitor array is much lower than the conventional structure, as the delta voltage step of only 0.5 LSB per conversion is required and voltage reference can be very low.

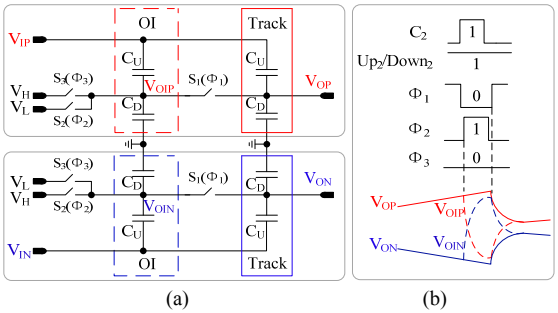

Fig. 3 (a) the 1-bit DAC (b) Waveform

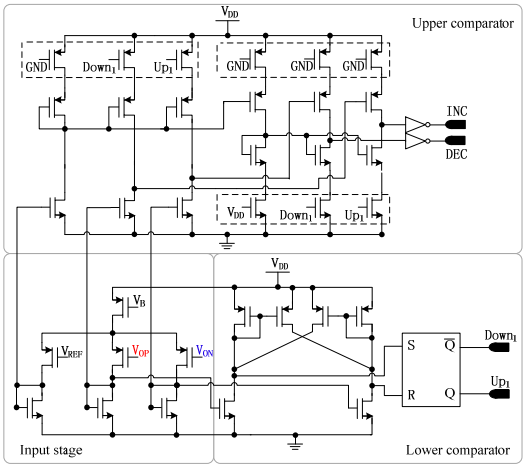

Fig. 4 Schematic of the comparators

C. Comparator

The proposed continuous-time comparators are shown in Fig. 4. The input stage comprises 3 PMOS inputs loaded by nMOS diodes. The MOSFETs inside the dashed boxes are either switches to cut off the idle branches or dummy switches to guarantee a better matching of the current mirrors. Although the upper and lower comparators share the first input stage, the structures of the following stages are totally different because of different systematic requirements.

From the upper comparator side, only one of the differential inputs is compared with V_{REF} to detect level crossings while the other one is idle, so it is possible to shut down the branches that are not in use. The following stages based on current mirrors with two outputs are thus adopted. The switches are controlled by the output of the lower comparator as differential inputs V_{OP} and V_{ON} are compared with each other to determine which one is closer to V_{REF}. Since it is much easier for lower comparator to make a decision, a second stage with internal positive feedback and differential output is used, followed by a SR trigger to increase gain and allow the output swing to reach rail-to-rail. Hysteresis is introduced in order to ensure noise robustness. To minimize the time offset, a maximum delay that is smaller than the resolution of the timer must be guaranteed.

IV. SIMULATION RESULTS

Simulations using AMS 0.18µm CMOS technology have been carried out. All the circuits operate from a 0.7V supply. The up/down counter and timer are realized by verilogA, so their power consumptions are not included in the entire system.

Note that the input voltage range is not limited by the voltage reference or even the supply voltage. We can achieve a larger LSB from a higher input swing for a given number of levels. But there is trade-off between power consumption and performance. Here, V_H and V_L are set to 10mV and 0mV, respectively. 1 LSB thus equals 10 mV.

There is a SNR definition of LC-ADCs in [4][5], which depends on the ratio of timer frequency to the input frequency. Fig. 5 shows the output spectrum for a 1.1 kHz sinusoidal input with amplitude of 800mV. The timer works at 5MHz and a reconstruction sampling frequency of 102.4 kS/s is used. To compute a standard FFT for the simulation results, a third-order polynomial interpolator was adopted in MATLAB.

Fig. 6 shows the conversion, total current consumption and samples generation when we use an EEG signal [8] as the input. The first two pictures show the original analog input and the number of levels after conversion, respectively. Dynamic power saving can be seen from the third picture where I_D is lower than I_U. Note that the transient current I_D and I_U are due to the level-crossing detections from lower comparator and upper comparator, respectively. The bottom picture shows some of the samples generated with different densities in time domain, a smarter sampling is thus achieved. The performance comparison is given in Table I.

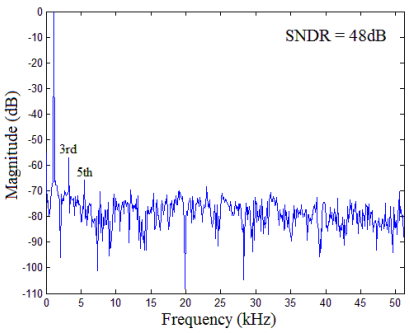

Fig. 5 FFT plot for 1.1 kHz sinusoidal input

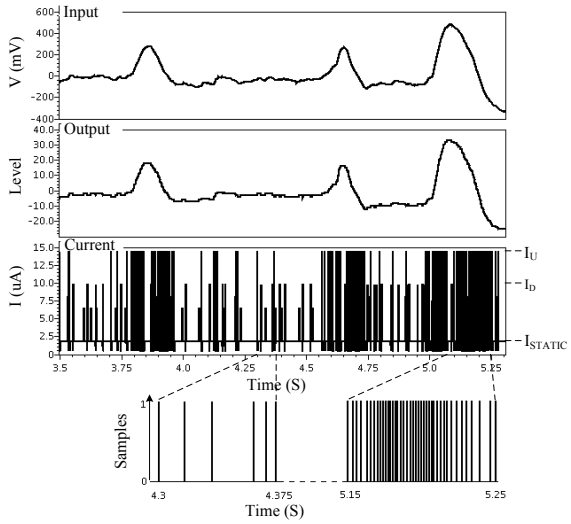

Fig. 6 EEG signal conversion, current consumption and generated samples

Table I Performance Comparison

	[3]	[4]	[6]	This work [a]
Technology	90nm	0.18µm	0.5µm	0.18µm
Supply(V)	1	0.7&1.4	3.3	0.7
Resolution	8 bit	8 bit	7 bit	8 bit
SNDR(dB) @kHz input	47@0.2 62@4 ($0.5V_{PP}$)	42.8@1.1 ($0.57V_{PP}$)	34@1 ($2.68V_{PP}$)	50@0.2 47@5 ($0.8V_{PP}$)
Input Swing	$=V_{REF}$	$>V_{REF}$	$>V_{REF}$	$>V_{REF}$
V_{REF}(V)	N/A	0.7	1.65	0.01
Power(µW)	>40 [b]	25 [c]	>10.7 [d]	1.42 [e]

a. Simulation results
b. Static power consumption
c. Without off-chip logic
d. Calculate from 4-channel static power consumption
e. For 5kHz, 0.8 V_{PP} sinusoidal input. Without up/down counter and timer

V. CONCLUSION

In this paper, novel architectures for the level-crossing ADC have been proposed. The circuit has been designed and simulated in AMS 0.18µm CMOS process. Lower power consumption and less design complexity are achieved due to the proposed topology. The event-driven characteristic makes the proposed ADC especially suitable for biomedical applications.

ACKNOWLEDGMENT

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