A COMPACT nA/V CMOS TRIODE-TRANSCONDUCTOR AND ITS APPLICATION TO VERY-LOW FREQUENCY FILTERS

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A simple nA/V CMOS transconductor for ultra-low power low-frequency g_m-C filters is introduced. Its input transistors are kept in the triode-region to benefit from the lowest g_m/I_D ratio. In contrast with weak inversion current-controlled techniques that demand an extremely low I_D, which is difficult to obtain precisely, the g_m is adjusted by a well defined (W/L) and V_{DS}, the latter a replica of the tuning voltage V_{TUNE}. Since the minimum V_{DS} is still considerably above the equivalent noise of the replica circuit, an improved control of g_m is achieved. The resulting design complies with V_{DD}=1.5V and a 0.35µm CMOS process. Its g_m ranges from 1.1nA/V to 5.5nA/V for 10mV $\leq V_{TUNE} \leq$ 50mV. A set of PSPICE simulations supports theoretical results. A designed bandpass filter has a 5Hz-center frequency and has a maximum idle dissipation of 17nW, whereas SNR=59.2dB for THD<1% @150mV peak value.

I. INTRODUCTION

On-chip realizations of large time constants are often required to design low cutoff-frequency (in the Hz and sub-Hz range) continuous-time filters in applications such as integrated sensors, biomedical signal-processing and neural networks. Due to their low-voltage low-power (LVLP) compatibility, g_m-C structures are a natural choice to perform the desired filtering characteristic. To limit capacitors to practicable values, a transconductor with an extremely small transconductance g_m (typically a few nA/V) is needed.

Previous work on LVLP CMOS techniques for obtaining very-low transconductances essentially combines different strategies such as voltage attenuation, source degeneration and current splitting [1-4]. The intrinsic input-voltage attenuating properties of floating-gate and bulk-driven techniques are exploited in [1]. The former solution demands nonetheless a double-poly fabrication process, whereas the latter implies in a finite input-impedance transconductor and lack of precision, as the bulk transconductance g_{mb} is very process-dependent. In the source-degeneration scheme presented in [2], a triode-biased transistor acts as a simple voltage-controlled resistor. Matching is a crucial problem in current splitting, since a large number of unity-cell transistors compose the current mirrors to implement very-high division factors. In [3], a downscaling factor of 40,000 is proposed, and in order to have all devices in strong-inversion for improved mirroring, a bias current of 15µA is forced. Because the final current of around 400pA is well above leakage, a more predictable transconductance is obtained, at the expense of power consumption. Conversely, a smaller division factor of 784 and a lower bias current are defined in [4], reducing the final current to only a few pA, which implies a less accurate transconductance.

Even though working either in weak, moderate or strong inversion, the transconductor input-transistor is always kept in saturation in the above-mentioned techniques. However, the lowest g_m/I_D ratio is obtained in strong-inversion triode-region (SI-TR), as discussed in Section II. Although this feature compromises the use of triode-transconductors in very-high frequency g_m-C filters, it turns out attractive when operation in the lower end of the frequency spectrum is devised. In [5], a low-g_m pseudo-differential transconductor based on a four-quadrant multiplication scheme is presented, in which the drain voltage of a triode-operating transistor follows the incoming signal. Nevertheless, because triode operation needs to be sustained, the input-signal swing is rather limited. Moreover, this solution only applies to balanced structures. Although triode-transconductors, in which the signal is directly connected to the input-transistor gate, have been successfully employed in high-frequency g_m-C filters [6,7], its potential for very-low frequency filter designing has not been exploited in the open literature.

This paper discusses the advantages and shortcomings of using a SI-TR transconductor to design ultra-low power low frequency g_m-C filters. Contrary to previous approaches, g_m is now controlled by a voltage rather than by a current. In a SI-TR MOSFET, by connecting the source terminal to one of the supply rails, a control voltage applied to the drain linearly adjusts g_m, as the latter scales with V_{DS}. Since (W/L) offers a degree of freedom in sizing g_m, V_{DS} values well above the equivalent noise of the replica circuit can be set, while still obtaining a very-low g_m. Consequently, filters with more predictable frequency characteristics can be implemented. Owing to its extended linearity, the SI-TR transconductor also handles larger signals, with no need for linearization techniques.

II. TRANSCONDUCTOR DESCRIPTION

A. Why strong-inversion triode-region?

The g_m/I_D ratio and the normalized drain current ratio N_{ID}, here defined as $I_D/I_{D_SI\text{-}TR}$, where $I_{D_SI\text{-}TR}$ is the drain current in SI-TR, are listed in Table I, for distinct MOSFET regions: SI-TR, weak-inversion saturation (WI-S) and strong-inversion saturation (SI-S). The gate-overdrive voltage is $V_{GO}=V_{GS}-V_{TO}$, where V_{TO} is the threshold voltage. U_T and *n* are the thermal voltage and the weak-inversion slope factor, respectively. As it can be noted, for a source-grounded device and V_{DS} small, the lowest g_m/I_D occurs for SI-TR operation, as V_{GO} can be set much higher than nU_T

For a given g_m, the current level in WI-S may easily become one order of magnitude lower than the one in SI-TR. For example, if V_{GO}=300mV, V_{DS}=20mV, n=1.2 and U_T=25mV, it turns out N_{ID}=0.10 for WI-S. For a specified g_m=2nA/V, the required I_D in WI-S is only 60pA, whereas in SI-TR I_D reaches 600pA. Although WI-S operation reduces the current/power consumption, the I_D required for a very-low g_m approximates the bound imposed by the junction leakage and its variation with temperature. Therefore, generating such a current reliably is difficult to achieve.

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	WI-S	SI-TR	SI-S
$\frac{g_m}{I_D}$	$\frac{1}{nU_T}$	$\frac{1}{V_{GO}-\frac{nV_{DS}}{2}}$	$\frac{2}{V_{GO}-nV_S}$
N_{ID}	$\frac{nU_T}{V_{GO}-\frac{nV_{DS}}{2}}$	1	$\frac{V_{GO}-nV_S}{2V_{GO}-nV_{DS}}$

Table I. g_m/I_D and N_{ID} ratios in different operation regions

B. Triode-Transconductor Circuit

A transconductor with a minimum transistor count helps reducing the equivalent noise. In this line, a compact triode-transconductor is proposed in Fig. 1. Input transistors M_{1A}-M_{1B} have their drain voltages regulated by an auxiliary amplifier that comprises M_{2A}-M_{2B}, M_{3A}-M_{3B} and bias current sources M_{5A}-M_{5B}. A simple current mirror M_{4A}-M_{4B} provides a single-ended output. Transistors are assumed pair-wise matched. Although the gate-source voltages of M_{3A} and M_{4A} are stacked, their values are below V_{TOn}, so that the circuit still complies with low-voltage requirements. The gate-voltage of M_{2A}-M_{2B} is set to $V_C=V_{TUNE}-|V_{GS2}|$, whereas V_B imposes a bias current I_B through M_{5A}-M_{5B}. Both voltages V_B and V_C are generated on-chip. Referring V_{TUNE} to V_{DD} and denoting $\beta_1=(W/L)_1\mu_pC_{ox}$, the transconductance of the entire circuit is

$$g_m = g_{m1} = \beta_1 V_{TUNE} \qquad (1)$$

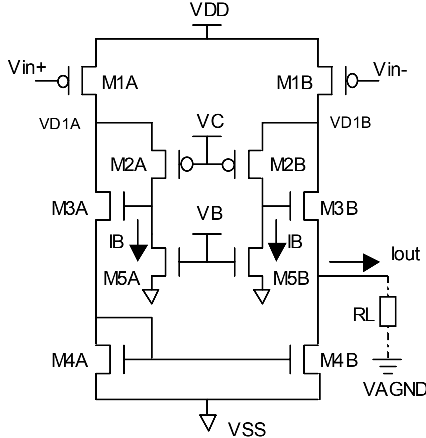

Fig. 1. Compact triode-transconductor

P-type input-transistors were chosen due to lower mobility and 1/f-noise coefficients as compared to similar parameters of n-MOSFETs. Except for M_{1A}-M_{1B} that stay in SI-TR, all remaining devices work in WI-S. Assuming M_{5A} (M_{5B}) to be ideal current sources, the transconductor output resistance r_{out} is given by

$$r_{out} \cong r_{ds1}(1 + g_{m2} r_{ds2}) \qquad (2)$$

Even though a common-drain configuration M_{3B} is seen from the output node, the transconductor still exhibits a relatively high output resistance, as the loop gain around M_{2B} and M_{3B} is relatively large.

To ensure that M_{1A}-M_{1B} remain in SI-TR, a trade-off between V_{TUNE} range and signal excursion should be established. Since the transconductor is usually embedded in a feedback topology in g_m-C filters, an identical swing should be assumed at input and output nodes. Lower and upper signal bounds, respectively V_{min} and V_{max}, are defined in Table II.

V_{min}	$V_{SS}+V_{DSAT4B}$
V_{max}	$\min(V_{in_max}, V_{out_max})$
V_{in_max}	$V_{DD}-\lvert V_{DS1\,max}\rvert-\lvert V_{TO1}\rvert$
V_{out_max}	$V_{DD}-\lvert V_{DS1\,max}\rvert-\lvert V_{DSAT2B}\rvert-V_{GS3B}$

Table II. Signal swing at transconductor input/output nodes

Common-mode voltage V_{AGND} that optimizes signal swing is $V_{AGND}=(V_{max}+V_{min})/2$, so that class-A operation is ensured by

$$I_B < \beta_1\left[\left(V_{DD}-V_{AGND}-V_{max}-\lvert V_{TO1}\rvert-\frac{n_pV_{DS1\,max}}{2}\right)V_{DS1\,max}\right] = I_{D1_Max} \qquad (3)$$

C. Bias Generator

Internal voltages V_B and V_C are derived from the circuit shown in Fig. 2. The generator is structurally alike the transconductor, with M_{1G}, M_{2G} and M_{3G} ideally matched to their counterparts. A servo-amplifier regulates M_{1G} drain-voltage to external voltage V_{TUNE}, so that $V_C \cong V_{TUNE}-|V_{GS2G}|$. Since $V_{GS2G} = V_{GS2A} = V_{GS2B}$, the expected value of V_C is achieved. A low-voltage OTA, with a topology similar to the one in [7], is employed as a servo-amplifier. Properly setting the current gain B (B >1) in M_{4G}-M_{5G} guarantees the value of I_B that complies with (3), while tracking down parameter variations on M_{1A} (M_{1B}).

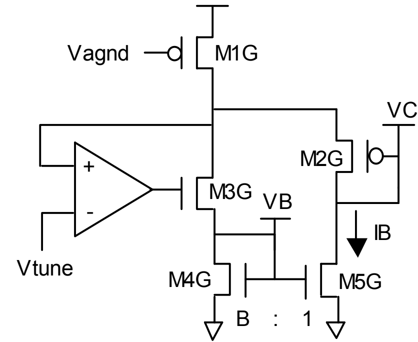

Fig. 2. Bias generator

D. Noise Properties

The MOSFET power spectral density (PSD) noise can be modeled either by a gate voltage source V_n^2 or a current source I_n^2 between drain and source. The latter is given by

$$I_n^2 = 4KTG_{nth} + \frac{K_F I_D^{A_F}}{C_{ox}L^2}\frac{1}{f^{E_F}} \qquad (4)$$

with $G_{nth} = g_m$ in SI-TR and $G_{nth} = g_m/2$ in WI-S [8], whereas K_F, A_F and E_F are 1/f-noise fitting coefficients. Even though the

dependence of the 1/f-noise component on transistor geometry and drain current varies with the operating region [9], such a fact is here disregarded, as available data on K_F were obtained using (6). Therefore, K_F is herein assumed constant with transistor bias, which has no physical support, particularly in ST-TR [9].

The circuit to evaluate the transconductor equivalent noise is shown in Fig. 3. For simplicity, only half-circuit of the transconductor is considered. Noise from M_3, M_4 and M_5 are represented by current sources, while those from M_1-M_2 are modeled as a voltage source $V_{ni}^2 = I_{ni}^2/g_{mi}^2$, for i =1,2. Upon usual assumption of uncorrelated noise sources and $g_m r_{ds}$>>1, the input-referred noise V_{nin}^2 is

$$\frac{V_{nin}^2}{2} = V_{n1}^2 + k_2^2 V_{n2}^2 + k_3^2 I_{n3}^2 + k_4^2 I_{n4}^2 + k_5^2 I_{n5}^2 \quad (5)$$

where coefficients k_2,k_3,k_4 and k_5 are listed in Table III. The intrinsic voltage-gain of M_1 corresponds to $\alpha_1 \cong -g_{m1}/g_{ds1}$, where $g_{ds1} = 1/r_{ds1}$. Since $|\alpha_1|$<< 1 usually occurs, the noise from M_2 is amplified when referred to the transconductor input. The 1/f-noise term on V_{n1}^2 is naturally minimized, as the gate-length of M_1 is chosen considerably long to obtain a very-low g_{m1}.

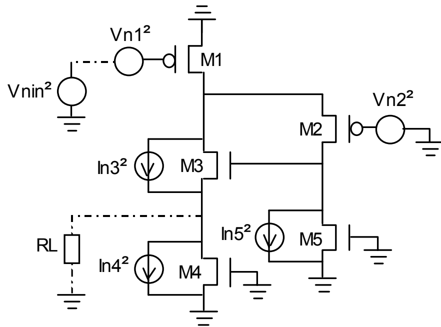

Fig. 3. Equivalent circuit for the transconductor noise analysis

k_2	$1/(g_{m1}r_{ds1})$
k_3	0
k_4	$1/g_{m1}$
k_5	$1/g_{m1}$

Table III. Coefficients k_2, k_3, k_4 and k_5

III. TRANSCONDUCTOR AND FILTER DESIGN

To back up the theoretical analysis, a SI-TR transconductor with g_m in the order of nA/V was designed and used as a building part in a low-frequency bandpass filter. The design complies with V_{DD}=1.5V and a standard 0.35μm n-well CMOS process, with typical parameters V_{THN}=0.50V, V_{THP} = -0.60V, $\gamma_n = 0.58V^{1/2}$, $\gamma_p = 0.45V^{1/2}$, μ_n = 403cm²/Vs, μ_p = 129cm²/Vs and C_{ox} = 446nF/cm². Flicker-noise coefficients are K_{Fn}=2.81e-27A²s/V, K_{Fp}=1.09e-27A²s/V, A_{Fn}=1.40, A_{Fn}=1.29 and E_{Fn}=E_{Fp}=1.

The tuning interval ranges from 10mV to 50mV, which implies 1.1nA/V≤g_{m1}≤5.5nA/V. The optimal V_{AGND} is 0.6V, theoretically limiting the signal amplitude to 185mV. Transistor sizes (in μm/μm) are $(W/L)_1$=(1.2/600), $(W/L)_2$=(10/100), $(W/L)_3$ = (12/2.4) and $(W/L)_4$ = $(W/L)_5$ = (40/40). These dimensions were determined with the aid of (5) and trade off 1/f-noise and layout area. Also, they comply with the weak-inversion onset $I_{lim}=2n(W/L)_1\mu_p C_{ox} U_T^2$ [9]. At nominal V_{TUNE} = 20mV, the calculated g_{m1} and common-mode current I_{D1CM} are 2.2nA/V and 0.63nA, respectively. A lossless integrator with C_{LOAD}=60pF has a unity-gain frequency f_{int} of 5.8Hz. Setting B=1.5 results in $I_B \cong$ 0.25nA, a good compromise between signal swing, 1/f-noise of M_{2A}-M_{2B} and M_{5A}-M_{5B}, thermal noise and auxiliary-amplifier power consumption

The gyrator-capacitor biquad bandpass filter of Fig. 4 was selected as an application example of the SI-TR transconductor. Assuming identical transconductors with g_{m1}=2.2nA/V, the calculated center frequency f_c is 5.8Hz. Owing to the large M_1 gate-area, the integrating capacitors should account for the transconductor input-capacitance C_{in}. For a SI-TR MOSFET, C_{GS} = C_{GD}= (1/2)WLC_{ox}, and, since $|\alpha_1|$<< 1, the Miller effect can be neglected, yielding $C_{in} \cong W_1L_1$Cox. Since V_{TUNE} is shared by all stages, a single bias-generator circuit can be used.

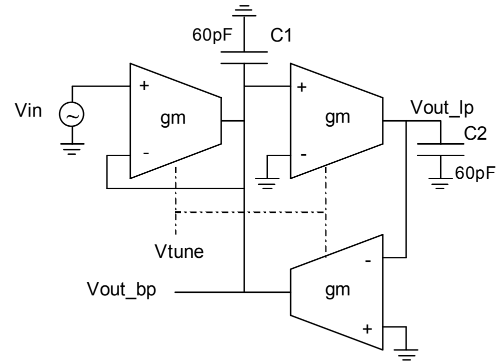

Fig. 4. Bandpass biquad filter

IV. SIMULATION RESULTS

Simulations were carried out using PSPICE 9.2 with Bsim3v3 models. With respect to its calculated value, V_{AGND} is decreased to 0.55V to improve the SNR, as observed in simulations. For a 1KΩ-load, fixing V_{in}^- =V_{AGND} and sweeping V_{in}^+, the g_{m1} dependence on tuning for 10mV ≤V_{TUNE} ≤ 50mV is plotted in Fig. 5. The transconductance remains almost constant in the linear region, scaling linearly with V_{DS1}.

The basic integrator exhibits $f_{_int}$ = 5.0Hz and an excess-phase of 0.6°, which indicates that the phase error is due to stray capacitances rather than to a finite r_{out}. Transconductor noise figures from PSPICE are in close agreement with the noise analysis of Section II. Calculation from (5) results in 51μV/√Hz @100mHz, 32μV/√Hz @10Hz (thermal component) and a corner frequency f_{nc} around 1Hz, whereas PSPICE gives 62μV/√Hz @100mHz, 43μV/√Hz @10Hz and $f_{nc} \cong$ 1Hz. The transconductor equivalent noise voltage for a 100mHz-10Hz bandwidth is 260μV_{RMS}. Similarly, the input-referred noise of the V_C generator is 42μV_{RMS}, so that for the lowest V_{TUNE} of 10mV, a tuning-to-noise ratio (TNR) of 47dB is obtained. Given that transistor geometries are well defined in modern fabrication processes, g_m can be controlled to a good extent, as it relies only on $(W/L)_1$ and V_{TUNE}.

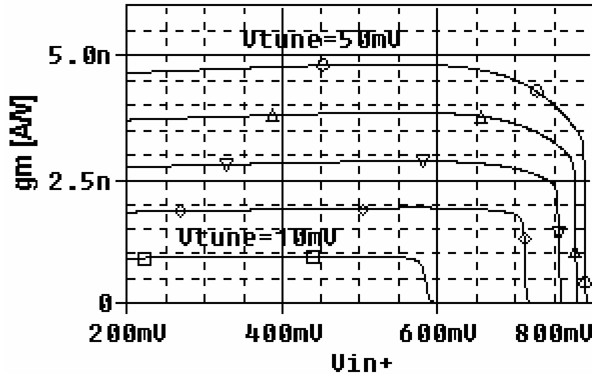

Fig. 5. Dependence of g_m on signal level and tuning

The frequency response of the bandpass section as function of the tuning voltage is displayed in Fig. 6. For 10mV≤ V_{TUNE}≤50mV, the center frequency ranges from 2.46Hz to 13.2Hz. A linear control of f_c by V_{TUNE} is observed, at a rate of 0.27Hz/mV. For comparison, the calculated f_c range and tuning rate are 2.9Hz ≤ fc ≤ 14.5Hz and 0.30Hz/mV, respectively. The maximum stand-by consumption of the filter is as low as 17nW. Assuming V_{TUNE} and V_{AGND} referred to V_{DD}, the filter characteristic suffers from no meaningful alteration, as the sensitivity of f_c to V_{DD} is only 0.7%.

At nominal tuning, the in-band equivalent noise is 116µV_{RMS}. Large-signal distortion corresponds to THD=1% for an amplitude of 150mV, so that an SNR of 59.2dB is attained. Since HD2 dominates, one may assume that a balanced version of the proposed transconductor would present better linearity. Monte Carlo analysis for a spread of ±0.5% on both (W/L) and V_{TO} parameters on every transistor of the filter revealed that the amplitude should be limited to 137mV to retain THD≤1%.

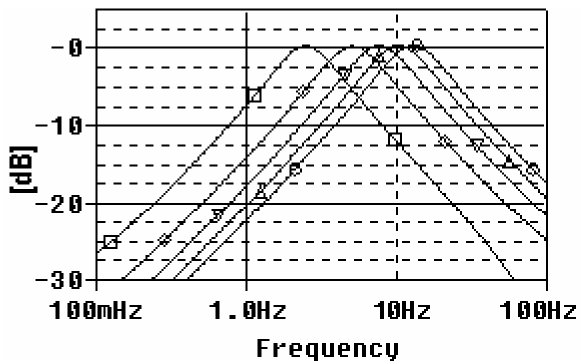

Fig. 6. Filter frequency response as function of tuning voltage

V. CONCLUSION

A compact CMOS transconductor suitable for ultra-low power g_m-C filters operating in the Hz and sub-Hz range has been proposed. Input transistors are kept in strong-inversion triode-region to profit from the lowest g_m/I_D. Because their drain voltages are regulated to V_{TUNE} by an auxiliary amplifier, g_m scales directly with (W/L) and V_{TUNE}. Such a voltage-controlled approach offers improved accuracy in obtaining g_m values in the order of nA/V, as the required I_D can be set well above expected values of leakage current.

The design was realized in accordance with V_{DD}=1.5V and a 0.35µm n-well CMOS process. Simulation data were obtained with PSPICE and Bsim3v3 models. The tuning voltage V_{TUNE} spans from 10mV to 50mV, yielding 1.1nA/V≤g_m≤5.5nA/V. For nominal g_m=2.2nA/V and C=60pF, the integrator unity-gain frequency and phase error are 5Hz and 0.6°, respectively, while the equivalent voltage noise is 340µV, for a 0.1Hz-10Hz bandwidth. Since the tuning-to-noise ratio TNR equals 47dB, accurate g_m control is achieved. As a design example, a bandpass filter is tuned from 2.46Hz to 13.2Hz, featuring a SNR of 59.2dB for THD=1%@150mV peak-value. The maximum stand-by consumption is only 17nW.

One may thus conclude that the proposed technique can be successfully applied to the design of low-frequency filters in power-stringent environments, such as human-implanted devices.

VI. ACKNOWLEDGMENT

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