# EFFECTS OF SUBSTRATE ON PHASE-NOISE OF BIPOLAR VOLTAGE-CONTROLLED OSCILLATORS

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## ABSTRACT

So far, there have been introduced many studies addressing the effects of the substrate on silicon-based integrated RF passive components, but none of them has addressed to what extent the substrate has influence on the RF front-end circuits and phenomena, such as noise-figure and phase-noise. In particular, there are many different models of spiral inductors on silicon, and even more substrate models of the very same inductors, all of them claiming to be the most-right representatives of their on-chip counterparts. When subjected to a verification in a circuit environment, for example in LC oscillators, those models often predict a dramatically different performance of the oscillators, being different phase-noise, voltage-swing, loop-gain and tuning-range, for a given power consumption. Therefore, this aspect of model verification is presented in this paper, showing that the design trajectory of LC-oscillators depends to an unallowably large extent on the inductor models used in the analysis. Also, it is shown that the phase-noise of a quasi-tapped oscillator is, contrary to common belief, not a monotonic function of a substrate resistivity.

## 1. INTRODUCTION

Since the early nineties, the design of integrated spiral inductors [1], has gained considerable attention, as the door for fully integrated RF front-end design was "open" for the first time. Indeed, full integration has numerous advantages over the use of external discrete components and circuits, imposing severe matching problems on the integration of the final design, introducing additional parasitics, and requiring more power due to 50Ω interfacing.

However, there are some disadvantages, mainly related to uncertainties in the modeling of integrated RF components. The models found in literature, describing the electrical behavior of monolithic inductors for example, are qualitatively different, even for the same technology, i.e., substrate. As a direct consequence of such a difference in circuit models, the results of computer simulations are substantially different as well. For oscillators, this means that the estimated oscillators'

performances fully depend on the chosen model parameters, representing the same on-chip inductor and the same technology. Accordingly, phase-noise, voltage-swing, loop-gain, tuning-range and power consumption of the LC-oscillator will not be the same, no matter the oscillator itself is the same.

The analysis presented in this paper, gives an insight into the effects of different substrate modeling, i.e., modeling of the corresponding spiral inductor on silicon, on the performance of quasi-tapped bipolar voltage-controlled oscillators [2], phase-noise being of most interest. Contrary to common belief, it is also shown that phase-noise is not only a decreasing or only an increasing function of substrate resistivity, but rather a convex function of substrate resistance, being electrical circuit equivalent of substrate.

The paper is organized as follows. After the introduction, a well-known model of spiral inductors on silicon is presented in Section 2. Effects of the substrate on LC oscillator performance is the subject of Section 3. Last section summarizes the conclusions of the presented analysis.

## 2. MODEL OF SPIRAL INDUCTOR

For the last decade, the characteristics of spiral inductors on silicon have been widely studied, with the emphasis on the metallization schemes and the properties of the underlying substrate. Consequently, it has appeared that while the metallization schemes and inductor geometries are "tamed" and properly mapped onto the corresponding models, the effects of the substrate on spiral inductors, i.e., their inductance and parasitics, are a "mystery", still being the stumbling block not only for the designers of integrated silicon-based RF passive components, but also for the designers of the RF front-end circuits.

To be beneficially used in a design of RF circuits of today, it is a craving necessity for the circuit designers to have a circuit model, describing electrical behavior of the monolithic inductors, at hand. However, the modeling is usually limited to one of the following options:

- fitting parameters of a lumped-element model to measured data [3,4]
- fitting parameters of a lumped-element model to results

of commercially available field-solvers [5,6]

- directly extracting parameters with the aid of computer programs [7,8]

Said to be the most complete, the lumped-element model of spiral inductor on silicon, shown in Fig. 1, will be used in the coming analysis.
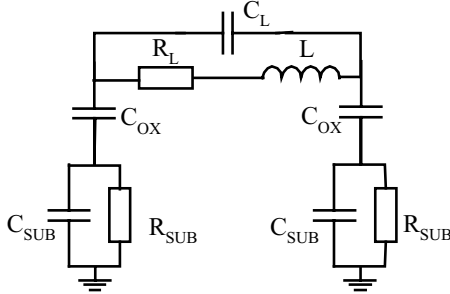


Fig. 1 Lumped-element model of spiral inductor on silicon.

The spiral coil itself is modeled by an ideal inductance $L$, a series resistance $R_L$, representing the ohmic losses in the coil, and an interwire capacitance $C_L$. The oxide capacitance between the spiral and the silicon substrate is modeled by $C_{OX}$. Representing the RF signal flow through the silicon substrate, the so-called substrate resistance and capacitance $R_{SUB}$ and $C_{SUB}$ are added as well.

Those are the series inductance and resistance, interwinding capacitance and oxide capacitance, the parameters that can be easily extracted from geometric and technological parameter specifications. This implies that the corresponding inductor model would be fully scalable, if substrate was not taken into account. Not only are the substrate resistance and capacitance unknown nor even scalable parameters of the model, but also it remains to be seen whether they are the most right representatives of the substrate effects on the inductor. Difficulties arise from the fact that ohmic losses in the conductive substrate, to be modeled in the electrical circuit model, are not easy to track and fully characterize, without full understanding of electromagnetic theory, being however out of the scope of the research area of the circuit designers. This, therefore, has resulted in yet incomplete knowledge on the substrate equivalent in circuitry.

In Tab. 1 the values of substrate resistance and capacitance for the model in Fig. 1, are shown for four different references, indicated in the table. Unlike the first reference (heavily-doped substrate), where the substrate resistivity and the epi-resistivity are 0.01Ω-cm and 10Ω-cm respectively, the others refer to a lowly-doped substrate with a resistivity of 10Ω-cm.

| Model\Reference | [5] | [9] | [3][8] |
|---|---|---|---|
| $R_{SUB}$ [Ω] | 35 | 385 | 600-800 |
| $C_{SUB}$ [pF] | 0.28 | 0.1 | <0.04 |

Tab. 1  Substrate parameters.

It is already obvious that if these values for $R_{SUB}$ and $C_{SUB}$ were used for the calculation of phase-noise in the corresponding LC-oscillator, the results would be certainly different. This is explicitly shown in the next section.

## 3. EFFECTS OF SUBSTRATE ON PERFORMANCE OF LC OSCILLATORS

There is a widespread belief that heavily doped substrates [3,6,8] offer poorer performance for the design of spiral inductors on silicon than their lowly doped counterparts. This is due to currents, being induced by the magnetic field of the inductor, that are free to flow in the heavily doped substrate, and cause both a decrease in inductance and an increase in resistive losses.

However, [9] is at standing that substrate eddy currents induced in the epi-layer sitting on low resistive substrates, are negligible up to several giga-hertz, and that a reason for a high-frequency degradation of inductor quality factor is in larger substrate parasitic capacitance only.

In line with this, on the example of a quasi-tapped VCO [2], shown in Fig. 2, the effects of the substrate on the performance of the oscillator, being in particular phase-noise, voltage swing and power consumption, will be examined. For this purpose, the values of the substrate resistance and capacitance, shown in Tab. 1, will be used for the model of the corresponding on-chip spiral inductors.
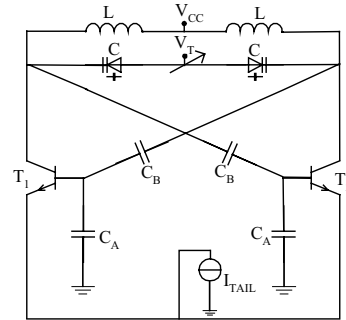


Fig. 2  Quasi-tapped VCO.

For the purpose of the analysis, let us first specify all the parameters of the oscillator. The frequency of oscillation is $f_0$=900MHz, the supply voltage is $V_{CC}$=2V. Parameters of the spiral inductors, also indicated in Fig. 3, are shown in Tab. 2, together with the technology parameters used in the calculations.

| Parameter | Value |
|---|---|
| Number of turns, $n$ | 5.25 |
| Track width, $w$ | 23um |
| Spacing between the tracks, $sp$ | 1um |
| Input diameter, $d_{IN}$ | 150um |
| Output diameter, $d_{OUT}$ | 387.5um |
| Track length, $l$ | 5.638mm |
| Metal thickness, $t_M$ | 1um |
| Metal resistivity, $\rho_M$ | 0.03Ω-um |
| Oxide thickness, $t_{OX}$ | 2.6um |

Tab. 2  Parameters of the inductor and technology.

When the inductance $L$ in Fig. 2 is substituted with the corresponding model shown in Fig. 1, the equivalent LC-tank of the oscillator is fully characterized by the model of Fig 4, that will be subsequently used for the simulations of the oscillator's performances.
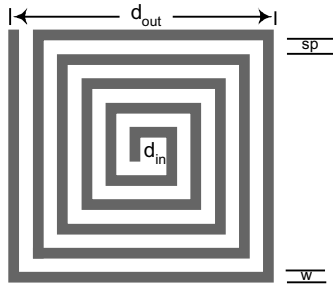
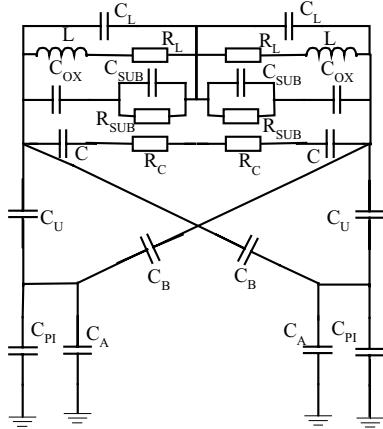Fig. 3 Layout of spiral inductor.



Fig. 4 Complete LC-tank.

Yet, $C$ is the varactor capacitance, $R_C$ its parasitic resistance, $C_U$ and $C_{PI}$ the parasitics of the transistors, and $C_A$ and $C_B$ the quasi-tapping capacitances.

In the analysis to come, the following notation will be used as well: $PN$ – phase-noise, $R_{SIG}$ – so-called signal resistance representing the LC-tank at resonant frequency, $V_{SIG}$ – voltage swing over tank, $P_{S\_S-UP}$ – safety start-up power consumption corresponding to the safety start-up condition, being the one with a loop-gain of two, $C$ – the varactor capacitance needed for the oscillations at the frequency $f_0$=900MHz, and $Q$ – the quality factor of the spiral inductor.

After supplying the $PNL$ (*phase-noise-inductance*) simulator [10] with the above specified values of the parameters of the quasi-tapped VCO, the following results are obtained:

| Parameter\Reference | [5] | [9] | [3][8] |
|---|---|---|---|
| $R_{SIG}$ [Ω] | 355 | 298 | 327 |
| $P_{S\_S-UP}$ [mW] | 1.5 | 2 | 1.8 |
| $V_{SIG}$ [V] | 0.48 | 0.40 | 0.44 |
| $PN@10MHz$[dBc/Hz] | -136 | -134 | -135 |

Tab. 3 Oscillator performances – comparison.

For geometry and technology dependent parameters of the model in Fig. 1, it is obtained: $L$=9.94nH, $R_L$=13Ohm, $C_L$ =99fF, $C_{OX}$=0.94pF. Note that all the results of the $PNL$ simulator are fully confirmed by the CADENCE simulation tool SpectreRF.

From these results, it is verified, that the performances of the oscillator are fully dependent on the chosen substrate parameters. Furthermore, this proves that both substrate parameters of the lumped-element model of spiral inductors, $R_{SUB}$ and $C_{SUB}$, and subsequent results of simulated VCO's are unreliable.

Let us now examine the effects of the substrate resistance on performance of quasi-tapped VCO, shown in Fig. 1, by means of the $PNL$ simulator. If the values of the VCO parameters are the same as in the previous example, then the simulation results can be presented as in Figs. 5, 6, and 7. Here, number of simulations is performed with the substrate resistance $R_{SUB}$ as a parameter that is changed between 12.5Ω and 3.2KΩ. Also, it is assumed that the inductor is placed either on a 10Ω-cm lowly-doped substrate or on a 10Ω-cm lowly-doped epi-layer sitting on a highly doped substrate. This allows as to use the relation $R_{SUB}C_{SUB}$=$\varepsilon_0\varepsilon_{SI}\rho_{SI}$=10ps [5,11], derived from the Maxwell equations.
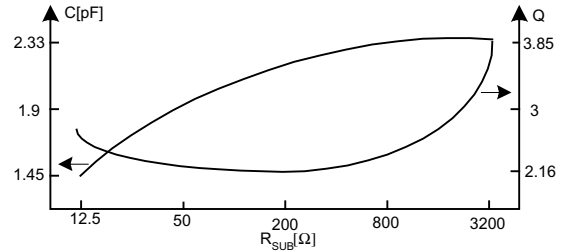


Fig. 5 Varactor capacitance and inductor quality factor versus substrate resistance.
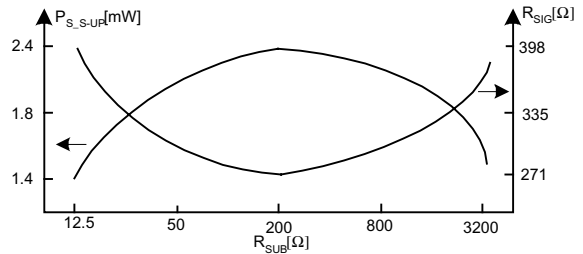


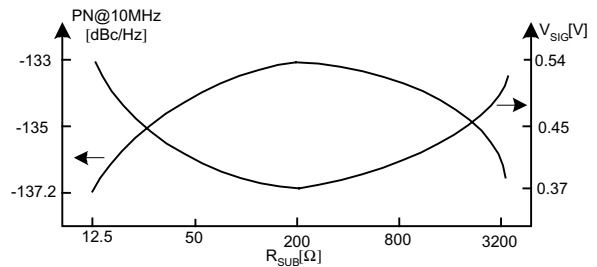Fig. 6 Safety start-up power consumption and signal resistance versus substrate resistance.



Fig. 7 Phase-noise and voltage swing over the tank versus substrate resistance.

Referring to these figures, a few very important remarks can be derived.

As suggested by [3,6,8], it is an ultimate goal to go for highly resistive substrates and accordingly high substrate resistance $R_{SUB}$ of the inductor model, as only under such conditions both high performance spiral inductors and high performance fully integrated VCO's are expected. In other words, they suggest that performances of both inductors on silicon and circuits to benefit with them are monotonic functions of substrate resistance $R_{SUB}$.

However, it appears that this is not in line with the results shown in Figs. 5, 6, and 7, respectively. Two high performance operating regions of the quasi-tapped VCO under consideration can be clearly identified. If the region of low $R_{SUB}$ corresponds to heavily-doped substrates and the region of high $R_{SUB}$ corresponds to lowly-doped substrates, it becomes obvious that both lead to the best performance of the oscillator, being the best phase-noise and LC-tank, the largest voltage swing, and the minimum power consumption. From Fig. 7 it can be seen that there is a difference of 4dB in phase-noise, depending on the substrate resistivity, i.e., substrate resistance.

In full agreement with [12], the following is observed as well. The high-frequency degradation of $Q$ for inductors on epi substrates is a direct consequence of the larger substrate capacitance. This means that unlike high-resistive substrates where the degradation of a quality factor of inductors is due to higher energy losses in the substrate, in case of low-resistive substrates, the degradation of $Q$ is referred to a lower self resonant frequency. This is confirmed by the simulations and shown in Fig. 5, as well. Note that a larger equivalent parasitic capacitance corresponds to a lower varactor capacitance, as the inductance $L$ and resonant frequency $f_0$ are kept constant.

Finally, contrary to common belief, the high-resistive substrates don't have to be the ultimate goal in the design of integrated spiral inductors, as the performance of corresponding integrated LC oscillators are not a monotonic function of substrate resistivity and its equivalent in the corresponding electrical circuit model, substrate resistance.

## 4. CONCLUSIONS

As the effects of the substrate on silicon-based RF passive components and their modeling have been widely studied, the effects of the very same substrate and corresponding models on the performance of the integrated RF circuits have not yet been examined to the extent required by circuit designers. Large differences in substrate modeling of spiral inductors impose uncertainty in the design of RF front-end circuits, in particular of LC oscillators.

Based on today's substrate models, the performances of the quasi-tapped VCO are compared for different substrate parameters. It is shown that simulation results depend to an unallowably large extent on the substrate resistance and capacitance, being the electrical circuit equivalents of substrate effects on spiral inductors.

Also, it is shown that there are actually two "high-performance" regions, corresponding to low and high resistive substrates, respectively.

Therefore a unique modeling of the substrate effects on spiral inductors must be considered as the main researcher's goal, simply because without an all-applicable and scalable model it is not possible to rely on computer aided design of fully integrated analog RF front-end circuits.

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