A 5b 12.9 μW Charge-Redistribution Phase Domain ADC for Low Power FSK/PSK Demodulation

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***Abstract*—This paper presents a 5 bit charge-redistribution phase domain ADC (PhADC) implemented in 0.18 μm CMOS technology for low power FSK/PSK demodulation. An IQ-assisted conversion algorithm is proposed to avoid the need for an accurate linear combination of in-phase (I) and quadrature (Q) signals with various scaling factors in a conventional zero-crossing algorithm, thus eliminating the power consumption and the phase nonidealities arising from such a linear combination. A PhADC based on a charge-redistribution DAC is demonstrated as a low power implementation of the algorithm due to the energy efficient operation in the charge domain. The prototype achieves an ENOB of 4.85 bit at 1 MS/s, while dissipating 12.9 μW from a 1.2 V supply, leading to a FoM of 1.2 pJ/step.**

I. Introduction

FSK modulation and PSK modulation are widely used in short range wireless personal and body-area networks due to their power efficient transmitter hardware and lower susceptibility to interference than ASK. Downconverted FSK/PSK signals are usually digitized by a pair of I and Q amplitude analog-to-digital converters (ADCs) before subsequent phase demodulation in the digital domain. Yet the data information is encoded in the signal phase alone rather than in the amplitude. Alternatively, I and Q signals can be directly digitized in the phase domain by a phase domain ADC (PhADC), resulting in compact and power efficient receiver systems [1-4]. The principle of the conversion algorithm employed in [1-4] is to detect the zero-crossings of rotated I and Q projections, i.e., a zero-crossing algorithm. A zero-crossing PhADC based demodulator has proven to have BER characteristics close to an ideal coherent GFSK demodulator [1]. The zero-crossing conversion algorithm has originally been realized in silicon by a resistor-bridge based approach featuring a large amplitude dynamic range [2], [5]. A current-mirror based approach [3], [4] has shown to reduce the power consumption and the area of the zero-crossing PhADC significantly.

However, the zero-crossing algorithm relies on accurate linear combinations of I and Q signals with various scaling factors, thereby limiting the efficiency and the simplicity of the hardware implementation. Besides, amplitude nonidealities arising from the linear combination circuitry also degrade the performance of zero-crossing PhADCs. For example, the 4 bit resistor-bridge based zero-crossing PhADC in [5] needs at least two power-hungry fully differential chopped OTAs to convert I and Q voltages into currents, which are subsequently converted into several phase-rotated voltages with the aid of a resistor bridge. The nonlinearities and the noise of the OTAs as well as the mismatch and the noise of the resistor bridge can introduce significant errors to the phase signal. In [3], [4], similar amplitude nonidealities also occur during the voltage to current conversion in the current-mirror based PhADC. Furthermore, both the resistor-bridge and the current-mirror based PhADCs operate in a flash-like fashion, thus consuming static power in either the resistor bridge or the current mirrors.

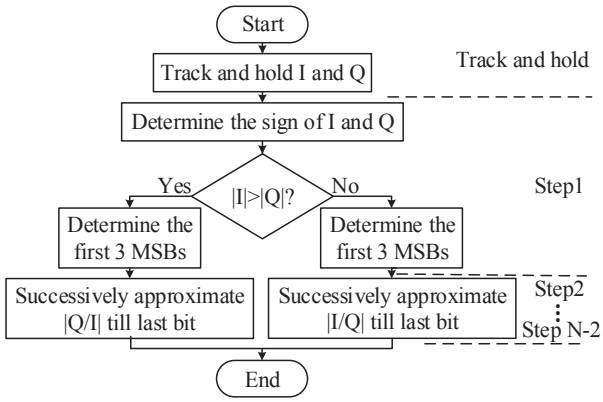

Figure 1. Flow chart of the proposed IQ-assisted conversion algorithm for an N bit PhADC.

In this paper, an IQ-assisted conversion algorithm is proposed to fundamentally avoid the accurate linear combination operation imposed by the zero-crossing algorithm, thereby eliminating the power consumption and the phase nonidealities stemming from the linear combination. A charge-redistribution PhADC is demonstrated as an energy efficient implementation of the proposed algorithm. In Section II, the proposed IQ assisted conversion algorithm and the system architecture are described, followed by a detailed description of the proposed PhADC in Section III. Measurement results are presented and compared to prior art in Section IV.

II. Conversion Algorithm and System Architecture

The proposed IQ-assisted conversion algorithm relies on the simple mathematical fact that for the phase, φ, it holds:

$$\varphi = \begin{cases} \arctan\frac{Q}{I} & Q < I \\ \operatorname{arccot}\frac{I}{Q} & I < Q \end{cases}, \varphi \in [0, \frac{\pi}{2}] \qquad (1)$$

where I and Q are the baseband in-phase and quadrature signals, respectively. Thus, the phase quantization between $[0, \frac{\pi}{2}]$ can be realized by the quantization of the ratio of either $\frac{Q}{I}$ or $\frac{I}{Q}$, depending on which one is greater, and the

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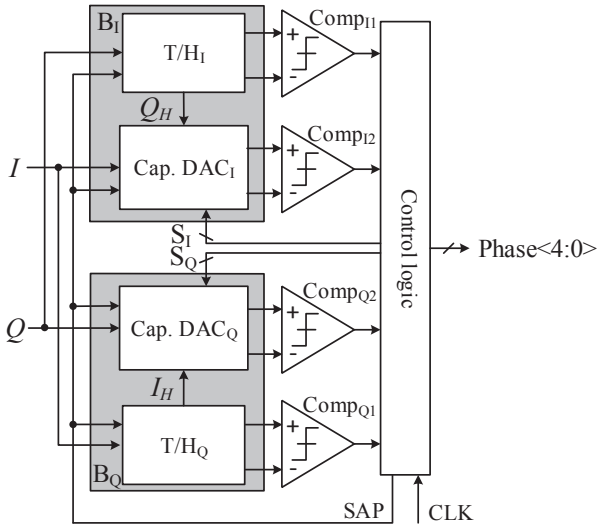

Figure 2. Proposed 5 bit PhADC block diagram.

mapping onto φ. Considering the symmetrical properties of the arctan and arccot functions in the phase domain, the phase quantization over the entire phase range $[0, 2\pi]$ can be realized by the quantization of a ratio factor a, which is defined as:

$$a = \begin{cases} |\frac{Q}{I}| & |Q| < |I| \\ |\frac{I}{Q}| & |I| < |Q| \end{cases}, 0 \le a \le 1. \tag{2}$$

The range of a indicates that the quantized phase is between 0 and $\frac{\pi}{2}$, but can be mapped back to the correct phase with the aid of the relations in (1) and the signs of the I and Q signals. The quantization process of a is essentially the same as that of a standard amplitude ADC, i.e., one amplitude is digitized by a reference amplitude, despite that the reference amplitude here is either the unknown I or the unknown Q rather than a known amplitude as is the case in the amplitude ADC. Consequently, the IQ-assisted algorithm could be implemented in a single (i.e., voltage or current or charge) domain like a standard amplitude ADC. In contrast with the zero-crossing algorithm, the IQ-assisted algorithm doesn't employ a linear combination of the I and Q signals with various scaling factors, hence doesn't require additional power consumption and doesn't suffer from any performance degradation introduced during the combination.

Fig. 1 shows the flow chart of the proposed algorithm for an N bit PhADC. After sampling the the amplitudes of I and Q, three comparisons are made in Step 1, viz., $I > 0?$, $Q > 0?$, and $|I| > |Q|?$. The result of $|I| > |Q|?$ can be resolved by determining $Q{>}I?$ and $-Q{>}I?$ with the aid of the signs of I and Q. Therefore, the first three most significant bits (MSBs) of the phase can be determined by the four comparisons in Step 1. In the next N-3 steps, I or Q is digitized by $(\pm)Q$ or $(\pm)I$ using a successive approximation algorithm, resolving the remaining N-3 bits. While any other standard amplitude conversion algorithm can also be applied from Step 2 to the end, the successive approximation algorithm is adopted to facilitate energy efficient charge domain operation.

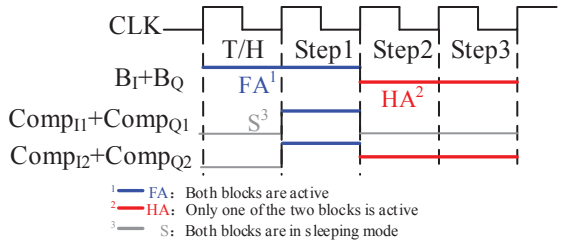

Figure 3. Circuit blocks are gated according to conversion phases.

The proposed 5 bit charge-redistribution PhADC diagram is shown in Fig. 2. Both the I and Q voltages are tracked and then held by a track-and-hold (T/H) circuit as well as a charge-redistribution DAC. The simultaneous T/H operation is controlled by the signal SAP. The voltages being held by two T/H circuits, i.e., T/H_I and T/H_Q, are Q_H and I_H, respectively. In conversion Steps 1-3, Q_H behaves as the reference voltage of DAC_I, while I_H is the reference voltage of DAC_Q. Four comparators, i.e., $Comp_{I1}$, $Comp_{I2}$, $Comp_{Q1}$ and $Comp_{Q2}$, determine the first 3 MSBs in Step 1. The last two bits can be resolved by a T/H circuit, a DAC and a comparator in the charge domain with low power consumption. Digital control logic decodes the comparator outputs and controls the switching procedure of DAC_I and DAC_Q via S_I and S_Q, respectively. In order to save power consumption further, all blocks are gated according to the conversion phases as illustrated in Fig. 3. Blocks B_I and B_Q denote the combination of T/H_I and DAC_I, and of T/H_Q and DAC_Q, respectively.

III. Circuits Design

A. Charge-redistribution DAC

The capacitance network of the PhADC implements another T/H operation besides the one made by the active T/H circuits, feedback DAC and summation node. As the phase is nonlinearly related to the ratio of I and Q (or Q and I) due to the arctan and arccot relations, in order to extract the linear phase, we need to nonlinearly map this ratio onto the quantized phase. In order to do so, two monotonic nonlinear unary DACs are implemented to approximate the nonlinear tan and cot functions between $[0, \frac{\pi}{2}]$ as follows:

$$\begin{aligned} \tan\frac{\pi}{16} &= \frac{Q}{I} \approx \frac{2}{10}, & \cot\frac{7\pi}{16} &= \frac{I}{Q} \approx \frac{2}{10} \\ \tan\frac{2\pi}{16} &= \frac{Q}{I} \approx \frac{4}{10}, & \cot\frac{6\pi}{16} &= \frac{I}{Q} \approx \frac{4}{10} \\ \tan\frac{3\pi}{16} &= \frac{Q}{I} \approx \frac{7}{10}, & \cot\frac{5\pi}{16} &= \frac{I}{Q} \approx \frac{7}{10} \\ \tan\frac{4\pi}{16} &= \frac{Q}{I} = 1 \quad , & \cot\frac{4\pi}{16} &= \frac{I}{Q} = 1 \end{aligned} \tag{3}$$

As shown in Fig. 2, the approximated tan function is realized by DAC_Q with Q being the input voltage and I_H being the reference voltage, whereas the cot function is realized by DAC_I with I being the input voltage and Q_H being the reference voltage. The architectures of the two DACs are identical. The largest error generated by the approximation is

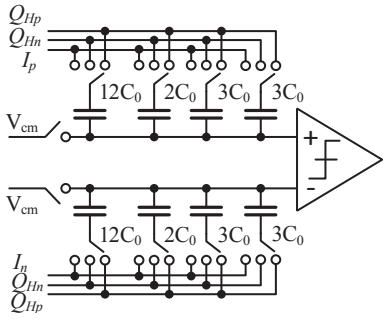

Figure 4. 2 bits unary-weigthed charge-redistribution DAC_I. DAC_Q has the same architecture.

only $0.7° = 0.06$ times the phase least significant bit (LSB), which is not a dominant source of error.

The DAC in the I signal path, DAC_I shown in Fig. 4, is taken as an example to describe its major design considerations. A differential DAC architecture is employed here since the I and Q_H as shown in Fig. 2 have different common mode voltages. Moreover, the differential architecture suppresses the odd-order amplitude nonlinearities of I and Q_H, hence reducing the phase error introduced by them. Each side of the differential network has 20 unit capacitors, which are segmented in such a way that the scaling factors in (3) can be obtained by the differential switching operation, viz., $\frac{2}{10} = \frac{12}{20} - \frac{8}{20}$, $\frac{4}{10} = \frac{14}{20} - \frac{6}{20}$, and $\frac{7}{10} = \frac{17}{20} - \frac{3}{20}$. The unit capacitor is implemented as a metal-metal capacitor by using only metal 5 (the one below the "analog metal") with a small value of 2.4 fF, which achieves a good trade-off between power efficiency and accuracy. Since Q_{Hp} and Q_{Hn} vary between 0.35 V to 0.85 V, complementary switches are used for Q_{Hp} and Q_{Hn} to reduce the nonlinearity.

B. T/H circuit and comparator

The low precision T/H circuit shown in Fig. 5(a) [6] is used in our design, due to its favorable energy efficiency and sufficient linearity in this relatively low resolution prototype. In post-layout simulations, the T/H circuit achieves a THD of -43 dB with a 499 kHz 1 Vpp input, and consumes 1.6 μA.

Due to the limited driving ability of the T/H circuit and the small value of the capacitor network (i.e., around 50 fF at each input node of the comparator), kickback noise is of primary concern in the comparator selection and design. We have adopted the static comparator shown in Fig. 5(b) [7] for our design. Two reset NMOS switches in parallel with the NMOS latch in [7] are replaced by a single switch M12, precharging Nodes V_{op} and V_{on} before the decision phase to increase speed. However, the precharged V_{op} and V_{on} may give rise to a static current in the subsequent SR latch during the reset phase if V_{op} and V_{on} are directly connected to the SR latch. For this reason, AND gates A1 and A2 are added to isolate the SR latch from the precharged analog voltages. The comparator can operate at 4 MHz clock rate. Its maximum input-referred offset measured through 200 Monte Carlo runs is 15 mV. M10 + M11 in Fig. 5(b), and M9 + M10 in Fig. 5(a) are used to enable/disable the comparator and the T/H circuit, respectively, thereby saving unnecessary power.

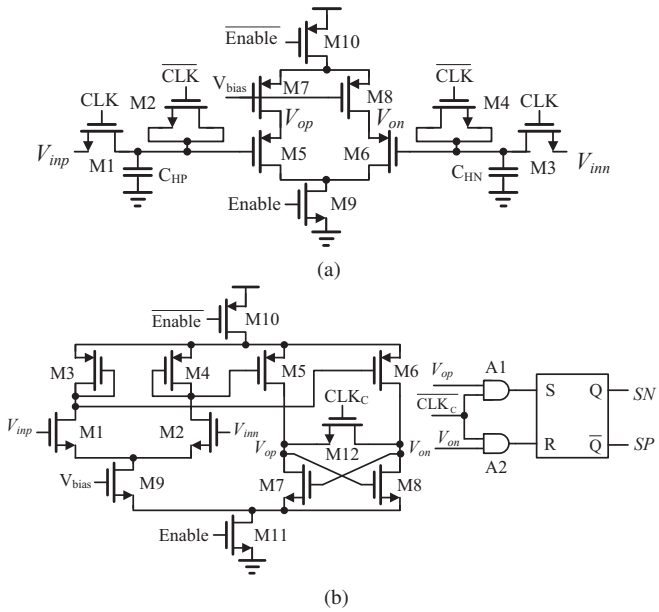

Figure 5. (a) Track-and-hold circuit. (b) Comparator circuit.

IV. Measurement Results

The prototype charge-redistribution PhADC was fabricated in 0.18 μm AMS CMOS technology with a core chip area of 0.059 mm^2. A micrograph of the die is shown in Fig. 6. The performance of the ADC was measured at 1.2 V and a 1 MS/s sampling rate. The 5 bit output is captured using a logic analyzer and fed to MATLAB for performance evaluation.

The dynamic performance of a standard amplitude ADC is usually measured with a single-tone input signal. Similarly, a complex signal (i.e., a pair of I and Q signals) with a single-tone phase input, i.e., $\pi\cos(\omega t)$ is used here to characterize the proposed PhADC. Due to the nonlinear relationship between the phase and the complex signal, the spectrum of the complex signal corresponding to the single-tone phase consists of several frequencies harmonically related to the phase frequency. For example, if only the first two non-DC frequency components of the I and Q signals are taken into account, the bandwidth of the I and Q signals is 8 times the phase frequency. Considering the channel bandwidths of low power short range standards, e.g. IEEE 802.15.6 [8], ranging from 300 kHz to 1 MHz, this prototype is designed for a phase frequency up to 62 kHz, and is specified up to the Nyquist frequency (i.e., 499 kHz).

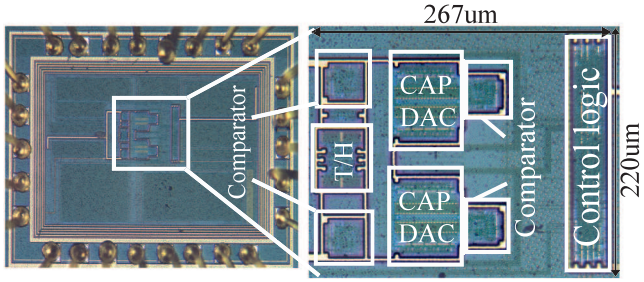

Figure 6. Die micrograph of the charge-redistribution PhADC

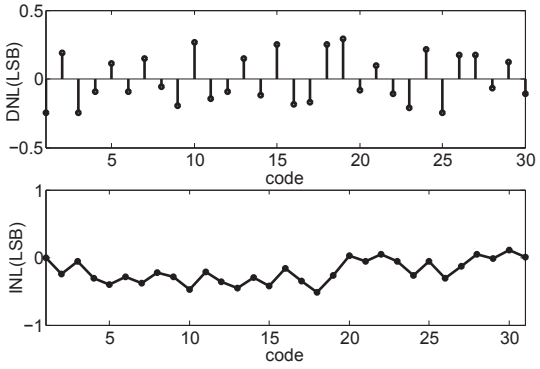

Figure 7. Measured DNL and INL. The differential peak-to-peak voltages of the I and Q signals are 900 mV.

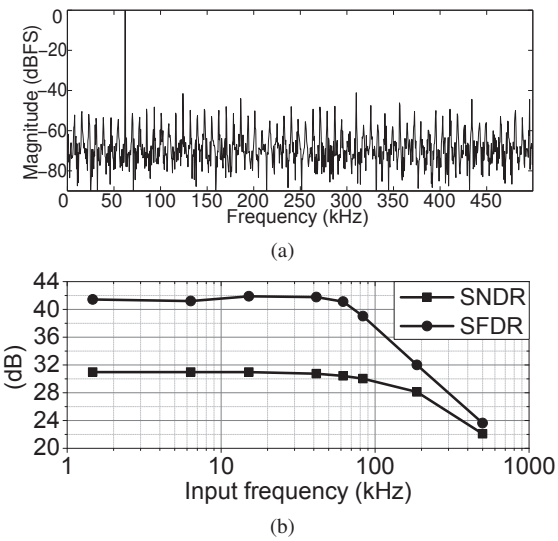

Figure 8. (a) Measured spectrum (2048-point FFT) at 1 MS/s with a 62.01 kHz input phase. (b) SNDR and SFDR as a function of input phase frequency. The differential peak-to-peak voltages of the I and Q signals are 900 mV.

The maximum DNL and INL are +0.29/-0.29 LSB and +0.11/-0.52 LSB, respectively, as shown in Fig. 7. Fig. 8(a) shows the output spectrum for a 62.01 kHz input phase, and Fig. 8(b) shows the SNDR and SFDR as a function of the input phase frequency. The SNDR at 1.5 kHz is 30.98 dB, i.e., yielding an ENOB of 4.85 bit, while the ERBW is 187 kHz. The decreased SNDR with increasing frequency is mainly due to the expanded bandwidth of the complex signal and the frequency-dependent nonlinearity of the T/H circuit. Like the PhADC in [3], [5], the proposed PhADC also features a large amplitude dynamic range (DR) as shown in Fig. 9. The SNDR at 1.2 Vpp is 30.9 dB, and drops by 3 dB at 0.4 V, indicating an amplitude DR of 9.5 dB. The ADC consumes 10.76 μA from a 1.2 V power supply, translating into a FoM of 1.2 pJ/step at 1 MS/s. The performance of the proposed ADC is summarized and compared with prior art in Table I.

V. Conclusions

The hardware implementation of the zero-crossing algorithm employed in PhADCs is power hungry and susceptible to the amplitude nonidealities. An IQ-assisted conversion algorithm is proposed to eliminate the linear combination operation, thereby reducing the power consumption and phase nonidealities caused by the operation. This algorithm is implemented in a charge-redistribution PhADC and proves to be an energy efficient solution with respect to prior art.

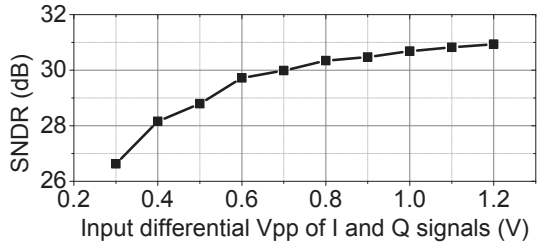

Figure 9. Measured SNDR as a function of the differential peak-to-peak voltages of the I and Q signals with a phase frequency of 62.01 kHz.

Table I
Performance comparison.

	[3]	[5]	This work
Technology (μm)	0.13	0.18	0.18
Power supply (V)	1	1.2	1.2
Power (μW)	25	348	12.9
Sampling rate (MS/s)	20	3.2	1
Resolution (bit)	4	4	5
ENOB (bit)	3.61	-	4.85
ERBW (kHz)	123.1[a]	-	187
FoM[b] (pJ/step)	8.3	-	1.2
Amplitude DR (dB)	19[a,c]	41[d]	9.5[c]
Chip area (mm^2)	0.015	0.044	0.059

[a]Estimated from [3]. [b]FoM=Power/($2^{ENOB}\cdot 2\cdot$ERBW).
[c]The range over which SNDR remains constant within 3dB.
[d]The range over which the maximum quantization error < 0.5 LSB.

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