Dynamic Translinear Nonlinear Energy Operator

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***Abstract*—The dynamic translinear principle, in contrast to the conventional, i.e., static, translinear principle, can be used for the realization of frequency dependent transfer functions. Using the dynamic translinear principle we can realize both linear and nonlinear differential equations. This paper presents the dynamic translinear realization of the nonlinear second-order differential equation describing the nonlinear energy operator performing the real time energy detection of analog signals. The expected behavior of the designed nonlinear energy operator is demonstrated by means of simulations.**

***Index Terms*—nonlinear energy operator, structured synthesis, dynamic translinear circuits, non-linear, analog integrated circuits, low power, low voltage**

I. Introduction

Translinear circuits are based on the exponential behavior of the bipolar transistor or the MOS transistor operating in the sub-threshold region. Translinear circuits are supposed to be a promising alternative in the area of low-voltage design, as the voltages in the translinear circuits are logarithmically related to the currents. Conventional, i.e., static, translinear circuits can be used to realize a wide variety of linear and nonlinear functions. By allowing capacitors in the translinear loops, the dynamic translinear circuits can be used to implement linear and nonlinear differential equations [1]. As an extension to conventional translinear circuits, dynamic translinear circuits inherit advantages of conventional translinear circuits. The main advantage is a high functional density, which makes translinear circuits suitable for low voltage, low-power applications.

To monitor the real-time energy of neural signals, including action potentials (spikes) and local field potentials [2], [3], the nonlinear energy operator (NEO) [4] is considered a good candidate since it is capable of discriminating between the desired pulse and the background noise as their energies are considered differently [5]. The NEO implements a nonlinear second order differential equation which is can directly put on silicon by using dynamic translinear circuit techniques.

In this paper, we apply the structured synthesis method for dynamic translinear circuits [6] to design the NEO. The static and dynamic translinear principles are reviewed in Section 2. In Section 3, the design of the NEO using the proposed synthesis method employing bipolar transistors is given. Section 4 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 5.

II. Translinear Principle

Translinear (TL) circuits can be divided into static (STL) and dynamic (DTL) circuits. Using STL circuits we can implement linear and nonlinear static transfer functions. Frequency-dependent (transfer) functions, i.e., differential equations (DEs) can be realized by DTL circuits. In this section we will review the STL and DTL principles by means of two examples.

A. Static Translinear Principle

The TL principle is based on the exponential behavior between voltage and current of the bipolar transistor and the MOS transistor in weak inversion region. In the following discussion, bipolar transistors are assumed. The collector current of bipolar transistors is given by

$$I_c = I_s e^{(V_{be}/V_T)}, \tag{1}$$

where I_s is the zero-bias current, V_{be} is the base-emitter voltage, $V_T = kT/q$ is the thermal voltage.

The TL principle applies to loops of semiconductor junctions, characterized by an even number of junctions [7], [8]. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Fig. 1. It is assumed that the transistors are biased at collector currents I_1 through I_4. When all devices are equivalent and operate at the same temperature, the TL loop is described by a simple static equation

$$I_1 I_3 = I_2 I_4. \tag{2}$$

B. Dynamic Translinear Principle

By admitting capacitors in the TL loops, frequency-dependent transfer functions can be realized. The DTL principle can be explained with reference to the sub-circuit shown

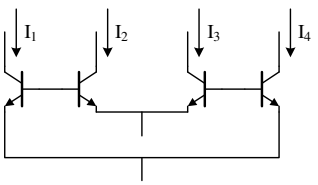

Figure 1. A four-transistor translinear loop.

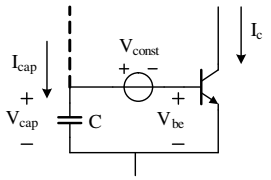

Figure 2. Principle of dynamic translinear circuits.

in Fig. 2. This circuit is described in terms of the collector current I_c and the capacitance current I_{cap} flowing through capacitance C. Note that the dc voltage source V_{const} does not affect I_{cap}. An expression for I_{cap} is easily be derived by taking the time derivative of (1)

$$I_{cap} = CV_t \frac{\dot{I}_c}{I_c}, \tag{3}$$

where the dot represents differentiation with respect to time. Equation (3) shows that I_{cap} is a function of I_c and its time derivative $\dot{I}_c$. By slightly rewriting equation (3)

$$CV_t \dot{I}_c = I_{cap} I_c, \tag{4}$$

we can directly state the DTL principle: *A time derivative of a current can be mapped onto a product of currents* [6]. From this point on, the product of currents on the right-hand side of (4) can easily be realized by the conventional STL principle. The DTL principle can be used to implement a wide variety of DEs, describing signal processing functions.

III. Dynamic Translinear NEO Operator

This section demonstrates the design of the NEO using the DTL structured synthesis method. Synthesis of a dynamic circuit, starts with a DE or with a set of DEs describing its function. The NEO operator can be described in the time domain by

$$y(\tau) = \left(\frac{\partial x(\tau)}{\partial \tau}\right)^2 - x(\tau)\frac{\partial^2 x(\tau)}{\partial \tau^2}, \tag{5}$$

where x and y represent the input and the output signal, respectively.

At first glance from (5), it seems like, in order to realize this function, differentiator, squarer and multiplier circuits are needed, which leads to a complex topology. Using the DTL structured synthesis method, (5) can be implemented by a very simple and compact topology of translinear loops circuit which will be shown shortly.

A. Transformations

An important difference between the mathematical and electronic domain is that the latter one is bounded by quantities having dimensions. To find an implementation of the mathematical equation we need to transform all time-varying signals in the DEs, i.e., the input signals, the output signals and the tunable parameters into currents [6]. Thus, the first step of dynamic structured synthesis is to add dimensions to the dimensionless mathematical equations. For the above expression, x and y can be transformed into the currents $I_{in} = xI_o$ and $I_{out} = yI_o$, I_o being the DC bias current that determines the absolute current swings. The dimensionless time τ, can be transformed into the time t with its usual dimension [s], using the equivalence relation given by

$$\left(\frac{\partial}{\partial \tau}\right)^k = \left(\frac{CV_t}{I_o}\right)^k \left(\frac{\partial}{\partial t}\right)^k. \tag{6}$$

Subsequently, dimensionless differential equation (5) is transformed into current-mode differential equation

$$I_{out} I_o^3 = (C_1 V_t \dot{I}_{in})^2 - I_{in} (C_2 V_t)^2 \ddot{I}_{in}. \tag{7}$$

B. Definition of the Capacitance Currents

By introducing the capacitance currents we are able to implement DEs by translating time derivatives into products of currents. Note that (5) is a second-order differential equation, which means that we need to take the time derivative of the first capacitance current that already contains the time derivative in order to map this equation on silicon. Thus, we need two capacitance currents. Defining I_{cap1} and I_{cap2} as

$$I_{cap1} = C_1 V_t \frac{\dot{I}_{in}}{I_{in} + I_o} \tag{8}$$

and

$$\begin{aligned} I_{cap2} &= C_2 V_t \frac{\dot{I}_{cap1}}{I_{cap1} + I_o} \\ &= C_1 C_2 V_t^2 \frac{\ddot{I}_{in}(I_{in} + I_o) - \dot{I}_{in}^2}{(I_{in} + I_o)^2 (I_{cap1} + I_o)}. \end{aligned} \tag{9}$$

for $C_1 = C_2$, current-mode differential equation (7) yields a current-mode polynomial without derivatives:

$$\begin{aligned} I_{out} I_o^3 &= I_{cap1}^2 (I_{in} + I_o)^2 \\ &- I_{in}(I_{in} + I_o)(I_{cap1} + I_o) I_{cap2} \\ &- I_{in}(I_{in} + I_o) I_{cap1}^2. \end{aligned} \tag{10}$$

As we can see, the above DE is now described by a current-mode polynomial where the time derivatives and capacitances are hidden in the capacitance currents. Observe that input current I_{in} and both capacitance currents, I_{cap1} and I_{cap2} can be positive and negative. As a consequence, a bias current needs to be added such that the collector currents always remain positive. By doing so, (10) becomes (11)

$$\begin{aligned} I_{out} I_o^3 &= I_o(I_o + I_{in})(I_o + I_{cap1})^2 \\ &- I_o(I_o + I_{in})(I_o + I_{cap1})(I_o - I_{cap2}) \\ &- I_o(I_o + I_{in})^2 (I_o + I_{cap1}) + I_o^3 (I_o + I_{in}) \\ &+ (I_o + I_{in})^2 (I_o + I_{cap1})(I_o - I_{cap2}) \\ &- I_o^2 (I_o + I_{in})(I_o + I_{cap1}). \end{aligned} \tag{11}$$

Both sides of the above DE are now described by current-mode polynomials and from this point on, the synthesis procedure for static TL circuits can be used [8].

C. Translinear Decomposition

The next synthesis step is translinear decomposition. That is, the current-mode polynomial has to be transformed into one or more TL loop equations that are characterized by the general equation

$$\prod_{CW} J_{C,i} = \prod_{CCW} J_{C,i}, \tag{12}$$

$J_{C,i}$ being the transistor collector current densities in clockwise (CW) or counter-clockwise (CCW) direction. As 'non-parametric' decomposition is not always possible, we can utilize 'parametric' decomposition of (11). It means that one or more intermediate currents need to be defined, introducing extra TL loops. If possible, extra TL loops should be included into existing TL loops, which will save us extra current branches and lower the total power consumption. Here, two intermediate currents I_A and I_B are defined. As a result, there will be four valid TL equations (13), (14), (15) and (16)

$$I_B I_o = (I_{in} + I_o)(I_{cap1} + I_o), \tag{13}$$

$$I_A I_o^2 = (I_{in} + I_o)^2 (I_{cap1} + I_o), \tag{14}$$

$$\begin{gathered}[I_{out} + I_A - (I_{in} + I_o) + 2I_B]I_o \\ = \\ [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o]I_L,\end{gathered} \tag{15}$$

$$\begin{gathered}(2I_B - I_A)(I_o - I_{cap2}) \\ = \\ [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o]I_R,\end{gathered} \tag{16}$$

with

$$I_L + I_R = I_B. \tag{17}$$

These functions are readily implemented in TL circuits [7], [8].

D. Circuit Implementation

The last synthesis step is the circuit implementation. The TL decomposition that was found during the previous synthesis step has to be mapped onto a TL circuit topology. A possible realization of the first capacitance current and intermediate currents is shown in Fig. 3. The TL loop formed by $Q_1 - Q_2 - C_1$, implement (8). Note that V_{BEQ2} can be considered a constant voltage source. Transistors $Q_1 - Q_2 - Q_3 - Q_4$ and $Q_1 - Q_2 - Q_3 - Q_5 - Q_6 - Q_7$ implement (13) and (14), respectively. M_2 through M_4 provide feedback and minimize the base currents, which results in more accurate intermediate currents. M_1 and M_5 ensure that the correct collector current will flow through Q_1 and set the V_{CQ1} to desired value. V_{ref1} provides some headroom for M_5.

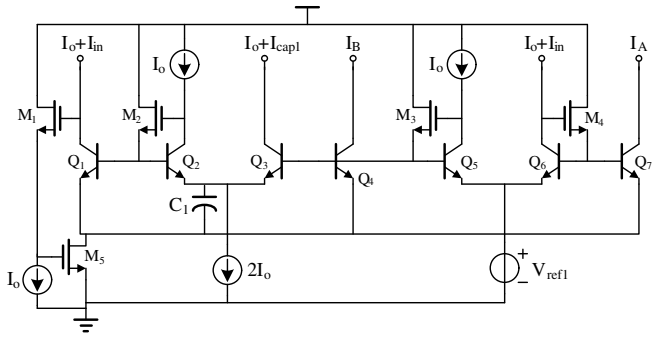

Figure 3. Implementation of the capacitance and the intermediate currents: (8), (13) and (14)

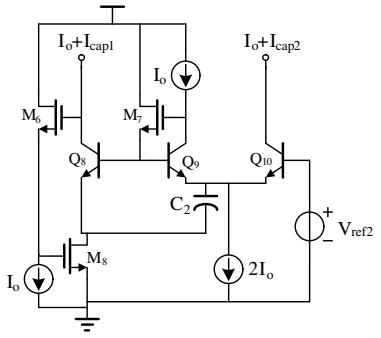

Figure 4. Implementation of the capacitance current: (9)

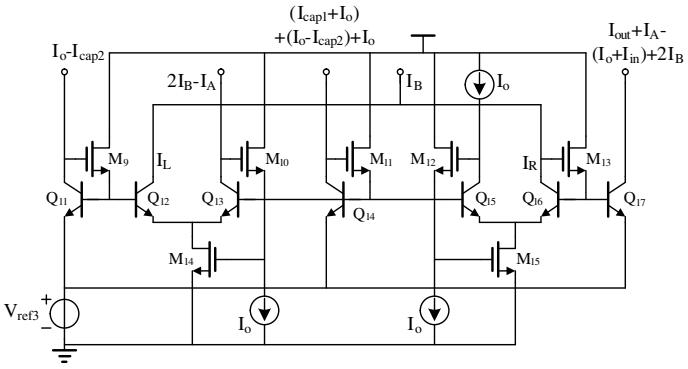

Figure 5. Implementation of the TL loops equations (15) through (17)

In Fig. 4, a circuit realizing the second capacitance current is shown. Loop $Q_8 - Q_9 - C_2$ implements (9). Voltage V_{be} across Q_9 is constant. M_6 and M_8 have the same function for Q_8 as M_1 and M_5 for Q_1. Function of M_7 is to minimize base currents. Headroom of M_8 is ensured by properly choosing V_{ref2}.

Fig. 5 shows the circuit that implements (15) through (17). Transistors $Q_{11} - Q_{12} - Q_{13} - Q_{14}$ and $Q_{14} - Q_{15} - Q_{16} - Q_{17}$ implement (15) and (16), respectively. The function of the MOS transistors M_9 through M_{15} is as discussed before. V_{ref3} lifts the drain voltage of M_{14} and M_{15} for proper biasing.

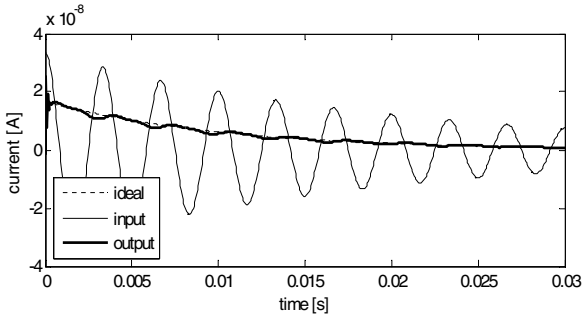

Figure 6. NEO applied to a damped sinusoidal signal. The output of NEO is showing the energy of the input sinusoidal.

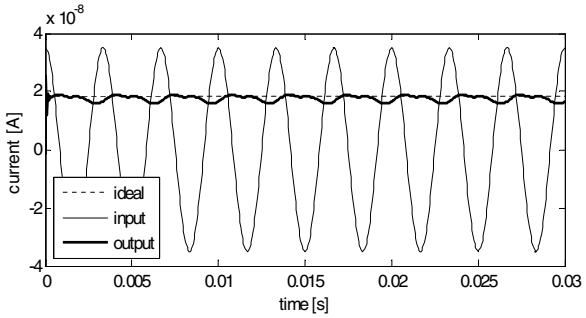

Figure 7. NEO applied to a constant sinusoidal signal. The output of the NEO has a constant magnitude when the input signal amplitude and frequency are constant.

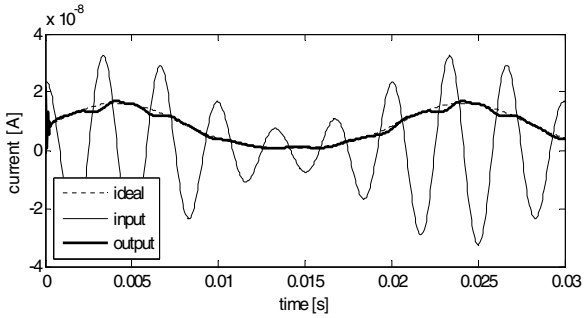

Figure 8. NEO applied to the sum of two sinusoids with different frequencies and the same amplitude. The output of the algorithm oscillates at the different frequency, about the sum of the energies in the two sinusoids.

IV. Simulation Results

The final circuit was verified in Cadence using RF spectre and AMIS 0.35 μm technology (I3T80). MOS transistor width (W) and length (L) were set as $W/L_{1-13} = 2\mu\text{m}/0.7\mu\text{m}$, $W/L_{14} = 4\mu\text{m}/0.7\mu\text{m}$ and $W/L_{15} = 1\mu\text{m}/1\mu\text{m}$. NPN transistor area is $16\mu\text{m}^2$. Supply voltage $V_{DD} = 2\text{V}$, reference voltages $V_{\text{ref1}} = 0.2\text{V}$, $V_{\text{ref2}} = 0.72\text{V}$, $V_{\text{ref3}} = 0.1\text{V}$ and bias current $I_o = 100\text{nA}$. The quiescent power consumption equals $7.2\mu\text{W}$.

Fig. 6 shows the transient response of the NEO in case a damped sinusoidal signal is applied to the input. The dashed line represents the output current of the NEO for the ideal case where (7) is applied directly to the input signal and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. It can be seen that for larger input signal amplitudes, the output of the NEO is showing higher "energy". Lower energy occurs at a lower amplitude.

In the case of a constant amplitude and frequency sinusoidal input signal, the result is shown in Fig. 7. The dashed line represents the output current of the NEO for the ideal case and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. It can be seen that in this case the NEO circuit is able to detect the energy of the input signal with small error resulting from nonideality effects in the form of a small ripple appearing at the output.

The output of the NEO, in case of an input signal consisting of two frequency components is shown in Fig. 8. The dashed line represents the output current of the NEO for the ideal case and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. The output signal also follows the real energy of the input signal with a small error.

V. Conclusions

In this paper, the application of the dynamic translinear principle to realize a nonlinear second order differential equation to be used in real-time energy detection has been shown. The BiCMOS version of the resulting circuit comprises two identical capacitors and a handful of transistors. Simulation shows that the proposed circuit consumes very little power and is able to detect the instantaneous energies of different kinds of input signals. Thanks to the compact circuit architecture and the low power consumption, the proposed circuit is a good candidate for local field potential and spike detection.

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