AN ULTRA HIGH-FREQUENCY 8-CHANNEL NEUROSTIMULATOR CIRCUIT WITH 68% PEAK POWER EFFICIENCY

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ABSTRACT

In order to recruit neurons in the targeted tissue, constant-current neural stimulators are usually used. Recently, Ultra High-Frequency (UHF) stimulation has been proposed and proved to have the same efficacy of constant current stimulation [1]. The total number of external components is reduced, while the power efficiency is increased. This leads to a smaller stimulator device with an increased battery life.
The core circuit of the UHF neurostimulator is a DC-DC converter, which generates current pulses. Each stimulation phase is made of a burst of current pulses injected into the tissue at a determined frequency. The amplitude of the pulses is controlled by means of a duty cycle signal.
Here, we present the design guidelines and the IC measurement results of a power-efficient UHF neural stimulator. An overall peak power efficiency of 68% is achieved when 8 independent channels with 16 fully configurable electrodes are used. The only external component is an inductor. It is operated in a time-interleaved fashion across all the activated channels. A novel zero-current detection scheme is proposed. It does not require the freewheel diode usually used in DC-DC converters to prevent current flow from the load back to the inductor. A gate-driver circuit is implemented. It allows to use thin gate oxide transistors as high voltage switches. By doing so, the external high voltage supply, usually used in neural stimulators, is avoided and the neurostimulator is powered from a 3.5 V input voltage. Both the current-detection technique and the gate-driving circuit allow to boost the power efficiency by 300% when compared to previous implementations of high-frequency neural stimulators [1], [2]. The circuit is implemented in a 0.18 μm HV CMOS process, and the total chip area is 3.65 mm^2.

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EMBEDDING SMALL ELECTRONIC COMPONENTS INTO TINY FLEXIBLE IMPLANTS

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ABSTRACT

Electronic components in the form of application-specific integrated circuits (ASICs) establishing the communication between the body and the implant, such as stimulation and recording, have, nowadays, become essential elements for current and future generations of implantable devices, as medicine is looking into substituting its traditional pharmaceuticals with electroceuticals, or bioelectronic medicines [1].

Protection of implant components inside the body is a mandatory important step to ensure longevity and reliable performance of the device. The package of the implant should act as a bidirectional diffusion barrier protecting the electronics of the device from body liquids, and also preventing diffusion of toxic materials from the implant towards the tissue. At the same time the implant's outer layer should match the tissue's mechanical properties in order not to cause scar growth around the implant or damage the body.

Current implants do not completely fulfill the desired properties mentioned above, either lacking hermeticity or softness.

In this work, an embedding process developed at Fraunhofer IZM [2] and used in the semiconductor packaging field for chip encapsulation is proposed to be modified and used for protecting implantable ASICs. Such a method will have a number of advantages, such as miniaturization, in comparison with conventional titanium case packaging. Furthermore, embedding allows to avoid long interconnects, which can be a crucial problem for the device implanted inside a constantly moving body. The other advantage is that the geometry of these interconnects can be well controlled, and the amount of contact pads can be higher than in widely used wire bonding technology, because the distribution of solder bumps during embedding can take place on the whole chip area.

In the proposed process, biocompatible polymer materials, such as ParyleneC and Polyurethane, together with thin glass films will be employed to provide the implant with the required hermeticity and at the same time flexibility. The developed embedding process technology will ensure homogeneous distribution of mechanical stresses, resulting in high reliability for uninterrupted long-term use of smart implants.

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MICROELECTRODE ARRAY (MEA) MEASUREMENTS FROM HUMAN INDUCED PLURIPONTENT STEM CELL-DERIVED NEURAL CULTURES FOR PSYCHIATRIC DISORDERS

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ABSTRACT

The pathophysiology of many neurological and psychiatric diseases remains undiscovered, due to our limited understanding of the biological mechanisms underlying these disorders. Induced pluripotent stem cell (iPSC) technology provides the unique opportunity to study neural cell cultures of individual patients *in-vitro* [1], thus enabling to assess the physiology of psychiatric disorders.

Several protocols used to obtain iPSCs-derived neuron subtypes, networks or whole brain organoids, expose low efficiency, often resulting into immature neuronal cultures. In addition, the conventional adoption of co-cultures, especially with exogenous mouse astrocytes, increases variability. Growing human iPSCs-derived neural cultures from a common neural progenitor cell (NPC), has shown to improve the differentiation efficiency [1]. NPCs are differentiated into functional neural network cultures of neurons and astrocytes in a controlled ratio, without the need of exogenous astrocyte co-culture [2]. Monitoring of the differentiation process is conventionally performed by patch clamp recordings. Single-cell patch clamp measurements, however, do not reveal network behaviour during the differentiation process, which is a critical aspect in potentially assessing the biological mechanisms of psychiatric disorders [1].

In this work, we combine the simplified neural differentiation protocol with the use of microelectrode arrays to record and stimulate neural activity at the network level during differentiation period using a MEA system (Multi Channel Systems)[1]. Measured cell culture data is analysed using a commercial analysis software (Multiwell-Analyzer), to assess spontaneous and stimulated network activity, synchronicity and bursting activity during a developmental phase.

Long-term characterisation of human iPSC-derived neural network cultures using MEA recordings helps us gain more detailed knowledge for the biological mechanisms that underlie neuropsychiatric disorders, for phenotype screening and for the development of personalized treatment and drugs with medium-throughput capacity.

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CO-INTEGRATION OF FLIP-TIP PATCH CLAMP AND MICROELECTRODE ARRAYS FOR IN-VITRO RECORDING OF ELECTRICAL ACVITY OF HEART CELLS

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ABSTRACT

The patch clamp has been widely considered the gold standard to measure intracellular ionic activity of single cells [1]. However, patch clamping is a laborious method and suffers from low throughput. To mitigate the disadvantages of patch clamping, planar patch clamp (PPC) chips with higher throughput have been recently introduced [2-3]. Yet those microfluidic chips do not allow to concurrently monitor the extracellular and the intracellular activity of the cells. Understanding of the complex cellular network activity and electrochemical processes, requires correlation between local field potentials (LFPs) of a population of cells and action potentials (APs) of single cells.

This abstract presents a novel CMOS compatible microfluidic system that integrates flip-tip planar patch clamps (FTPPCs) and microelectrode arrays (MEAs) on the same wafer, for in-vitro extra- and intra-cellular recordings of electrical activity of cardiac cells.

The device is fabricated using conventional wafer front- and back-side photolithography. The fabrication process leverages anisotropic wet etching selectivity of potassium hydroxide (KOH) and deep reactive ion etching (DRIE) to pattern FTPPCs. Before DRIE process, plasma-enhanced chemical vapor deposition (PECVD) of silicon dioxide (SiO_2) is applied as passivation layer. After DRIE process, a metallization step is performed by sputtering titanium nitride (TiN) on patterned structures. As the final step, SiO_2 is removed and backside DRIE is used to open apertures approximately with 2 µm diameter. The FTPPCs are intended to have a tip in 20 µm depth after KOH etching, and a spacing of 200 µm to ensure that mechanical stability of the device after DRIE. The planar MEAs are then patterned on the front side with 50 µm diameter and a pitch of 200 µm.

A PDMS culture chamber is attached the front-side of the wafer, while a PDMS microfluidic channel is constructed on the back-side. By applying suction through the microfluidic channels, the cells are trapped in the FTPPC apertures. Potentiostatic measurements are used to record the ionic activity of the cells intracellularly, while low-noise instrumentation amplifiers are used in combination with the MEAs, to concurrently measure LPFs.

Co-integration of PPC and MEAs on the same wafer can provide valuable insight in the correlation between single-cell activity and cellular network dynamics of heart cells in healthy and pathological states.

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ENERGY EFFICIENT SAMPLING AND CONVERSION OF BIO-SIGNALS USING TIME-MODE CIRCUITS

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ABSTRACT

With the continuous developments in science and engineering, specifically in the fields of electronics and manufacturing, implantable electronic devices have become a reality during the last decades. Implantable electronic devices have hard design constraints: 1) As small size as possible to reduce tissue damage, 2) Minimum heat generation to protect the surrounding tissue, and 3) Minimum energy dissipation as these devices are mostly operated using a small battery or wireless power transfer.

The advancement and scaling of CMOS technologies has always been based on improving the performance of digital systems. With each new technology node, the threshold voltages of the available MOS transistors and the supply voltage of the process node is scaled as well. Scaling of the supply voltage reduces the headroom that is available to the transistors for operating in the region. Even though reducing the supply voltage reduces the energy dissipation, without transistors operating in the saturation region, it is very hard to realize signal processing and amplification functions in the analogue domain.

To address the mentioned hard constraints of implantable electronic device design, we propose time-mode circuits for energy efficient sampling and conversion of bio-signals in advanced process technologies. The types of circuits we are proposing benefit both from voltage scaling and smaller size of advanced process nodes while being able to process digital signals with analogue accuracy, i.e., time-mode circuits represent an analogue signal by the time difference between two binary switching events. For example, when compared to standard digital CMOS circuit operation, to transfer N bits of data in parallel, the number of switchings required may change from 0 to N in standard CMOS, while it always takes time-mode circuits two switching if the rising and falling edges of a pulse is used for signal representation.

Based on these observations, we designed a bio-signal sampling and conversion system that consists of an analogue-to-time converter (ATC) followed by an asynchronous time-to-digital converter (A-TDC). The ATC converts the sampled bio-signal to a time-pulse with a high analogue-to-time conversion gain, and the A-TDC resolves this generated pulse to a digital value, completing the sampling and conversion process. We will present the design process and simulation results of such an implementation that operates with a supply voltage of 0.6V in a standard 0.18um process.

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LAB-ON-CHIP DEVICE FOR HIGH-THROUGHPUT MULTI-ANALYSIS SINGLE-CELL STUDIES

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ABSTRACT

Lab-on-chip (LoC) devices embody several key features, including the use of small sample volume, control over fluid dynamics, easy integration of cell manipulation techniques (cell sorting, cell isolation) and higher throughput than conventional analytical methods (e.g. patch clamp) [1-2]. Impedance flow cytometry (IFC) has been widely adopted for high-throughput cell detection and manipulation, sorting and counting. IFC works by measuring the impedance between a set of electrodes as single cells pass through a microchannel [3]. IFC, however, allows only for short-term single-cell analysis. Microelectrode arrays (MEAs) are often used to perform long-term analysis of cell populations. Coupled with electrical impedance spectroscopy (EIS), adhesion, morphology, proliferation and temporal evolution of cells can be analysed [4].

In this work, a novel LoC device is proposed, which integrates in-channel IFC and in-chamber MEAs in the same microfluidic platform. The microfluidic chip is fabricated on standard Si wafers through a CMOS-compatible photolithographic process, allowing for future microelectronics integration. Several versions of the chip are realized on the same Si wafer, diced and singularly tested to evaluate the effect of the geometrical parameters and channel configuration on the detection sensitivity. The first design includes IFC electrodes of different sizes at the bottom of a 10x10 μm^2 microchannel, and a culture chamber comprising of 9 microwells with interdigitated electrodes. Different IDE parameters (width from 10 μm to 100 μm, gap from 5 μm to 20 μm) are also realized to assess optimum geometries for high sensitivity and SNR.

The IFC and MEA electrodes are characterised using a multichannel impedance analyser. The performance of the microfluidic device is tested in a fluidic system with microbeads of different sizes (4-6-8 μm).

Integration of IFC and MEAs in the same platform enables automated, high-throughput single-cell sorting and manipulation and long-term network analysis, allowing for more comprehensive studies of cell cultures.

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TOWARDS AN ACTIVE GRAPHENE-PDMS IMPLANT

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ABSTRACT

Neural interface in the form of microelectrodes are used to monitor and treat spinal cord injury and other neurological disorders by the means of recording and stimulation. Despite of the apparent result of these electrical interventions, understanding of the mechanism behind neural stimulation is still inadequate. The use of optical monitoring during implantation is limited due to the use of opaque electrode partially blocking the implantation site. While the use of transparent conductor for electrode is not uncommon in general electronics where indium tin oxide (ITO) is widely used for displays, however ITO is not suitable for implantation due to its brittle nature[1].

An alternative material to fabricate transparent electrodes is graphene, a single layer of carbon atom forming sp^2 hybridization. Its high charge mobility, flexibility, mechanical strength and optical transparency make it suitable for various flexible electronics applications including implantable microelectrode arrays. In biomedical fields, graphene has shown potential application as biosensor, stimulation and recording electrode[2].

Although fabrication of graphene microelectrodes has been previously shown[3], graphene had to be transferred manually for each individual implant. The high temperature needed during graphene deposition makes device fabrication directly on the flexible material impossible. Instead, the fabrication process relies on a transferring process of graphene layer from growing medium with high thermal budget to another desired substrate. Manual transfer process of graphene is a skill-dependant process with low scalability.

In this work, a method of fabricating encapsulated graphene electrodes in polydimethylsiloxane (PDMS) with a controlled wafer-scale graphene transfer is proposed. Graphene transfer is done by wafer-assisted PDMS-PDMS bonding to minimalize operator dependency. The novel use of PDMS as encapsulation material for graphene electrode is due to its biocompatibility, flexibility and optical transmittance.

Difference in material characteristics, such as the thermal expansion coefficient has become one of the challenges during fabrication process. Despite of these challenges, the prospect of transparent implant has been shown in preliminary testing on optical transmittance of graphene layer on PDMS with up to 77% transmittance in the visible light spectrum. While full characterization of the device is still in progress, further results will be reported during the conference.

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POLYMER-ENCAPSULATED SINGLE-CHIP IMPLANTS FOR BIOELECTRONIC MEDICINE

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ABSTRACT

The main goal of bioelectronic medicine is to, one day, replace conventional chemical drugs with miniaturized implants. This way, tiny electrical pulses will be locally delivered to a small group of neurons in order to influence and modify biological functions. Developing such implants, however, has brought many new challenges both in the technological and biological domains. One technical challenge, is packaging such tiny deceives in a way that protects the sensitive electronics inside from the harsh body environment [2], while, at the same time ensures certain flexibility that allows the implant to conform to the surrounding soft tissue.

Conventionally, medical implants have relied on a titanium (Ti) or ceramic box to protect the inside electronics. Driven by the increased functionality offered by CMOS technologies and the need for further miniaturization, in recent years tremendous efforts have been made in designing miniaturized implants by integrating the majority of components on a single chip [3]. Such a single-chip approach, however, would require novel packaging solutions since the box would consume greater volume compared to the chip and greatly limit the flexibility of the implant. Polymer encapsulation could be an alternative packaging solution which meets the physical constraints needed for bioelectronic medicine [1-2].

One main drawback of polymeric encapsulation, however, is the eventual penetration of water through the polymer. For this purpose, extensive efforts have been carried out on finding thin multi-layer coatings that could delay water and ion penetration and thereby, increase device lifetime [3]. Despite the increased protection offered by these layers, it has been shown that device lifetime can still be reduced when exposed to high electric fields. For example, the authors of [4] have found that continuous DC biasing of the device reduced the lifetime by a factor of 13 compared to a state where the devices were idle.

In this research, we intend to work towards a single-chip implant by investigating the effect of different electric fields on device lifetimes in soak conditions. For this aim, test structures have been fabricated in standard CMOS technologies and currently being tested in saline. More detailed and up-to-date results will be shared during the conference.

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TOWARDS A SEMI-FLEXIBLE PARYLENE-BASED PLATFORM TECHNOLOGY FOR ACTIVE IMPLANTABLE MEDICAL DEVICES

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ABSTRACT

Active implantable medical devices have been developed for diagnosis, monitoring and treatment of large variety of neural disorders. Since the mechanical properties of these devices need to be matched to the tissue, soft materials, such as polymers are often preferred as a substrate [1]. Parylene is a good candidate, as it is highly biocompatible and it can be deposited/etched using standard Integrated Circuit (IC) fabrication methods/processes. Further, the implantable devices should be smart, a goal that can be accomplished by including ICs. These ICs, often come in the form of additional pre-packaged components that are assembled on the implant in a heterogenous process. Such a hybrid integration, however, does not allow for size minimization, which is so critical in these applications, as otherwise the implants can cause severe damage to the tissue. On the other hand, it is essential that all components are properly packaged to prevent early failure due to moisture penetration [2].

In this work we use a previously developed semi-flexible platform technology based on a Parylene substrate and Pt metallization, which allows integration of electronic components with a flexible substrate in a monolithic process. We use an IC fabrication-based platform that allows for the fabrication of several rigid regions including Application-Specific Integrated Circuits (ASICs) and other components connected to each other by means of flexible interconnects. We aim to add more functionality to this technology and thereby extend it to a platform for a variety of medical applications. An example of such functionality is integrating Light Emitting Diodes (LEDs) for optogenetic stimulation or integrating Capacitive Micromachined Ultrasound Transducers (CMUTs) for ultrasound stimulation or ultrasound wireless power transfer. Since the long-term reliability is critical for implantable devices, we intend to reinforce our implant with an extra Polydimethylsiloxane (PDMS) encapsulation layer that relies on the low viscosity of the uncured rubber to flow in every detail of the surface to prevent void formation [3]. Therefore, this work also focuses on enhancing the adhesion of PDMS to Parylene, as it must remain strong for the required lifetime of the device.

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DESIGN AND CUSTOM FABRICATION OF A SMART TEMPERATURE SENSOR FOR AN ORGAN-ON-A-CHIP PLATFORM

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ABSTRACT

Incubators in cell cultures are used to grow and maintain cells under optimal temperature alongside other key variables, such as pH, humidity, atmospheric conditions etc. As enzymatic activity and protein synthesis proceed optimally at 37.5 ºC, a temperature rise can cause protein denaturation, whereas a drop in temperature can slow down catalysis and polypeptide initiation [1].

Inside the incubator, the measurements are gauged according to the temperature of the heating element, which is not exactly the same as that of the cells. Time spent outside the incubator can greatly impact cell health. In fact, out-of-incubator temperature and its change over time are unknown variables to clinicians and researchers, while a considerable number of cell culture losses are attributed to this reason.

To accurately monitor the temperature of the culture throughout cell growth, an in situ temperature sensor with at least ±0.5 ºC of resolution is of paramount importance. This allows the growth of the cultured cells to be optimized.

This work reports on the design and fabrication of a time-mode signal-processing in situ temperature sensor customized for an organ-on-a-chip (OOC) application. The circuit was fabricated using an in-house integrated circuit technology that requires only 7 lithographic steps and is compatible with MEMS fabrication process. The proposed circuit is developed to provide the first out-of-incubator temperature monitoring of cell cultures on an OOC platform in a monolithic fabrication. Measurement results on wafer reveal a temperature measurement resolution of less than ±0.2 ºC (3σ) and a maximum nonlinearity error of less than 0.3% across a temperature range from 25 ºC to 100 ºC.

To the authors' best knowledge, no in situ temperature-sensing fully integrated on an OOC platform exists to date. This is the first time such integration is being performed using a custom-designed circuit fabricated on the same silicon substrate as that of the OOC. The simple, robust, and custom IC technology used for the sensor fabrication grants a very cost-effective integrated solution in virtue of the reduced cost per wafer along with the large silicon area available on the platform [2]. Moreover, no further complicated assembly and subsequent protection of the pre-fabricated components is required. This minimizes the extra processing steps, along with the related handling risks, leading to higher yields. Finally, the freedom enjoyed by the MEMS-electronics co-design offers a large degree of versatility to accomodate electronics in a range of different OOC shapes and structures.

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DESIGN OF A MULTI-FUNCTIONAL SMART OPTRODE FOR ELECTROPHYSIOLOGY AND OPTOGENETICS

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ABSTRACT

Optogenetics is a neuromodulation method that holds great potential for the realization of advanced neuroprostheses due to its precise spatial-temporal control of neuronal activity [1]. The development of novel optogenetic implants (optrodes) may open new doors to investigate complex brain circuitry and chronical brain disorders, such as epilepsy, migraine, autism, Parkinson's disease, etc [2]. Design challenges for the optrode include interference minimization between the μLED drivers and the recording electrodes, selection of proper materials, structures and dimensions to minimize tissue damage, biocompability, and batch production.

In this work, we propose the construction of a multi-functional optrode to be used for physiological studies in group-housed, freely-moving rodents. It comprises commercial blue-light μLEDs for optical stimulation, an active electrode array for recording the local field potentials at different depths in the brain, and a time-domain temperature sensor.

To accomplish this, silicon bulk micromachining is the essential technique used for the device manufacturation. Process steps include epitaxial growth, layers deposition, geometrical etching, ionic implantation, oxidation and diffusion.

For the interconnection of the μLEDs, flip-chip bonding is used. Light intensity and frequency can be controlled via a microcontroller interface assembled on a flexible PCB mounted on the rodent head-stage. The active microelectrode array (MEA) is constructed from a Ti/TiN layer to both meet the biocompatibility requirements and to reduce the electrode-tissue interface impedance, and by this the associated thermal noise. Using a custom, simple, robust and cost-effective BiFET in-house IC technology, the recording amplifiers are monolithically integrated into the MEA to achieve a high signal-to-noise ratio (SNR) and to minimize potential crosstalk coming from the μLED drivers.

Using the same BiFET IC technology, a time-domain temperature sensor is monolithically integrated into the optrode to anticipate possible brain tissue temperature changes of more than 1ºC that may come from heat dissipation in the μLEDs or circuit power dissipation.

Finally, the optrode is coated with a PDMS film to electrically protect the μLEDs from the tissue and avoid uncontrollable electrical stimulation of the brain tissue.

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SIGNAL SPECIFIC SAR ADC FOR MULTI-CHANNEL ATRIAL ELECTROGRAM SIGNAL ACQUISITION

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ABSTRACT

Atrial electrograms (AEGs) are the signals recorded on the surface of the heart and can be used to study the signal propagation in the atria with an aim to understand the development and progression of atrial fibrillation, which is a type of cardiac arrhythmia. AEGs are acquired using a high resolution electrode array which pose strict constraints on the power and area consumption of the data acquisition system. For a single channel, a dedicated analog-to-digital converter (ADC) is used. However, this approach becomes hardware intensive as the number of channels increase. Multi-channels closely spaced together acquire AEGs that are slowly varying in time, and also share similarities in terms of amplitudes values. Digitizing the signals acquired from every electrode in a multi-channel acquisition system generates a large amount of redundant data. While researchers have attempted to apply various signal specific approaches [1,2,3] such as adaptive resolution ADC, adaptive sampling rate based ADC, a signal specific successive approximation register (SAR) ADC which depends on the difference between the two samples which differ by a few LSBs, a non-linear signal specific SAR ADC, they suffer from being incomplete in the signal data representation and do not account for the redundancies in the spatial domain.

In this work, we aim to exploit the redundancies in space based on the gradient or the difference in the amplitudes of the signals recorded between adjacent electrodes. Firstly, signal characteristics of the AEGs are extracted from the available sample data. The difference in the amplitudes between different channels at a given time instant is calculated and is averaged over many time instants. From a probability density function curve, the mean difference in amplitude and the variance over the entire array is obtained. Based on the values, we define a threshold to activate a high resolution or a low resolution operation mode of the ADC. We aim to develop a signal specific algorithm and circuit architecture using a SAR ADC, that accounts for the changes in the spatial domain to arrive at an energy and area efficient multi-channel data acquisition design for AEGs.

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THE INFLUENCE OF SOFT ENCAPSULATION MATERIALS ON THE WIRELESS POWER TRANSFER LINKS EFFICIENCY

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ABSTRACT

As the era of Bioelectronic medicines (BEms) evolves, new technological challenges are generated, including miniaturized devices that are encapsulated with flexible materials and energized by wireless power transmission (WPT) techniques. Among them, magnetostatic, also known as inductive, and ultrasound (US) are the most viable candidates for shallow and deep applications, respectively. However, the conductive nature of the human tissue with high relative permittivity increases the parasitic components of the printed spiral coils (PSCs), while the acoustic impedance mismatch between the tissue and ultrasound transducers leads to power losses in the WPT link.

This study focuses on the influence of biocompatible, soft, polymeric materials, such as polydimethyloxane (PDMS) and Parylene-C, on the electrical behaviour of the aforementioned externally powered receivers. Unlike previous works, this investigation includes the high gas permeability property of polymers, predicting the electrical impact of moisture absorption. Analytical and simulation models are utilized to discriminate the effect of various packaging schemes and to relate their influence on the WPT link efficiency. Lastly, empirical measurements in air and saline aim to verify the proposed methods.

Early modelling results demonstrate that when a PSC is encapsulated with 50 μm PDMS and submerged into saline, its resonance frequency and quality factor are decreased by 3.6% and 34.2%, respectively. That renders the maximum theoretical WPT link efficiency to be reduced by 9%, compared to free-space propagation in air. Interestingly, when the coating thickness increases to 500μm, the WPT link efficiency drops only by 2.4%.

In the case of US, similar effects are predicted, yet the influence of the coating materials will be different. More specifically, their acoustic impedance decreases the US transducers' natural frequency of vibration and mechanical quality factor, due to the effect of added mass. In addition, when the coating thickness increases towards the wavelength of the incident US wave inside the material, the aforementioned effects become more evident.

The outcome of this study aims to address the contributing factors on the WPT link power losses from the electronics packaging perspective and to suggest on how the effect of the surrounding medium could be mitigated, improving the WPT link efficiency.