Activity Dependent Multichannel ADC Architecture using Level Crossing Quantisation for Atrial Electrogram Recording

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***Abstract*—This paper presents a novel multichannel level-crossing (MLC) ADC architecture aimed at recording atrial electrograms from multiple channels. The proposed architecture combines synchronous sampling with level-crossing (LC) quantisation to achieve activity dependent operation while recording from multiple channels simultaneously. In the proposed architecture the number of comparisons performed by the quantiser to reach a decision is dependent on the activity of the input signal and is 2-3.3 times lower than that in a conventional SAR ADC. The architecture uses one comparator and one reference level instead of two comparators and two reference levels as in conventional LC ADCs. The proposed architecture is modeled in VerilogA and is designed to be implemented in a standard 0.18 um CMOS process. The MLC ADC converts signals from 4 channels simultaneously and achieves an SFDR of 53.33 dB and an SNDR of 48.96 dB while consuming 9.32 μW of power from a 1.8 V power supply.**

***Index Terms*—event-driven, level crossing, asynchronous, biosignal acquisition, multichannel LC ADC, atrial electrogram**

I. Introduction

Atrial electrograms (AEGs) are recorded from the atrial myocardium to help in deeper diagnosis of the atrial fibrillation condition. The recording is performed by using a patch of 192 electrodes [1]. The current setup uses a 3 m long cable to transmit the acquired signals to an analog front end (AFE) and suffers from the fact that noise and interference can corrupt the signal. To mitigate this, an IC-based AFE is required that can be placed near the electrodes and can thus prevent corruption of the acquired signals.

The AEGs behave similar to regular (surface) electrocardiograms (ECGs) as they have high-amplitude peaks in between time intervals of low activity, making the signals sparse in the time domain. Conventional nyquist rate ADCs sample the input signals at a constant rate irrespective of signal activity and thus do not exploit the temporally sparse property of certain biosignals such as AEGs, ECGs, etc. Asynchronous ADCs such as LC ADCs (shown in Fig. 1(a)) exploit the signal sparsity by waiting for an event to happen (such as the signal crossing over a reference level) instead of sampling it at regular intervals [2]. However, LC ADCs are not compatible with discrete time signal processing (DSP) blocks [3]. Also, they produce higher amounts of data as compared to nyquist rate ADCs, especially at the higher resolutions that are required for signals with high dynamic range such as AEGs [4].

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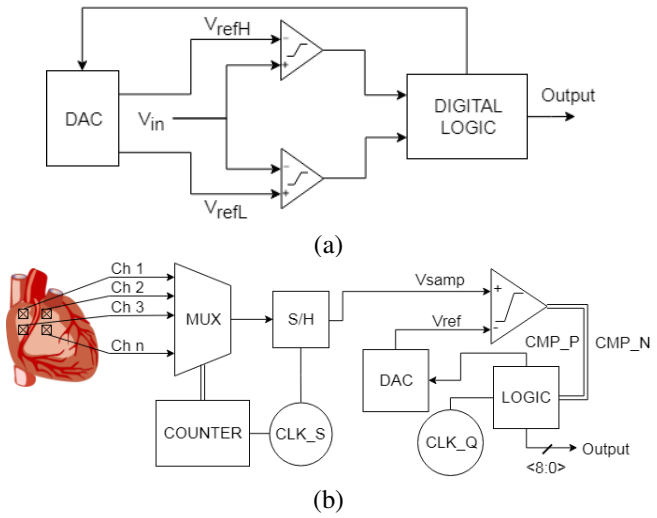

Fig. 1. Block diagram of (a) a conventional LC ADC architecture and (b) the proposed multichannel LC ADC architecture.

Multichannel ADC topologies have been reported in literature, which can be used in the AFE for recording AEGs [5]. The existing multichannel ADCs however are not activity-dependent. LC ADCs are a better choice here as their operation is activity dependent. Currently, multichannel configurations of LC ADCs do not yet exist.

In this paper we propose the novel MLC ADC architecture shown in Fig. 1(b), which combines features of both synchronous and asynchronous recording methods. The signal is acquired synchronously as is done in nyquist rate ADCs. Then the sample is quantised using the level-crossing sampling approach, which makes the quantisation process activity-dependent. Multiple channels are sampled simultaneously by time-multiplexing the ADC across the channels. The quantisation process is configured based on the signal activity. This approach reduces the average number of comparisons required per sample for quantisation of AEGs by up to 3.3 times.

The system design and modelling of the proposed MLC ADC architecture are explained in Section II. The circuit implementation is described in Section III. The simulation

results are discussed in Section IV. Finally the conclusions are discussed in Section V.

II. Proposed Architecture

In this section the system-level design considerations and modelling of the proposed MLC ADC architecture are discussed.

A. System Design

In conventional LC ADCs (Fig. 1.(a)), the reference window consists of two reference levels to which the input signal is compared. The reference window follows the input signal as it tries to keep the current value of the input signal within the reference window. Conventional LC ADCs track the signal continuously and generate events when a level crossing is detected. Although this method is signal-driven, it is not power-efficient as the continuous-time comparators draw power all the time. Moreover, the LC ADCs operate in continuous time and hence cannot be configured to convert signals from multiple channels simultaneously, as is done in synchronous ADCs, without increasing the data rate and power consumption considerably. Sampling the input signal synchronously and quantising the sample using level-crossing quantisation allows the conversion to be signal-driven and reduces power consumption as well. Rather than counting the number of LSB steps crossed by the sample from the mean level (half of the common mode input range), the highest reference level crossed by the previous sample is used as the starting point of quantisation for each sample.

Conventional SAR ADCs and similar synchronous ADCs use a fixed number of steps to quantise the sample but in the proposed method the number of steps required is signal-dependent. If the current sample is at the same amplitude level as the previous sample, the quantisation is completed after just two comparisons. In the worst case, the number of levels counted would be equal to 2^N where N is the resolution of the quantiser. However most of the high-amplitude contents of biosignals occur at lower frequency ranges, as shown in the FFT plot of an AEG in Fig. 2.

Hence, the average number of steps required for quantisation of each successive sample in the proposed method would be less than that in conventional synchronous sampling methods. This assumption is verified with MATLAB models, which show that the proposed method can reduce the number of comparisons required by 2-3.3 times depending on the target resolution of the quantiser (10 bit - 8 bit, respectively). The number of comparisons required for conversion of a typical AEG with 8-bit resolution is shown in Fig. 3. The model samples the AEGs at 1 kS/s from each channels for 10 s. Thus a total of 10000 samples are quantised from each channel. The plot also shows that the number of comparisons in the proposed method increases and approaches the number of comparisons required in the multichannel SAR algorithm at higher resolutions. Thus, for lower resolutions the proposed method has an advantage over the conventional SAR algorithm.

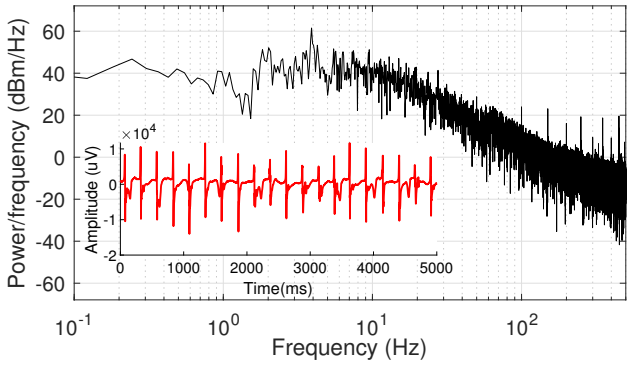

Fig. 2. Power spectral density of AEG (inlay: AEG). Data Courtesy: Erasmus MC, Rotterdam [1]

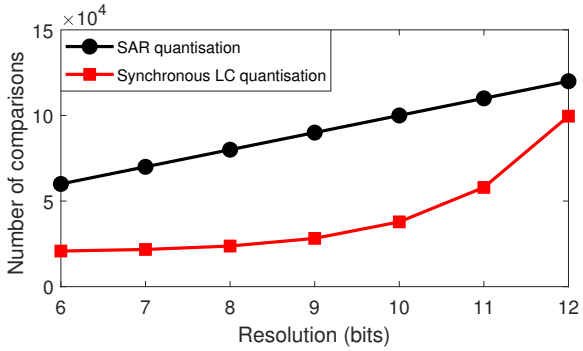

Fig. 3. Estimation of number of comparisons performed by the quantiser for quantisation of AEGs by using the SAR algorithm and by using the proposed method in a MATLAB model for 10 s of conversion.

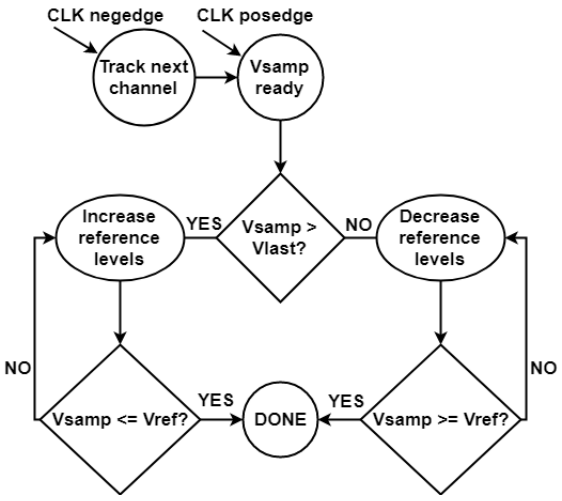

Fig. 4. Flowchart of operation of proposed multichannel LC ADC architecture.

The flowchart of the operation of the proposed MLC ADC architecture is shown in Fig. 4. At the positive edge of CLK, a sample is captured in the Sample & Hold (S/H) block and the highest reference level crossed by the previous sample is loaded in the DAC and compared with the sample. If

the sample has a higher amplitude then the reference level is increased by 1 LSB and compared again. This process continues until the sample amplitude is under the reference level and the comparator output is changed. The highest reference level reached is given as output. The final reference level is then used as the starting point for the quantisation of the next sample. Multiple channels are sampled with the same ADC by time-multiplexing the S/H. The digital logic stores the output of the first comparison of each sample and uses it to reach the end point of quantisation. Moreover, each channel has a set of registers to store the reference level after completion of the quantisation of its corresponding sample.
The clock speed required for quantisation is determined by the signal activity and time required for each conversion. The maximum number of steps covered by the quantiser for each sample is estimated through VerilogA models and thus the clock speed is set to cover the worst case. The requirement for a clock signal for quantisation can be obviated by implementing an asynchronous quantisation method [6].

B. VerilogA modelling

A model of the proposed MLC ADC architecture is developed in VerilogA to verify its functionality. The model is used to convert an AEG and the output is used to reconstruct the AEG in MATLAB. The LSB step size for the conversion is 1mV. The input signal and the quantised samples are shown in Fig. 5. The lower plot of Fig. 5 shows the number of LSB steps covered by the quantiser for each sample. For most of the samples, the number of steps covered is nearly zero since the signal does not change considerably for most periods of time. The maximum number of steps to be covered for a specific signal can be estimated through this model.

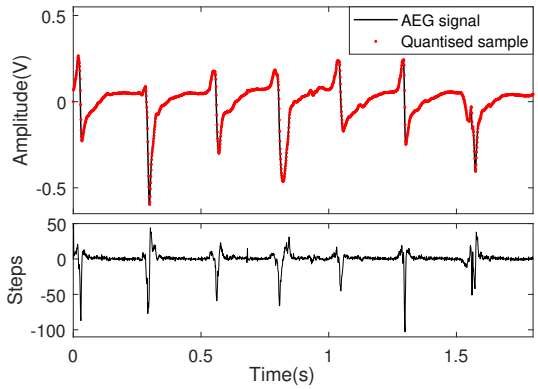

Fig. 5. Waveform showing input AEG waveform and quantized samples in VerilogA model of the proposed MLC ADC architecture. The lower plot shows the number of LSB steps covered by the quantiser for each sample.

III. Circuit Implementation

The proposed MLC ADC architecture is designed to be implemented in TSMC's 0.18 um CMOS process. The ADC supports conversion from 4 channels simultaneously at a resolution of 8 bits.
A S/H block is implemented with a 1 pF hold capacitor. Two transmission gates are used to switch between the 'track' and 'hold' phases. An 8-bit DAC is implemented in binary-weighted configuration with a unit capacitor of 35.6 fF.
The S/H is multiplexed with several channels by using a counter to select the channel number and NMOS transistors as switches. Since the sampling frequency is 1 kS/s, the counter increments at 4 kHz and thus selects the subsequent channel for sampling every 250 ms.
A strong-arm dynamic latch with a PMOS input pair is used for the comparison such that the common mode input range is within 0-1.2 V for a power supply of 1.8 V. A preamplifier is used to reduce kickback noise [5].
The control logic block is designed in Verilog and synthesized using the Synopsys Design Compiler. The control logic uses a 1.6 MHz clock signal to synchronize the quantisation. The speed of the quantisation clock signal is calculated after estimation of the maximum number of steps that need to be covered for quantisation of the AEG from the VerilogA model, as discussed in the previous section. The control logic stores the output of the first comparison for each sample and uses this value to determine the end point of quantisation of the sample. A separate memory is used to store the final reference level of each channel and thus the signal in each channel is tracked separately. The signal SW<0:7> is used to load the reference level in the DAC for each comparison. A simplified schematic of the whole ADC is shown in Fig. 6. The timing diagram of operation of the quantiser is shown in Fig. 7. CLK_Q is used to synchronise the quantiser while CLK_S is used to synchronise the S/H block. The DAC_SET and CMP_EN signals are used to control the DAC and the comparator, respectively. After quantisation is completed for a specific sample the DONE signal is set. When the next sample is ready, DONE is reset and quantisation starts again.

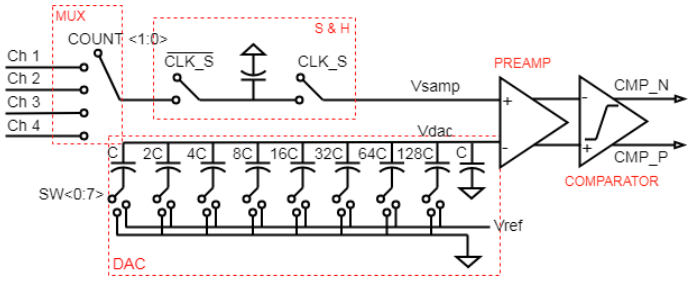

Fig. 6. Circuit schematic of the implemented design of the proposed MLC ADC architecture.

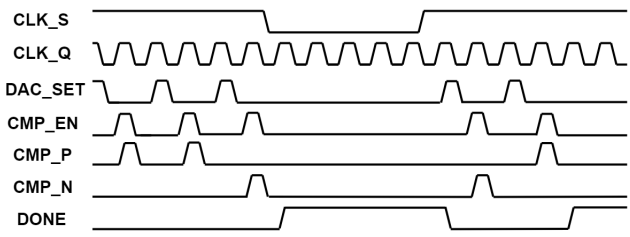

Fig. 7. Timing diagram of operation of the proposed MLC ADC.

IV. Results and Discussion

The transistor-level implementation of the ADC is tested with sinusoidal input signals with V_{p-p} = 1.2 V at 125 Hz on all input channels with a delay of 120 μs between each channel. The signals are sampled at 1 kS/s and the quantisation is performed at 2 MHz while considering the maximum number of steps required by the quantiser to be 100, which is much higher than actually required. The quantized output is used to reconstruct the signal in MATLAB through spline interpolation. The input signals and the quantised samples are shown in Fig. 8.

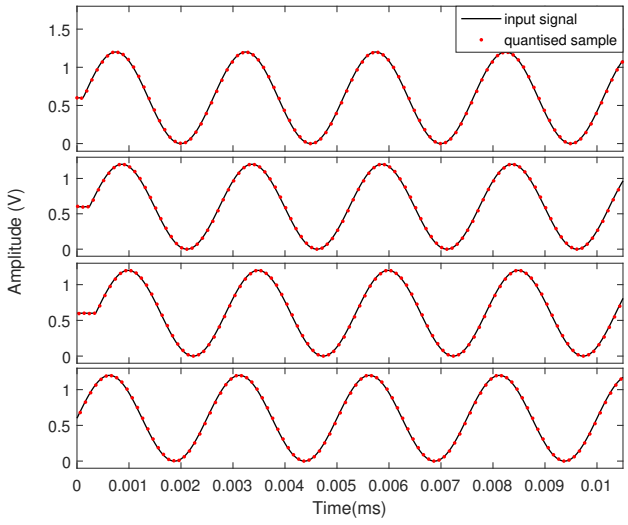

Fig. 8. Reconstructed signals from 4 multiplexed channels.

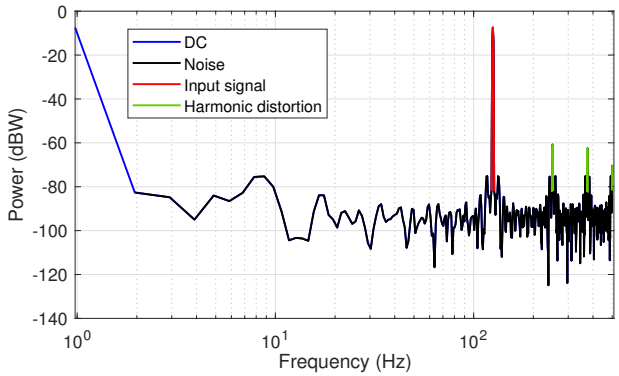

Fig. 9. Output spectrum of the proposed MLC ADC for a 125 Hz sinusoidal input at f_s = 1 kS/s.

The implemented design converts signals from 4 channels simultaneously and achieves an SFDR of 53.33 dB and an SNDR of 48.96 dB (Fig. 9) while consuming 9.32 μW of power. As shown in Fig. 8 the input signal is reconstructed successfully from the output of the ADC. Similarly, AEG signals were converted in the MLC ADC with a quantisation clock frequency of 2.4 MHz. The power consumption measured in the simulation was 7.58 μW, which illustrates the activity-dependent operation of the ADC. The power consumption is reduced even while using a higher quantisation clock frequency. The proposed MLC ADC architecture is scalable and hence the number of channels, resolution, sampling rate and quantisation time can be reconfigured according to the application requirements. Unlike the conventional LC ADCs in which the amount of data generated doubles with every extra bit of resolution, the proposed MLC ADC produces only 'n' bits of data at the sampling frequency. The differences between conventional ADC architectures and the proposed ADC architecture are summarised in Table 1.

TABLE I
Comparison of Architectures

Feature	***LC ADC***	***Synchronous ADC***	***Proposed MLC ADC***
Activity dependent	Yes	No	Yes
Multichannel	No	Yes	Yes
Comparators	2	1	1
Operation	Asynchronous	Synchronous	Synchronous
Data rate (max)*	$\frac{2\pi f.Vmax}{Vref}$	F_s	F_s
Data volume (bits)#	2	n	n

* Here f refers to bandwidth of the input signal, Vmax refers to maximum input signal amplitude and F_s refers to sampling rate.
# Here n refers to resolution of the ADC

V. Conclusion

The proposed MLC ADC architecture combines synchronous sampling with level-crossing quantisation and is demonstrated using a VerilogA model and transistor-level simulations. The motivation behind the design of the architecture and its benefits are discussed. The MLC ADC achieves lower data rate as compared to conventional LC ADCs and it is shown that for AEG signals the number of comparisons required by the MLC ADC is reduced by 2-3.3 times as compared to conventional multichannel SAR ADCs.

References

[1] A. Yaksh et al., A novel intra-operative, high-resolution atrial mapping approach, J. Interv. Card. Electrophysiol., vol. 44, no. 3, pp. 221225, 2015.

[2] S. Patil, A. Ratiu, D. Morche and Y. Tsividis, "A 3–10 fJ/conv-step Error-Shaping Alias-Free Continuous-Time ADC," in IEEE Journal of Solid-State Circuits, vol. 51, no. 4, pp. 908-918, April 2016.

[3] B. Schell and Y. Tsividis, A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation, IEEE J. Solid-State Circuits, vol. 43, no. 11, pp. 24722481, Nov. 2008.

[4] Y. Li, D. Zhao, and W. A. Serdijn, A sub-microwatt asynchronous level-crossing ADC for biomedical applications, IEEE Trans. Biomed. Circuits Syst., vol. 7, no. 2, pp. 149157, 2013.

[5] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, The 128-channel fully differential digital integrated neural recording and stimulation interface, IEEE Trans. Biomed. Circuits Syst., vol. 4, no. 3, pp. 149161, 2010.

[6] P. Harpe, E. Cantatore, and A. Van Roermund, A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/conversion-step, IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 30113018, 2013.