A 0.8V 8-Bit Low-Power Asynchronous Level-Crossing ADC with Programmable Comparison Windows

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***Abstract*— We propose a low-power asynchronous level-crossing analog-to-digital converter (LC-ADC) for use in a biomedical readout system. A comparator with programmable offset and a low-power single-bit digital-to-analog converter (DAC) are proposed to separate the comparison windows and fix the common-mode voltage of the comparator. Implemented in a 0.18 µm CMOS technology, the proposed LC-ADC uses a chip area of 220×230 µm^2. Operating from a supply voltage of 0.8 V, the ADC input range can exceed the power supply voltage. It consumes 0.32 - 0.84 µW from 5 Hz to 5.1 kHz with an ENOB of 7.8.**

I. INTRODUCTION

Application in wireless body area networks pushes the power consumption of wearable and implantable wireless biomedical readout sensors further to their limits. So far, there is little research on circuit and system design techniques that take advantage of the signal characteristics. Generally, the highest expected frequency of the input signal determines the system operation bandwidth and speed, and thereby the power consumption. Operating the whole system at its maximum rate regardless of the possible sparsity of the input signal results in a waste of energy. Running the system at an adaptive rate according to the input signal activity may lead to considerable power savings.

In order to make the readout system adaptive, the frequency and amplitude information of the normal and abnormal excursions of the input signals need to be extracted and be continuously available to adjust the whole system. Such information, available from an activity monitoring block, can be used to control the data transmission rate, the ADC sampling rate, the biasing current of the analog blocks, the gain of the programmable-gain amplifier (PGA) and so on. In some previous works, window comparator based activity monitors can be found in adaptive sampling for data compression [1] and adaptive DC level control for motion artifact compensation [2]. But the operation of these monitors are triggered by clocks, which are usually much slower than the highest possible ADC sampling rates. Therefore, they are not able to truly continuously monitor the whole range of input signals over the complete input bandwidth.

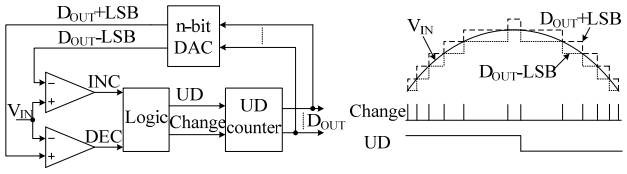

Fig. 1. Conventional LC-ADC and its example waveform.

One possible implementation of a continuous monitoring block is the even-driven asynchronous level-crossing (LC) ADC [3-9]. The conventional system structure of an LC-ADC and an example waveform are shown in Fig. 1. Basically, two identical comparators are used to compose the comparison window. The DAC together with the digital logic and the up/down (UD) counter are employed to form a feedback loop to track the input voltage. The sampling of the LC-ADC is triggered by signal crossings of specified levels, resulting in event-driven operation [3-5]. Such a structure requires fast power-hungry comparators to accommodate the input common-mode (CM) voltage variation over the entire input range. Improved from this structure, [3-9] focused more on the implementation of the n-bit DAC with adaptive resolution or a single-bit DAC to fix the CM voltage and decrease the loop delay. To date the reported LC-ADCs still consume microwatt power and are not suitable for low-power biomedical readout system design. In this paper, we propose a low-power and low-area LC-ADC with innovations at both the architecture level and the circuit level. In Section II, we analyze the possibility of lowering power consumption and propose solutions at system level. Section III introduces the circuit implementation. Measurements are presented in Section IV, followed by the conclusion in Section V.

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II. System Architeture

Normally, a window with an upper and a lower level is necessary for level-crossing detection. However, the structure with two identical comparators as found in previous LC-ADCs or in any window comparator application does not consume its power efficiently, because the input signal only approaches one level at a time, so only one comparator is active for detection while the other one is always idle. To further save power from the idle comparators, the conventional symmetrical comparison window has to be modified.

The proposed LC-ADC and an example waveform are shown in Fig. 2. Instead of tracking the input within the dynamic range by two n-bit DACs, two single-bit DACs with charge sharing are adopted to track and perform the addition or subtraction to the differential input signal whenever there is a level crossing. Two comparators with additional logic and a multiplexer (MUX) are combined. The lower comparator detects the polarity of the input signal ($V_{ON} > V_{OP}$ or $V_{ON} < V_{OP}$), and controls the MUX to switch between (V_{OP}, V_{ON}) and (V_{ON}, V_{OP}) in such way that the lower one of (V_{OP}, V_{ON}) is always connected to the negative input of the upper comparator. With the purposely introduced built-in offset (V_{OS}) at the negative terminal of the upper comparator, the input at the negative node becomes level shifted up by V_{OS}. Now there are three signals: V_{OP}, V_{ON} and V_{OFS} (V_{OP} or V_{ON} plus V_{OS}). The lower comparator compares the original differential input (V_{OP}, V_{ON}), while the upper one compares V_{OFS} with V_{OP} (or V_{ON}).

In this way we create two comparison windows: the one

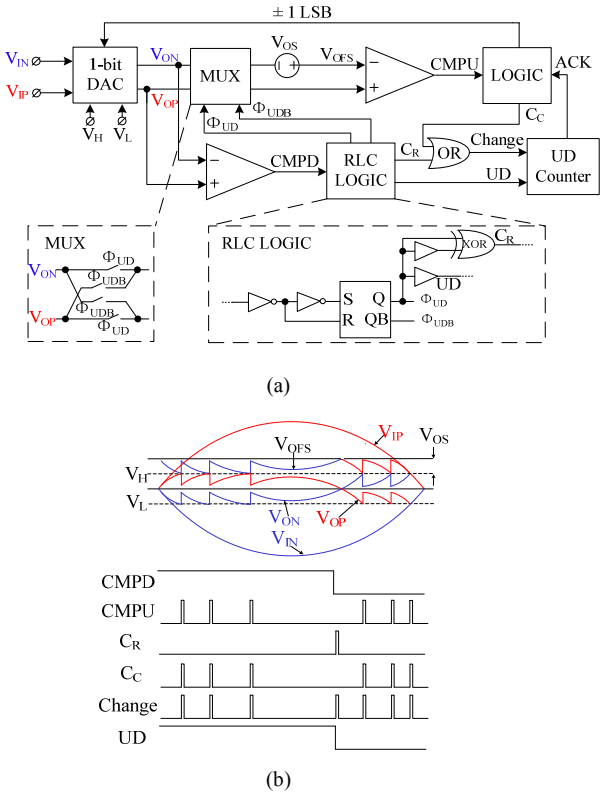

Fig. 2. (a)Proposed LC-ADC (b)its example waveform.

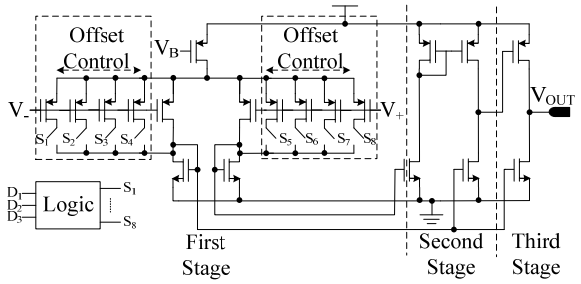

Fig. 3. Continuous comparator with build-in offset

with solid lines for the upper comparator and the one with dotted lines for the lower comparator (Fig. 2(b)). The size of 1 LSB is thus equal to the upper window. Whenever V_{ON} and V_{OP} cross each other, the lower comparator senses that and switches the two inputs for the upper comparator. So the level-crossing detection is split with the upper comparator detecting level crossings and the lower comparator detecting direction changes. Depending on the frequency of occurrence of the two different crossings, different supply power can be allocated to the comparators. Consequently, with two separate comparison windows, more flexible design of the comparator is enabled and power consumption can be lowered.

III. Circuit Implementation

A. *Comparator with built-in offset*

As a LC-ADC operates continuously, there is no clock for offset cancellation. In previous works, offset was compensated by either applying a compensating DC level at the input [4], or DACs to tune the offset [5-6]. However, we make explicit use of the offset in this work and further introduce the imbalance in the comparator input pair. The comparator with built-in offset is shown in Fig. 3. The input stage comprises a pMOS input pair loaded by nMOS diodes. The transistors in the dotted box are from the additional input pair to introduce the imbalance in the main input pair. Three bits (D_1-D_3 in Fig. 3) are used to digitally control the value of the offset (V_{OS}). The width of the each pMOS transistor of the additional pair is eight times smaller than the one in the main pair. nMOS switches are used at the drain of the pMOS input pair. A programmable offset ranging from -20 mV to 23 mV was obtained from the measurements.

There are two signal paths from V_- to V_{OUT}: the one via the second stage is for gain enhancement while the one via only the third stage is for speed enhancement. Considering the two inputs of the upper comparator, V_+ is always lower than V_- when the signal stays within the comparison window. Therefore, the third stage does not consume static power as the pMOS is shut down by the output of the second stage when $V_- > V_+$. Only when the V_+ is approaching V_- the third stage starts to draw current from the power supply. The lower comparator uses similar structure but with hysteresis.

B. *1-bit DAC*

The proposed 1-bit DAC is shown in Fig. 4. Only one DAC is shown for simplicity. nMOS transistors are utilized as switches. The DAC here is a combination of a charge pump

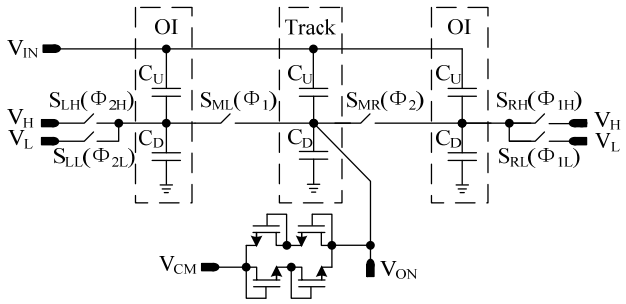

Fig. 4. Proposed 1-bit DAC.

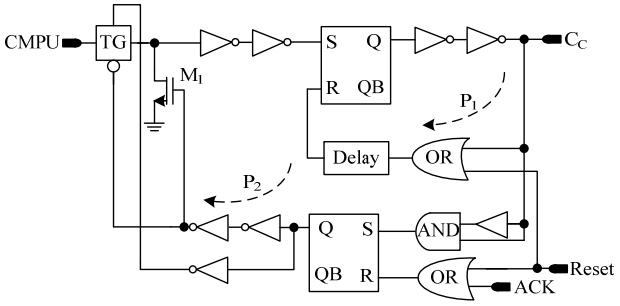

Fig. 5. Asynchronous logic.

and a tracking circuit, injecting an offset voltage while tracking the continuous-time input. Offset injection in the two-branch structure in [9] or resetting buffer in [7] requires a certain settling time for resetting. In this work, three identical branches in the capacitor array are designed. As a consequence, the settling time requirement of the three-branch structure is relaxed considerably. The detailed operation principle can be found in [8].

C. Asynchronous logic

The asynchronous logic control circuit is shown in Fig. 5. CMPU is the output signal from the upper comparator. ACK is the acknowledgement signal from the U/D counter. Reset is for resetting the asynchronous logic at the conversion start up. C_C is the output pulse to the next stage that processes the level-crossing conversion.

When there is no level crossing, the transmission gate (TG) is on and the NMOS M_1 is off. Whenever there is a signal crossing about to happen, the output of the comparator will start to rise. As soon as the comparator output (CMPU) crosses the threshold of the following two inverters, the upper SR trigger is set and its output is changing from "low" to "high". Then, there are two paths controlling the subsequent operation. For the lower path (P_2), the rising edge of the C_C pulse is detected by the detector (AND and the delay chain). The logic AND outputs a pulse that sets the lower SR trigger. Consequently, the TG is switched off and M_1 is switched on to pull the drain node to ground. The comparator output is then disconnected from the asynchronous logic. For the upper path (P_1), the delayed rising edge comes then and resets the SR

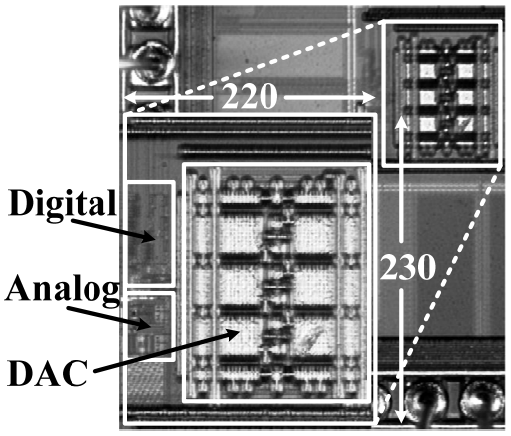

Fig. 6. Chip micrograph. The active area is approximately 220×230 μm^2.

trigger. The delay time is determined from the system requirements. The entire asynchronous logic is disabled until the pulse of the acknowledgement (ACK) from the next stage arrives. When ACK goes high, all the blocks are reset to the normal operation mode to wait for the next level crossing.

IV. Measurement Results

The proposed LC-ADC has been implemented in AMS 0.18 μm CMOS technology. Fig. 6 shows the chip micrograph. The active area is approximately 220×230 μm^2. All the blocks shown in Fig. 3 were included on the chip. We set 1 LSB equal to 15 mV for all measurements. Since level-crossing sampling is non-uniform sampling, signal reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. A logic analyzer was used in the measurements for counting the time in between two samples.

As the LC-ADC is an event-driven converter, it is worthwhile to measure to what extent the power consumption of the LC-ADC varies for different input signals. Fig. 7 depicts the power consumption as a function of the input frequency and amplitude, respectively. In Fig. 7 (a), an 800 mV_{PP} sinusoidal signal, its frequency swept from 5 Hz to 5.1 kHz is used. Due to the structure of the DAC, the input range of the LC-ADC can exceed the power supply. For the reliability of the device, a maximum input up to 2.25 V was used. The power consumption for a 0.45 kHz sinusoidal input signal ranging from 50 mV to 2.25 V is shown in Fig. 7 (b). The total power consumption of the ADC increases with input frequency and with input amplitude. The analog power consumption dominates at low frequencies and amplitudes while the digital power consumption increases with frequency and amplitude. Fig. 8 shows the measured spectrum of the ADC output for a 5.1 kHz input signal. The logic analyzer sampling frequency equals 10 MS/s and a reconstruction sampling frequency of 102.4 kS/s and 1024 points were used to derive the spectrum. The SNDR degradation is mainly due to offset accumulation and slope overload. The low frequency distortion can be corrected by digital filtering or by introducing a mixed-signal loop [10]. A performance comparison is summarized in Table I. The proposed LC-ADC achieves sub-microwatt power consumption while maintaining small area and moderate accuracy.

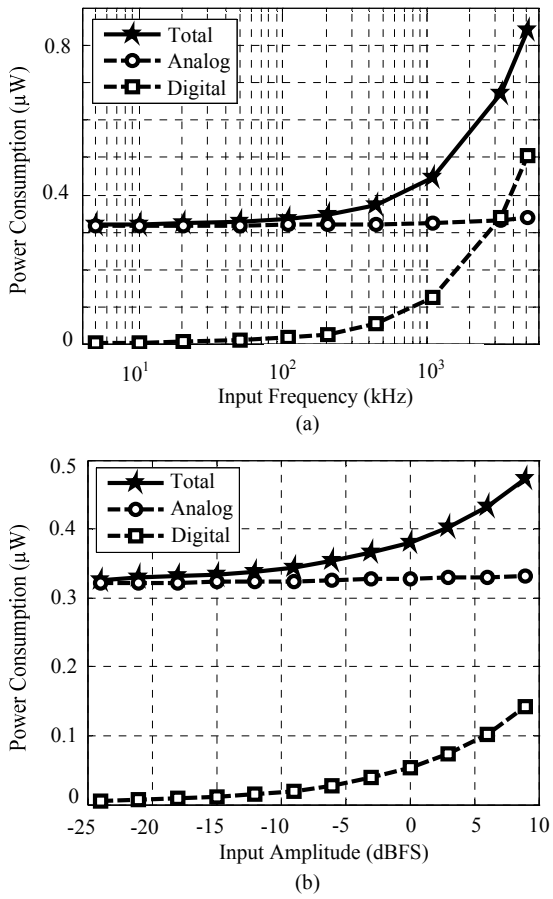

Fig. 7. (a) Power consumption as a function of input frequency ranging from 5 Hz to 5.1 kHz, for a 0.8 V_{PP} input signal. (b) Power consumption as a function of input amplitude ranging from 50 mV to 2.25 V, for an input frequency of 0.45 kHz.

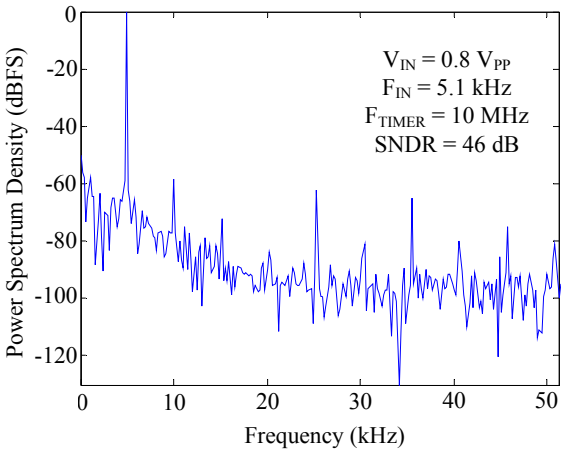

Fig. 8. FFT of the measured ADC output for a 5.1 kHz sinusoidal input, using 1024 points reconstructed at 102.4 kS/s. A 6th order polynomial interpolator was used to reconstruct the signal.

TABLE I. PERFORMANCE COMPARISON

	[4]	[5]	[6]	[7]	[8]	This work
Technology (nm)	90	180	130	500	180	180
Supply Voltage (V)	1	0.7	0.8	3.3	0.8	0.8
Adaptive Resolution	No	Yes	Yes	No	No	No
Automatic Calibration	No	No	Yes	No	No	No
SNDR (dB)	47-62	Peak 43.2	47-54	Peak 31	Peak 49	Peak 49.4
Input Bandwidth (kHz)	0.2 – 4	0.001 - 1.1	0.02 – 20	0.2-5	0.005 – 3.3	0.005 – 5.1
Full-Scale Input (V_{PP})	0.5	1.4	0.72	2.68	1.6	2.25
Power Consumption (µW)	40 @DC	25 @1kHz	2.6 - 7.4	106 @1kHz	0.31 - 0.58	0.32 - 0.84
Active Area (mm^2)	0.06	0.96	0.36	0.06	0.045	0.05

V. CONCLUSION

A LC-ADC employing a novel level-crossing detection mechanism has been presented. The innovations at both system and circuit level lead to low-power operation for the LC-ADC. The low power and low area, together with the event-driven operation, pave the way for integrating asynchronous LC-ADC in biomedical applications for system monitoring.

REFERENCES

[1] R.F. Yazicioglu, S. Kim, T. Torfs, H. Kim and C. Van Hoof, " A 30 µW analog signal processor ASIC for portable biopotential signal monitoring," *IEEE JSSC*, Vol. 46, No. 1, pp. 209-223, Jan. 2011.

[2] S. Hong, S. Lee, T. Roh and H.J. Yoo " A 46 µW motion artifact reduction bio-signal sensor with ICA based adaptive DC level control for sleep monitoring system" in *Proc. IEEE CICC*, 2012, pp. 1-4.

[3] E. Allier, J. Foulier, F. Sicard, A. Dessani, E. Ander and M. Renaudin, " A new class of asynchronous A/D converters based on time quantization", in *Proc. IEEE ASYNC*, May 2003, pp. 196-205.

[4] B. Schell and Y. Tsividis, " A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation," *IEEE JSSC*, Vol. 43, No. 11, pp. 2472-2481, Nov. 2008.

[5] M. Trakimas and S. R. Sonkusale, " An adaptive resolution asynchronous ADC architecture for data compression in energy constrained sensing applications," *IEEE TCAS-I*, Vol. 58, No. 5, pp. 921-934, May 2011.

[6] C. Weltin-Wu and Y. Tsividis, " An event-driven, alias-free ADC with signal-dependent resolution," in *Proc. IEEE Symp. VLSI Circuits*, 2012, pp. 28-29.

[7] W. Tang et. al, " Continuous time level crossing sampling ADC for bio-potential recording systems," *IEEE TCAS-I*, Vol. 58, No. 99, pp. 1-12, May 2013.

[8] Y. Li, D. Zhao and W. Serdijn, " A sub-microwatt asynchronous level-crossing ADC for biomedical applications," *IEEE TBioCAS,* Vol. 7, No. 2, pp. 149-157, Apr. 2013.

[9] Y. Li and W.A. Serdijn, " A continuous-time level-crossing ADC with 1-bit DAC and 3-input comparator" in *Proc. IEEE ISCAS*, 2012, pp. 1311-1314.

[10] R. Mohan, S. Hiseni and W.A. Serdijn, " A Highly Linear, Sigma-Delta Based, Sub-Hz High-Pass Filtered ExG Readout System" in *Proc. IEEE ISCAS*, 2013, pp. 181-184