A Sub-GHz UWB Pulse Generator for Wireless Implantable Medical Devices

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***Abstract*—The design of a MOS-only pulse generator for sub-GHz Ultra-Wideband (UWB) biomedical communication is presented. The oscillator based pulse generator is capable of generating Binary Phase Shift Keying (BPSK) modulated pulses and is tunable in both frequency and output power. A varactor biasing circuit is developed that keeps the varactor bias voltage constant during oscillator startup and shutdown. The pulse occupies a bandwidth of 550 MHz. The center frequency can be controlled from 0.53 to 1.05 GHz and the digital gain control offers a 13.5 dB tuning range. For a 2.5 V supply and 1 MHz Pulse Repetition Frequency (PRF), the average power consumption ranges from 30 μW to 150 μW, depending on the pulse power controlled by the digital gain. The circuit performance is very robust over process corners, device mismatch and antenna reactance variations.**

***Index Terms*—Sub-GHz, UWB, Pulse Generator, Biomedical, Implantable, Antenna, Wireless**

I. Introduction

Implantable medical devices equipped with wireless communication can improve the treatment of medical disorders and thus improve the quality of life. Today's wireless biomedical communication such as inductive coupling and narrow band communication do not meet all requirements such as reliability, power efficiency and wireless range. An alternative solution thus has to be found.

Sub-GHz UWB biomedical communication may be a good candidate to reach all of these requirements. In previous work [1] it was found that the best tissue penetration is achieved at sub-GHz frequencies and that for this particular application a *current* driven antenna results in the most reliable information transfer. This paper is a follow-up of the work in [1] and discusses the design of a sub-GHz UWB pulse generator capable of efficiently driving an implantable antenna that suffers from considerable antenna reactance variations.

In Section 2 the pulse generator topology is discussed, followed by the circuit design in Section 3. The designed pulse generator performance is verified with circuit simulations in Section 4. Finally, this paper ends with conclusions.

II. Pulse Generator Topology

Three important requirements for an implantable chip are low power consumption, small chip area and reliability. Inductors should therefore be avoided in the design because of their large chip area and poor Q-factor for sub-GHz frequencies. This already eliminates some pulse generator topologies such as passive filter structures and LC oscillators. An active filter based pulse generator would be an alternative but usually requires too much power (> mW) [2].

A simple and low power approach is to make use of the antenna frequency characteristics to shape a rectangular or quasi-Gaussian pulse [3], but this principle cannot be used in this design due to the non-predictable properties of the implantable antenna [1].

An alternative pulse generator topology is based on combining different pulse phases that are generated using NAND, NOR and delay blocks [4]. Disadvantage is that accurate delay blocks are required for a robust pulse generator, as any variation in the delay blocks will change the pulse shape.
Oscillator based pulse generators have drawn much attention lately because of their low area, low complexity, robustness and energy efficiency. The main principle of this pulse generator is explained with the aid of Figure 1.

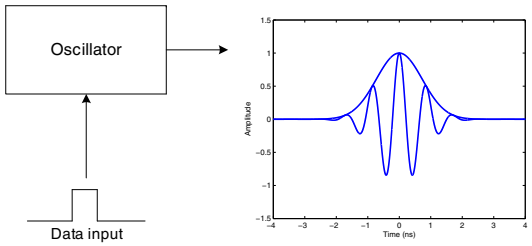

Figure 1: Oscillator based pulse generator principle.

By switching the oscillator on and off, the amplitude will follow the attack and release time constant of the oscillator. This generates an UWB pulse that occupies a bandwidth dependent on the time duration of the data input. In [5], the use of a relaxation oscillator as pulse generator was proposed. These oscillators can operate at high frequencies, occupy small chip area and are stable over process variations. They also suffer from poor phase noise performance, but this is acceptable in UWB systems. We therefore will investigate a relaxation oscillator as basis for our pulse generator.

III. Circuit Design

The first part of the circuit design involves a circuit analysis of the relaxation oscillator. The second part deals with the circuit implementation of the pulse generator.

A. Oscillator analysis

A MOS relaxation oscillator with two diode-connected transistors as load is depicted in Figure 2. These transistors implement a reasonably linear resistance of $R \approx 1/g_{mR}$, even for large signal swings. The reason why we choose nMOS

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instead of pMOS as load will become clear later. We will start the circuit analysis by calculating the startup condition.

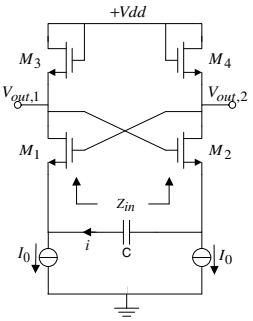


Figure 2: MOS relaxation oscillator.

Startup condition: Assuming that M_1 is identical to M_2 and M_3 to M_4, one can find that for this circuit the input impedance seen from the capacitor is given by [6]

$$Z_{in}(s) = 2\frac{\left(\frac{1}{g_{m0}} - \frac{1}{g_{mR}}\right) + \frac{s}{g_{m0}g_{mR}}\left(C_{gs} + 4C_{gd}\right)}{\left(1 + s\frac{C_{gs}}{g_{m0}}\right)\left(1 + s\frac{4C_{gd}}{g_{mR}}\right)} \quad (1)$$

where all parameters have their usual meaning. After adding the timing capacitor in parallel with Z_{in}, we can obtain the characteristic equation by calculating the roots of $Z_{in}(s)\, sC + 1 = 0$. For sinusoidal oscillation we require the solution for s to be purely imaginary. For the startup condition however, it must be guaranteed that at least one pole lies in the positive halfplane so that oscillations can take place. It then follows that the startup condition can be expressed as

$$g_{m0} > g_{mR}\left(\frac{C + C_{gs}/2}{C - 2C_{gd}}\right) \quad (2)$$

Equation 2 reveals how the startup condition will be affected by process corners. Ideally, the ratio of g_{m0}/g_{mR} should not vary over corners, which suggests to implement the load transistor and the cross-coupled gm cell with the same transistor type (nMOS in this case) so that *all* transistor undergo the same relative variation in g_m. We can minimize the influence of C_{gd} and C_{gs} by choosing $C \gg C_{gs}$ and $C \gg C_{gd}$.

The robustness of the startup condition can be described by introducting robustness factor θ to the equation such that $g_{m0} = g_{mR}\theta$. A safety margin should thus be included to make sure Equation 2 is valid over all process corners such that oscillation will always occur. The robustness factor θ can be set with

$$\theta = \sqrt{\frac{W_0 L_R}{W_R L_0}} \quad (3)$$

Frequency: The oscillating frequency resulting from the roots of the characteristic equation is given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{2KI_0\sqrt{\frac{W_R W_0}{L_R L_0}}}{C\left(C_{gs} + 4C_{gd} + \frac{2C_{gd}C_{gs}}{C}\right)}} \quad (4)$$

where $K = \mu C_{ox}$. We can see from Equation 4 that the frequency can vary significantly over process corners. To compensate for this effect, a suitable parameter in Equation 4 has to be chosen to tune frequency. The bias current I_0 is often used for this, but doing so will also influence the output voltage and power consumption during tuning. Since this is not an attractive solution, we choose to tune capacitor C by means of a varactor.

Amplitude: To find the large signal steady state voltage between the two drains we must first calculate the steady state current i. This can be approximated by $i \approx I_0\sqrt{8\left(1 - g_{mR}/g_{m0}\right)}$ [6]. Since the current through the diode-connected transistor and the cross-coupled pair transistor is the same, we can relate I_0 to g_m by writing $g_m = \sqrt{2KI_0\left(W/L\right)}$. The peak-to-peak differential output voltage in terms of bias current and transistor size then becomes

$$v_{out} \approx \sqrt{16I_0\frac{L_R}{KW_R}\left(1 - \sqrt{\frac{W_R L_0}{W_0 L_R}}\right)} \quad (5)$$

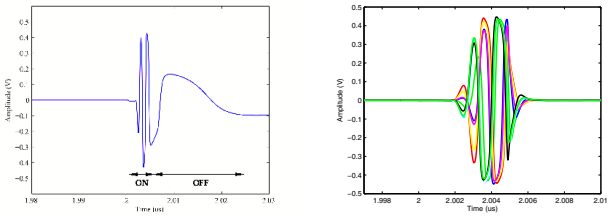
Bias current: If we combine Equations 3, 4 and 5, we obtain the bias current in terms of the oscilator frequency, robustness factor and differential output voltage

$$I_0 \approx \pi f_0 v_{out}\sqrt{\frac{C\left(C_{gs} + 4C_{gd} + \frac{2C_{gd}C_{gs}}{C}\right)}{8\left(\theta - 1\right)}} \quad (6)$$

B. Pulse generating circuit implementation

Generating the UWB pulses is done by switching the current sources with the binary data input. The pulse shape is determined by the attack and release time of the oscillator and the duration of the data input.

Turn-off effects: In contrast to the relaxation oscillator with passive load resistors, this circuit implementation cannot generate pulses without additional circuity because of the increase in load impedance of $M_{3,4}$ when the oscillator is switched off. This increases the oscillator release time constant so that the pulse shape slowely decays to zero after turn-off as shown in Figure 3a. This problem is solved by introducing transistor M7 between the two drains as shown in Figure 4. When this transistor is driven with input D_1 it removes the charge difference from the output nodes, effectively decreasing the release time.



(a) Turn-off effect on pulse. (b) Undefined initial pulse condition

Figure 3: Pulse shape generating design issues.

Other turn-off effects are caused by undefined voltages at the drains of $M_{1,2}$ and $M_{5,6}$ in Figure 4 when the oscillator is switched off. These undefined voltages can cause an offset in the differential output voltage and therefore must be defined using transistors M_{34} and M_{37}. This will guarantee that the differential output voltage equals zero after the pulse is generated, since both outputs will be forced to the supply

voltage. These transistors are driven with input D_2, which is slightly longer in time compared to D_1 so that the pulse shape is not affected by the switching action.

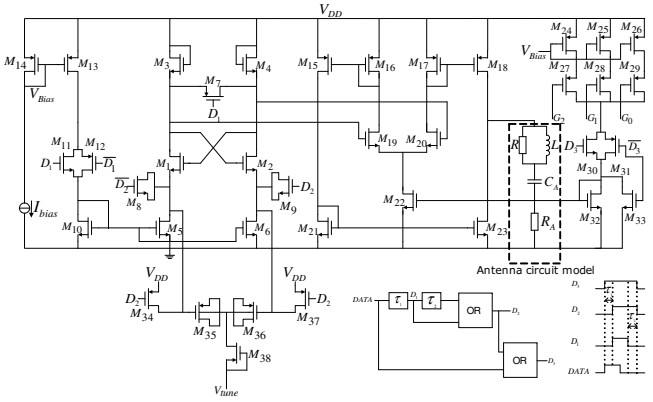


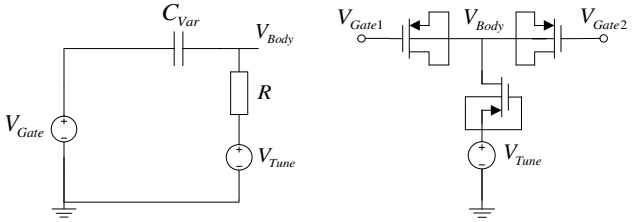
Figure 4: Pulse generator circuit implementation

Defining the initial pulse condition: A perfectly symmetrical relaxation oscillator will only start to oscillate when it becomes unbalanced. In practice, noise and device mismatch will unbalance the circuit and positive feedback will cause the circuit to oscillate. Since these conditions are not well defined, the startup condition is not always the same. This effect can be clearly seen over 10 Monte Carlo mismatch runs in Figure 3b. To overcome this, the initial pulse condition is defined by injecting charge at one side of the circuit to 'push' the oscillator into a defined unbalanced initial state just before the pulse is generated. This is accomplished by transistors M_8 and M_9 in Figure 4.

Realizing BPSK modulation: The concept of fixing the initial condition by injecting charge at one side of the circuit can be used to realize a transmitter capable of transmitting BPSK modulated pulses. By simply injecting charge at either the left side or the right side of the circuit we can generate two types of pulses that are of opposite polarity. This is a very elegant and simple way to implement BPSK since the modulation does not take place in the signal path and the initial pulse condition is already defined *before* the pulse is generated. Note that an additional circuit block is needed to modify the binairy input data such that it can be used to control transistors M_8 and M_9 (not discussed in this paper).

Frequency tuning: The frequency tuning will be done by changing the capacitor C with an accumulation-mode varactor. An additional biasing circuit is required to provide the varactor with a stable bias condition. This can be understood by analysing the varactor gate voltage during startup and shutdown. At the moment the circuit is switched on, the gate voltage of the varactor will drop by $V_{DD} - V_{ds,M5}$ due to M_{34} (see Fig. 4). This will cause a large change in capacitance value since the varactor capacitance is strongly related to its bias voltage. The result is that the oscillator's frequency is changing during startup.

In order to have a constant varactor biasing we need to ensure that V_{bg} remains constant during oscillation. In other words, when the gate voltage of the varactor drops by 1V during startup, the body voltage must also drop by the same



(a) Equivalent circuit (b) Circuit implementation

Figure 5: Varactor biasing.

amount. To understand how we can realize this, we first analyse the simple RC circuit of Figure 5a. The voltage across the capacitor represents the varactor bias voltage $V_{bg} = V_{body} - V_{gate}$. The tuning voltage V_{tune} is a fixed DC voltage and V_{gate} is the varying gate voltage during startup. If we introduce a large resistance R between the transistor body and tuning node, we create a large time constant with capacitor C. When the circuit is switched off, V_{gate} equals V_{DD} and the voltage at V_{body} equals V_{tune}. When the circuit is switched on, V_{gate} will drop from V_{DD} to $V_{ds,M5}$. Since the time constant is much larger than the pulse duration, V_{body} will follow the variations in V_{gate}. The result is that the varactor bias voltage V_{bg} is insensitive to variation in V_{gate}. Figure 5b shows the transistor implementation of the varactor.

Output amplifier: The output amplifier is based on a simple transconductance stage followed by a current-mirror based amplifier that drives the implantable antenna with a current. To reduce power consumption, the amplifier is completely switched off when there is no input data. The tail current of the transconductance amplifier is switched on just before the actual pulse is generated to make sure that the amplifier biasing has settled. Transistor M_{33} helps to define the gate voltage of M_{22} when the pulse generator is switched off. This prevents turn-on effects and also helps to reduce power consumption. The transconductance gain can be controlled by adjusting the tail current with G_0, G_1 and G_2.

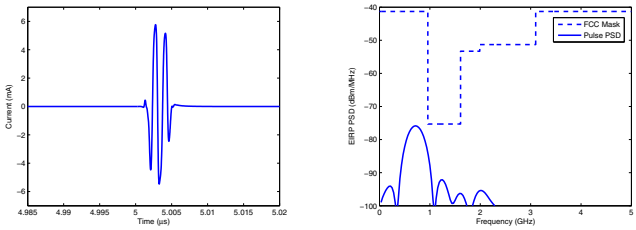
The entire pulse generator circuit implementation is shown in Figure 4. Binary signals D_1, D_2 and D_3 are realized using the input data, two delays and two logic OR ports. The accuracy of the two delay block does not have to be very high since these binary signals are used for the switching action just before and after the pulse is generated. Small variations in the delay will therefore not have a significant effect on the pulse shape. All parameters of the pulse generator can be found in Table I.

IV. Simulation results

The functionality of the complete circuit will now be verified. The circuit is designed using AMIS 0.35μm I3T25 technology and circuit simulations are done using Cadence RF Spectre. The supply voltage is set to $V_{DD} = 2.5$ V to make sure that all transistors operate in strong inversion over all process corners. Furthermore $I_{Bias} = 4\,\mu$A and the data input has a duration of 2.5 ns.

Figure 6 shows the current pulse in the antenna and the corresponding Power Spectral Density (PSD) with the FCC

mask. The pulse occupies a -10 dB bandwidth of 550 MHz centered at 750 MHz. The average power consumption equals 78 μW for a PRF of 1 MHz. Figure 6b shows that the pulse train meets the emission level limits set by the FCC.

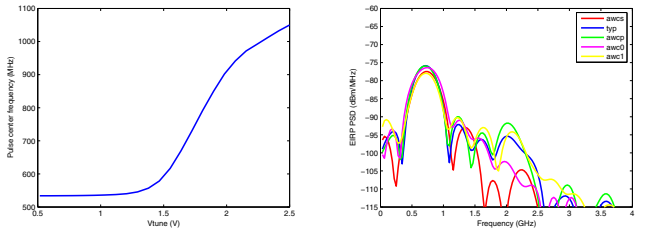


(a) Current pulse in the antenna (b) Pulse PSD and FCC mask

Figure 6: Antenna current pulse and PSD.

The digital gain stage can be controlled over 8 different levels and offers a 13.5 dB tuning range. The average power consumption ranges from 30 μW to 150 μW.

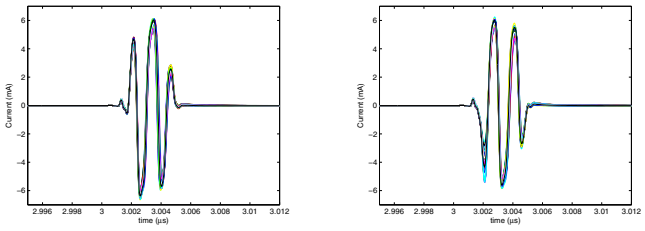
Figure 7a shows the pulse generator frequency tuning in the typical process corner. The varactor covers a tuning range from 530 to 1050 MHz. Figure 7b shows the PSD over all worst case process corners. The varactor is able to reset the operating frequency to 750 MHz for each process corner.



(a) Pulse center frequency f_0 vs. V_{tune}. (b) PSD over process corners

Figure 7: Pulse generator tuning characteristics and PSD over process corners

The effect of mismatch among identically designed transistors is checked with a 200 run Monte Carlo simulation as shown in Figure 8. From this figure we can conclude that the effect of device mismatch on the pulse shape is small and that the two BPSK pulses are well defined.



(a) BPSK '0' (b) BPSK '1'

Figure 8: Monte Carlo simulations (200 runs)

To verify the robustness of this pulse generator against antenna impedance variations, we observe the change in pulse shape while the antenna reactance is varied with the same amount we observed during measurements and simulations (we only vary the reactance since the variation in the antenna resistance is considerably less [1]). This corresponds to the following component values in the antenna equivalent circuit model in Figure 4: $3.5 \leq C_A \leq 5.5$ pF and $5 \leq L \leq 7$ nH, $R_A = 10\,\Omega$ and $R = 400\,\Omega$.

It was found that there is a negligible effect on the pulse shape for these practical variations. The effect of device mismatch and process corners has a much larger influence on the pulse shape compared to the antenna reactance variations. This verifies that the current-driven antenna indeed is a reliable antenna-electronics interface. It not only guarantees that the desired power is always delivered to the radiation resistance, but also allows us to better predict the received pulse shape.

Table I: Pulse generator transistor parameters. Both L and W are expressed in μm.

Transistor	W	L	m	Transistor	W	L	m
$M_{1,2}$	9	0.35	1	M_{21}	8	0.35	1
$M_{3,4,10}$	5	0.7	1	M_{22}	5	0.7	15
$M_{5,6}$	5	0.7	2	M_{23}	8	0.35	15
$M_{7,11,30,34,37}$	2	0.35	1	M_{24}	6	1	8
$M_{8,9,12,31,33}$	5	0.35	1	M_{25}	6	1	4
M_{13}	2	1	10	M_{26}	6	1	2
M_{14}	2	1	1	$M_{27,28,29}$	4	0.35	1
$M_{15,16,17}$	16	0.35	1	M_{32}	5	0.7	1
M_{18}	16	0.35	15	$M_{35,36}$	14	5	1
$M_{19,20}$	14	0.35	1	M_{38}	0.5	0.35	1

V. Conclusions

The designed pulse generator is capable of generating BPSK modulated pulses with a bandwidth of 550 MHz and the center frequency can be controlled from 0.53 to 1.05 GHz. The digital gain control offers a 13.5 dB tuning range. The average power consumption ranges from 30 μW to 150 μW for a 2.5 V supply and 1 MHz PRF, depending on the gain settings. The circuit performs well over all process corners, device mismatch and is very robust against antenna reactance variations. This guarantees that the desired power is always delivered to the radiation resistance and also allows to better predict the received pulse shape, thereby increasing the reliability of the communication link.

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