Design of a low power 100 dB dynamic range integrator for an implantable neural stimulator

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***Abstract*—Neural stimulators are expected to play an important role in the future treatment of a wide range of pathologies. A novel system architecture was presented in which the fundamental quantity for functional electrical stimulation, charge, is controlled by measuring the stimulation current [1]. This sets the need for a current integrator to calculate the injected charge.**

Existing current integrators cannot cope with the specifications for the neural stimulator, including a very high dynamic range, low power consumption and robust enough against process and power supply variations. Therefore a current integrator design is proposed here, which is able to handle a large dynamic range by converting the output to a periodic signal. For this purpose a novel Schmitt trigger design is presented based on a threshold compensated inverter.

The implementation shown here has a dynamic range of 100 dB, while achieving a low static power consumption (171 nW). This makes it suitable for application in an implantable neural stimulator.

I. Introduction

Neural stimulators are expected to become a dominant treatment method for a wide variety of diseases in the future. Presently they have shown to be effective for various pathologies, including Parkinson's disease and tinittus. To increase the effectiveness, a more versatile stimulator is required; especially with more control over the stimulation waveform. Using an alternative for the square shaped pulses available now, tissue habituation is expected to decrease significantly. Furthermore stimulators with a smaller form factor are needed to reduce the impact for the patient, requiring lower power consumption to decrease the battery size.

In [1] the design of a new type of stimulator is proposed based on a double loop feedback voltage based stimulator to meet these requirements. The basic principle is depicted in Figure 1. The starting point for this design was the fact that the fundamental quantity in functional electrical stimulation is *charge*: to either evoke or block action potentials in the tissue, the potential of the tissue is elevated up to a particular threshold by injecting a certain amount of charge. Charge is also important for safety reasons: charge cancellation (no netto charge injection) must be assured to eliminate tissue damage due to electrolysis.

To inject the charge into the tissue, it was chosen to make a voltage based system to maximize the power efficiency. To control the charge the tissue current needs to be sensed and subsequently integrated. This was realized using indirect current feedback: a scaled transistor pair with ratio $1 : N$ ensures that an accurate fraction of the current injected into the tissue is measured and integrated. Because of the indirect current feedback, a second feedback loop was required to control the tissue voltage as shown in Figure 1.

The advantage of the system is that any arbitrary waveform can be injected into the tissue. Irrespective of the voltage waveform chosen, full control over the charge is ensured by sensing the stimulation current. Furthermore, the system is designed such that it operates from positive supply voltages only. Only part of the system operates from a high voltage (up to 18 V) required for stimulation, while the rest can operate using a much lower voltage (around 3 V) to decrease the power consumption.

In this paper the design of the integrator in this system is treated in more detail. It turns out that the integrator has challenging specifications, especially for the dynamic range. In the next section the requirements of the integrator are specified. Subsequently the system level design is treated in Section 3. In Section 4 the circuit design is presented and in Section 5 the simulation results are discussed.

II. System requirements

The integrator is required to integrate a copy of the stimulation current. Its output is a voltage which is a measure of the amount of charge injected into the tissue.

The range of stimulation currents determines the input range of the integrator. Since this system is voltage steered and the impedance of the tissue has a huge spread among patients and time, the stimulation current is not known accurately. Based on the specifications of some existing current source based stimulators (such as found in [2] and [3]), it is found that the stimulation current can range from about 10 μA up to about

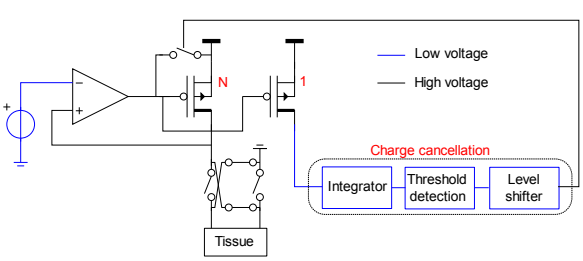

Fig. 1. Overview of the stimulator system

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10 mA. When the integrator current is 1/100 of the stimulation current ($N = 100$ in Figure 1) this yields an input current of 100 nA up to 100 μA for the integrator.

At the output of the integrator is a voltage corresponding to the injected charge. If a constant stimulation current is assumed, the injected charge is easily found to be $Q = IT$ with T the pulse width. Again some specifications of existing systems are used to find that the pulse width might vary between 10 μs up to 1 ms. In the worst case scenario, this would mean that the output can have a dynamic range of 5 decades. Although in practice the high amplitude pulses will most likely have a shorter period, the dynamic range is still very high (clinical values in for example [4] show a range between 90 nC and 8000 nC). This makes the design of the integrator not straightforward: a very high resolution would be required for the output voltage.

Besides dynamic range, additional requirements include sufficiently low power and small area. These requirements go hand in hand with any implantable system: the size and power constraints are very tight. No absolute maximum ratings are specified here: low power consumption and small area are two aspects that are kept in mind during the complete design cycle.

III. Integrator architecture

For almost all implementations of integrators a capacitor is at the heart of the circuit as the integrating element (either in an active or passive implementation). The voltage over the capacitor is a measure for the integrated current: $V = C^{-1} \int idt$. To handle the large dynamic range some form of scaling is required. Looking at the equation, the scaling can be done for i, C and V.

1) i-scaling: First of all the input current can be scaled, before it is fed to the integrator. Inputting only a controllable fraction of the current into the integrator decreases the dynamic range at the input.

2) C-scaling: Scaling in the integrator itself can be achieved by changing the value of the capacitor. When the capacitance is increased, the output voltage will be smaller for the same injected charge. One way to increase the capacitance is by placing multiple capacitors in parallel. The drawback of scaling C is the relatively large area required for linear capacitors.

3) V-scaling: Instead of requiring a high resolution output voltage, it can be converted to another domain. One way to do this is to convert the output voltage into a periodic signal. The output will now consist of a signal for which the frequency is related to the rate of charge injected in the tissue. Each period corresponds to a particular amount of charge: a charge packet. This periodic signal is subsequently fed into a counter to be able to detect a particular number of charge packets.

Because of the large area required for C-scaling the design will only include scaling of the input current combined with the periodic signal converter.

IV. Circuit design

For the complete integrator system both the current divider and the integrator need to be designed. The design of a current divider with a constant attenuation factor over the large input range is not very trivial. Several options exist, including a MOSFET Only Current Divider (MOCD) [5] or scaled current mirrors. The implementation of these circuits will not be discussed in detail in this paper.

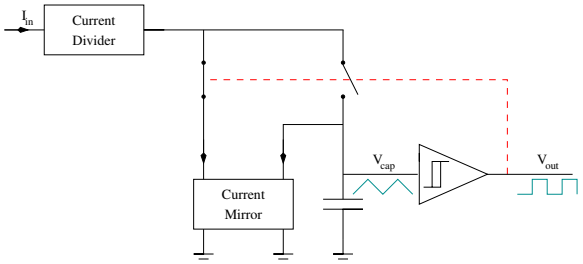


Fig. 2. Integrator system architecture

The integrator and periodic signal converter circuit need to create a periodic signal based on the current injected by the input signal. It was chosen to implement this by switching the integrator voltage between two thresholds. As soon as a threshold is reached, the input current is reversed to integrate towards the other threshold. An overview of the implementation is given in Figure 2. Flipping of the current is done by using a current mirror. The two threshold voltages can be implemented using a Schmitt Trigger circuit.

As can be seen from Figure 2 it was chosen to implement the integrator in a passive way using a capacitor. This offers an easier solution compared to an active implementation and does not consume static power.

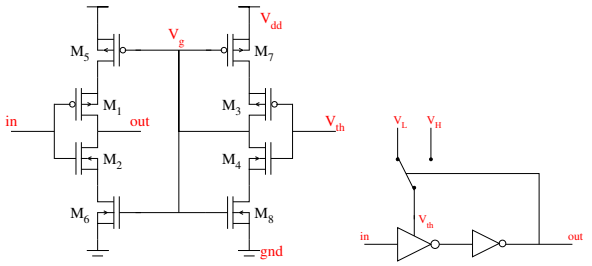
Existing Schmitt trigger designs all have particular disadvantages that make them unsuitable for this application. An opamp based solution has the disadvantage of using a static bias current, which increases the power consumption of the circuit. Other solutions comprising (cross coupled) inverters do not have static power consumption, but are too sensitive to process and supply voltage variations [6].

Therefore a novel design is proposed. The concept is based on the fact that a Schmitt Trigger actually is a comparator with two different threshold levels. At the heart is probably the simplest comparator available: a CMOS inverter.

A. Schmitt trigger based on a threshold compensated inverter

The design proposed here is based on the threshold compensated inverter introduced in [7]. The basic idea is to have an inverter for which the threshold voltage can be set independent of V_{DD} and process variations. In this design the threshold is not only set, it is also varied to construct the functionality of a Schmitt trigger, as a Schmitt trigger is nothing else than a comparator with two threshold voltages.

The circuit implementing the threshold compensated inverter is depicted in Figure 3a. The basic inverter is formed by transistors M_1 and M_2. Transistors M_3 and M_4 are duplicates of M_1 and M_2 with the required V_{th} at their inputs. The output voltage of these transistors, V_g, determines the gate voltage of transistors M_5-M_8. Transistors M_7 and M_8 form a feedback loop with M_3 and M_4 to bias the V_{th} of M_1 and M_2 to the required value using M_5 and M_6. Note that the correct



(a) V_{th}-compensated inverter (b) Schmitt Trigger

Fig. 3. Threshold compensated inverter circuit and its application

working principle of this circuit relies on the matching of transistor pairs M_1-M_3, M_2-M_4, M_5-M_7 and M_6-M_8.

As explained, this circuit can be used in a Schmitt trigger when the threshold voltage is made dependent on the output voltage. This principle is depicted in Figure 3b. The threshold compensated inverter is the first inverter in the chain and has an additional input V_{th}. It is followed by a normal inverter to make the output square shaped.

Subsequently this square shaped voltage is used to control the threshold voltage of the first inverter. The threshold voltages can in principle be freely chosen to be $0 < V_L, V_H < V_{dd}$. The main advantages of this design include its simplicity and the robustness against process variations.

B. Power consumption

When considering the power consumption of the threshold compensated inverter a problem is found. Consider the situation in which the threshold is set at a value close to $0.5V_{dd}$. In this case the inverter M_3 and M_4 is close to its 'natural' threshold, which sets V_g close to $0.5V_{dd}$ as well. Therefore both M_7 as well as M_8 will operate in strong inversion. This means there exists a DC path from V_{dd} to gnd through M_7, M_3, M_4 and M_8, yielding a very high static power consumption. Two possible solutions exist:

- Choose V_{th} to be close to gnd or V_{dd}. In this case the V_{th} set will be far away from the 'natural' V_{th} of the inverter. This means that either M_7 or M_8 will be in weak inversion, yielding a low current. For this particular application, a V_{th} which is close to V_{dd} or gnd is beneficial. In this way the full voltage range of the capacitor is used and therefore the capacitor is used at its maximum efficiency.
- The length of transistors M_5, M_6, M_7 and M_8 can be increased, yielding a lower static current through the right branch of the circuit.

These methods can be used in combination with each other. However, they will have some negative consequences on the performance of the circuit. By increasing the length of transistors M_5 and M_6, the output current will decrease. This will decrease the speed of the circuit: it will take longer to switch the output ((dis)charging the next inverter). Increasing the length also increases the capacitive load at node V_g. This means it will take longer before the V_g required for the new V_{th} is reached. Both effects influence the period and therefore the size of a charge packet.

A redimensioning of the threshold compensated inverter is required. The fundamental reason to increase the length of the transistors was to decrease the current in the right branch of the circuit formed by M_3, M_4, M_7 and M_8. The fact that this also decreased the maximum output current of the circuit was because it was assumed that M_5 and M_6 need to have the same size as M_7 and M_8.

It turns out it is possible to make M_5 and M_6 much shorter than M_7 and M_8 while still achieving sufficient accuracy. Consider the case when V_{th} is chosen close to 0 V. In this case M_7 will be in saturation, while M_8 will be in triode. For the saturated transistor the following equation holds:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \tag{1}$$

Here V_t is the threshold voltage of the transistor. If channel length modulation is ignored, the current I_d is decreased proportionally for an increase in L, irrespective of V_{ds}. For the transistors in triode it holds, assuming $V_{ds} \ll 2(V_{gs} - V_t)$:

$$V_{ds} = \frac{L}{\mu C_{ox} W (V_{gs} - V_t)} I_d \tag{2}$$

This shows that although the L is increased, the saturated transistor makes the I_d decrease with the same factor, yielding the same V_{ds} for the triode transistor. This means V_{th} should still be the same while M_7 an M_8 can be much larger than M_5 and M_6. A similar reasoning can be made for the situation in which V_{th} is chosen close to V_{dd}.

V. Simulation Results

To test the feasability of the circuit, it is simulated in a circuit simulator. The technology used is AMIS 0.35μ High Voltage (25 V), coded I3T25. The simulator software used is the Cadence design enviremont with Spectre. V_{dd} for the low voltage part was set to 3 V, but the circuit can work for lower supply voltages as well.

A. Threshold compensated inverter

First the operation of the redimensioned threshold compensated inverter is verified. In Figure 4 the DC response is given for several values for V_{th}. For the solid lines transistors M_5, M_6, M_7 and M_8 all have $L = 20\,\mu$m, while for the dashed lines M_5 and M_6 were given $L = 1\,\mu$m. As can be seen, the threshold voltages of the symmetrically sized circuit indeed correspond to the values set. For the asymmetrical circuit some obvious deviations are clear. However, the values relatively close to V_{dd} and gnd show only minor ($< 20\%$) deviations. The deviations are explained using some second order effects which were ignored in the equations (the effect of V_{ds} in both the saturated as well as the triode case).

The simulated V_{th} is close enough to the value set by V_{th} and since it is a static deviation, it does not lead to charge mismatch when used in the neural stimulator. This makes it possible to operate this threshold compensated inverter with low power consumption and still making it fast enough to switch. The threshold voltages of the schmitt trigger are chosen to be 0.5 V and 2.5 V. If they are chosen to be even closer to V_{DD} or 0, M_5 or M_6 will be operating in subthreshold, decreasing the output current too much.

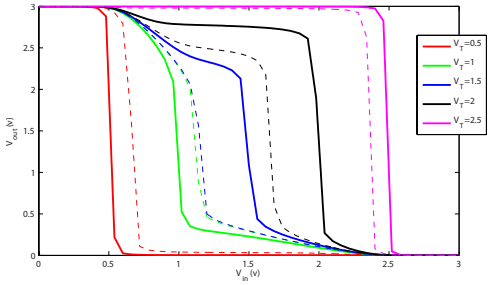


Fig. 4. DC response of the Vt compensated inverter for a symmetric (solid lines) and non symmetric design (dashed lines)

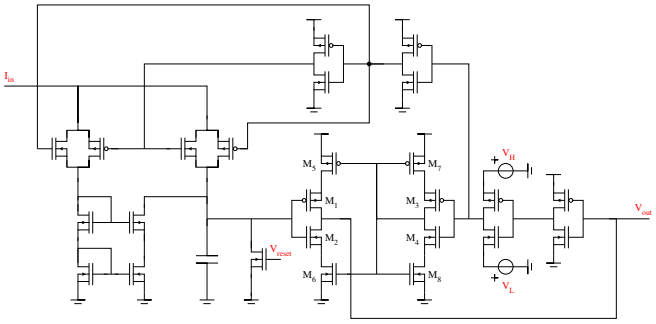


Fig. 5. Complete circuit of the integrator

B. Integrator

Subsequently the complete integrator circuit as depicted in Figure 5 is simulated. It is assumed that the current divider will decrease the maximum input current towards $1\,\mu$A (this requires a current divider with a factor 1/100). The maximum output frequency is set at about 30 kHz. This sets the value of the capacitor in the integrator at approximately 10 pF.

The circuit is simulated by injecting a DC current. The capacitor voltage will therefore be triangular shaped, while the output voltage will be block shaped as depicted in Figure 6. To check the accuracy of the circuit, various input currents are used (10 nA, 100 nA and $1\,\mu$A). The frequencies are found to be 288 Hz, 2.88 kHz and 28.6 kHz respectively. This shows the circuit is able to handle a very large range of input currents very accurately.

The static power consumption is mainly dominated by the static current through the M_3-M_4-M_7-M_8-branch of the threshold compensated inverter. When the integrator is reset ($V_{cap} = 0$ V), the supply current is 57 nA, resulting in 171 nW.

When the integrator is active, the power consumption increases, mainly due to current through the M_1-M_2-M_5-M_6-branch of the threshold compensated inverter. The current depends on the threshold voltages set at the schmitt trigger, since this determines the level of inversion of M_5 and M_6 by V_g. For 0.5 V and 2.5 V the current consumption increases to 800 nA and $4.1\,\mu$A respectively. This can be decreased by shifting the threshold voltages more to 0 V and V_{dd} or by increasing the length of M_5 and M_6 at the cost of speed since it will make the output current smaller.

The minimum and maximum detectable amount of charge

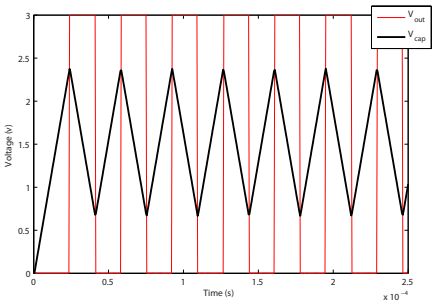


Fig. 6. Capacitor and output voltage of the integrator

determine the dynamic range of the integrator. The minimum charge output (one charge packet) is defined by one period of the integrator. This corresponds to a 4 V change (twice V_H-V_L) in a 10 pF capacitor, yielding $Q_{min} = 40$ pC. For the maximum charge, the current divider is set to its maximum attenuation 1/100 and each period corresponds to a charge of $100Q_{min} = 4$ nC. Assuming an N-bit counter, the maximum charge is set at $(2^N - 1)4$ nC. A 10 bit counter can for example accomodate for a charge of $Q_{max} = 4.1\,\mu$C. This results in a total dynamic range at the output of $20\log(Q_{max}/Q_{min}) = 100$ dB.

VI. Conclusion

A current integrator circuit has been proposed, offering a 100 dB dynamic range, while it only has a static power consumption of 171 nW. Because the output is converted to a periodic signal with each period corresponding to a charge packet, the dynamic range is limited only by the counter processing the output.

This integrator makes it possible to accurately measure the charge injected in the tissue by a neural stimulator circuit. This is the key ingredient for charge based stimulation, while it also allows for any arbitrary stimulation waveform. Combined with the low power consumption, this paves the way for much more effective and patient friendly neural stimulation.

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