An Additive Instantaneously Companding Readout System for Cochlear Implants

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***Abstract*—This paper presents an additive instantaneous companding technique in order to record the compound action potentials from the stimulated auditory nerve. This technique is intended to be combined with an analog to digital converter to achieve the 126-dB dynamic range that covers both stimulus (up to 20V), artifact and the neural response (down to 10μV). From the readout signal, the correct operation and placement of the cochlear stimulator can be estimated and useful information for further clinical studies can be obtained. The proposed system is designed to be implemented in AMIS I3T25 (high voltage) CMOS technology. Simulation results confirm the correct operation of the circuit.**

I. INTRODUCTION

At the moment more than 100,000 people suffer from deafness. In the case of profoundly deaf, the patients cannot be helped with conventional hearing aids. Cochlear implants (CIs) can successfully restore hearing of people who are profoundly deaf. CIs nowadays are the most successful and most advanced neurostimulator available. An important tool to help fitting cochlear implants to patient specific needs is a neural readout system. Besides, this readout system is used for acquiring neural responses for scientific research to get better understanding of the human hearing and pushing forward the development of autonomous closed loop cochlear implanted devices.

Reading out the neural response after stimulation can be done by using a technique called evoked compound action potential (eCAP) [1]. Unfortunately, only a small part of the total eCAP can be captured due to the limited dynamic range of the neural amplifier used.

In this paper, a compact readout system using a technique called 'additive instantaneous companding' to handle the entire range of the evoked neural response is proposed. This technique can be realized by using compact switched-capacitor (SC) circuits. Despite being compact, i.e., having a low physical area hence low total capacitance, the noise contribution of the circuit can be kept small. Using the proposed technique, the stimulus and the artifact amplitude can be lossless compressed to fit the dynamic range of a practical electronic circuit while the neural response amplitude is preserved.

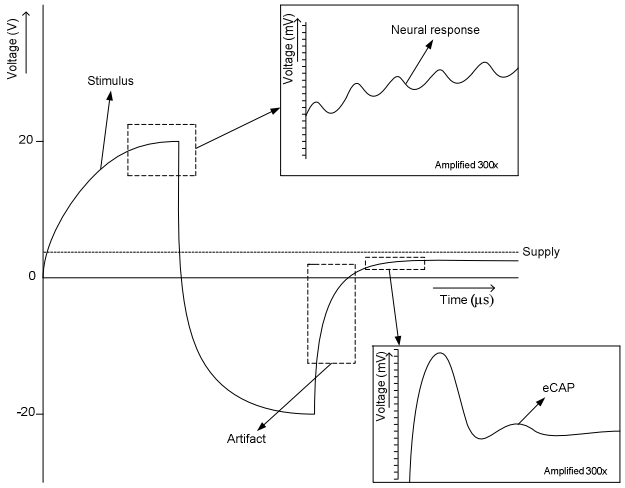

Figure 1. Signals presented at the cochlea

The remaining sections of the paper are organized as follows. In the next section, an overview of the compound action potential is described. In Sec. III, several techniques that have been investigated to read out action potentials will be discussed. The proposed technique and its circuit solutions are reported in Sec. IV. Next in Section V, the simulation results are reported. The conclusions will be drawn in the last section.

II. EVOKED ACTION POTENTIAL

Signals occurring at the cochlea excited by electrical stimulation can be divided into three categories. The first one is the stimulus generated by a stimulator; the second one the residual charge caused by the stimulus, called artifact; and the last one the neural response coming from the auditory nerves that can take place during stimulus, artifact and thereafter. Fig. 1 illustrates a typical signal occurring at the cochlea.

As can be seen from Fig. 1, the peak amplitude of the input signal can reach 20V. Neural responses can have frequencies

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up to 10 kHz [2]. This implies a minimum sampling rate of 20kS/s is needed for the signal conversion. The neural response to be measured can be as small as 10µV. This implies a dynamic range of 126dB is needed. Converting this signal range into a digital code, at least 21 bits resolution is required. Using the most power efficient analog to digital converter (ADC), a successive approximation ADC, a huge area for the capacitive array and a relatively large switching energy will be needed [3].

III. EXISTING SOLUTIONS

In order to cope with the large dynamic range of the input signal, four system principles are considered.

1. *Resistive divider*: By linearly attenuating the input signal level down to the level of the supply voltage or lower. Major drawback of this method is the noise contribution of the resistors combined with the attenuation of the original signal. The neural responses will drown into the noise making this principle not suitable for this application.
2. *Multiplicative companding*: This technique
    a. compresses the dynamic range at the input, thereby decreasing the signal to noise ratio.
    b. Processes the signal in a low-voltage environment.
    c. Expands the dynamic range such that it becomes equal to that of the input signal.

    In this way, a high dynamic range can be achieved and overloading of subsequent circuitry is prevented. However, the higher the compression, the higher the noise level will be [4][5]. Just as the resistive divider, also multiplicative companding will not meet the noise requirements.
3. *Folding ADC*: A folding ADC consists of several folding cells. Each folding cell consists of high voltage components in order to handle the high input voltage levels [6]. High voltage components use a large amount of chip area compared to their low voltage equivalents which is very critical in medical implants.
4. *ΣΔ ADC*: A sigma-delta ADC can typically convert up to 24 bits. High dynamic ranges in combination with low noise levels can be achieved. However, power consumption is quite high compared to other ADC architectures. Just as in the previous case, high voltage components will be needed causing a high chip area consumption [7].

The aforementioned techniques do not provide a good solution to handle the high dynamic range signal within an electronic device that consumes a small area and low power consumption. In the next section, we propose to use the concept of additive instantaneous companding to solve the problem.

IV. PROPOSED READOUT DETECTOR

A. System

To readout the evoked action potential, an additive instantaneous companding system is proposed. Fig. 2 depicts a high level system block diagram. V_{in} represents the input signal coming from the electrode placed in the cochlea. A (small) attenuation factor g is introduced at the input and will be discussed in more detail later. After this attenuation block, the signal is sensed by two comparators. One comparator compares the input signal with a high reference voltage, V_{refh}, and one comparator compares the signal with a low reference level, V_{refl}. When one of the reference levels is crossed, a pulse will be given to an offset generator. The positive offset will be generated when V_{refl} has been reached and when V_{refh} has been reached a negative offset will be generated. The signal coming from the offset generator is added to the attenuated signal. Then, the added signal is sampled by a sample and hold amplifier (SHA) and converted to the digital domain by an ADC. In order to keep track of the amount of positive and negative offsets generated, a shift register is added to reconstruct the input signal in the digital domain.

The output will be "reset" to a high or a low level whenever one of the voltage references is reached. Fig. 3a depicts the input and output voltages in case of a sinusoidal input signal. The output voltage follows the input voltage until reference V_{refh} is reached. Then, a negative offset is added. The signal can rise again but does not reach V_{refh} again. It goes down to V_{refl} and now a positive offset is added. This mechanism goes on throughout the whole sine wave. What actually happens is shifting the input voltage range up or down within the input dynamic range as soon as the input voltage becomes too high or too low. This can be implemented without extra noise contribution.

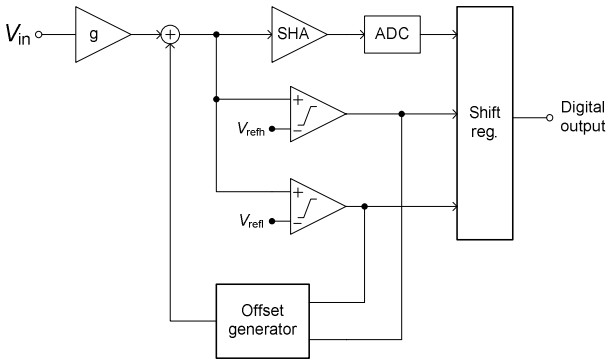

Figure 2. High level system diagram of the additive companding technique

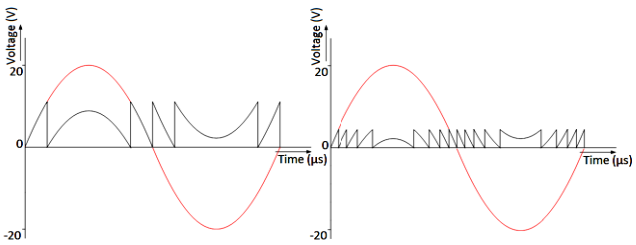

Figure 3. The input and output waveforms of the system at different reference voltages

Fig. 3b again shows the input and output signal obtained by setting a lower V_{refh} . As can be seen, this results in more switching steps.

B. Circuits

Two implementations of the system are discussed. The first one is based on offsetting in the voltage domain. The second one is based on offsetting in the charge domain.

1) Offsetting in the voltage domain

A voltage domain implementation of the system is depicted in Fig. 4. The control loop circuit that controls the switches is omitted for clarity. Gain stage g is formed by the connection of two capacitors C_1 and C_2 yielding

$$\mathrm{g} = \frac{C_1}{C_1 + C_2} \tag{1}$$

The ratio of them can be chosen such that the gain will be close to 1 in order to keep the gain high. The offset voltage generator can be realized by two simple switches S_1, S_2 and two voltage sources, V_H and V_L for a high and low reference voltage, respectively. The voltages are chosen to be different from V_{refh} and V_{refl} of the control loop to prevent oscillation. Capacitors C_1 and C_2 represent the attenuation stage. Switch S_1 together with V_L represent the offset voltage generator to reset to a lower voltage across C_2. Switch S_2 together with V_H represent the offset voltage generator to reset to a higher voltage across C_2. The circuit can be represented by (2) in which *floor* stands for rounding down to integers, for example so 0.8 becomes 0.

$$V_{out} = \mathrm{g} \cdot \left[V_{in} - (V_{TH1} - V_L) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_{TH1} - V_L} \right) + (V_H - V_{TH2}) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_H - V_{TH2}} \right) \right] \tag{2}$$

Accuracy of the system is crucial for the correct operation of the circuit. Offset voltages generated by the actual offsetting should not exceed 10µV. This implies that at the threshold voltage the switch has to be closed immediately to prevent overshoot. Also, the switch has to be opened fast enough in order to prevent loss of the signal as, during offsetting, the voltage across C_2 cannot follow the input signal. The control action will always undergo a certain delay and have a certain spread in exact switching time. In (2), the inaccuracy can be found by giving a small deviation to V_{TH1} and V_{TH2}. Moreover, the accuracy depends on the input signal frequency. The higher the input signal frequency, the bigger the inaccuracy will be. In order to have sufficient accuracy, the switching time should not exceed 2ps. In most technologies, this will not be possible in a low power fashion. It is therefore necessary to design the circuit in a different way.

2) Charge domain based offsetting

Offsetting can also be done by injecting a certain charge. For offsetting to lower voltages, a negative charge can be used. For offsetting to higher voltages, a positive charge can be used. The principle is depicted in Fig. 5. Attenuation stage g is identical to the voltage domain circuit described in the previous subsection. The ratio of C_1 and C_2 again can be chosen such that the gain will almost be 1.

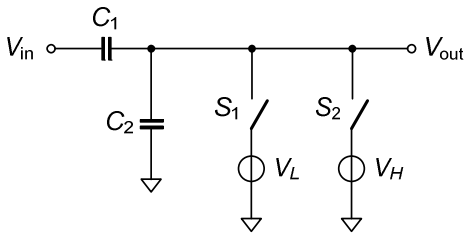

Figure 4. Voltage controlled offsetting circuit

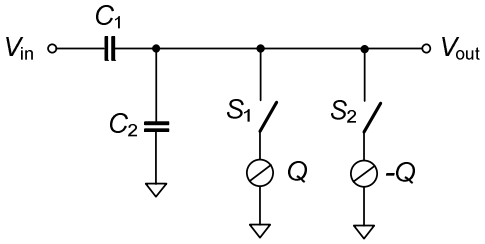

Figure 5. Charge controlled offsetting circuit

The charge injector can be realized by a charge source $-Q$ for injecting a negative charge which can be switched by switch S_1 when output voltage V_{out} reaches threshold V_{refh} and a charge source Q for injecting a positive charge which can be switched by S_2 when output voltage V_{out} reaches threshold V_{refl}. During the injection of charge Q or $-Q$, the input signal is still passed through the capacitive divider to the output. The addition or subtraction of charge does not influence the charge distribution from the input signal over C_1 and C_2 (superposition holds). A well defined charge Q or $-Q$ is added to the charge in C_2. The circuit can be seen as a dynamical system and can be represented by (3).

$$Q_{out} = V_{in} \cdot \mathrm{g} \cdot C_2 - \mathrm{Q} \cdot floor\left(\frac{-V_{in} \cdot \mathrm{g} \cdot C_2}{-\mathrm{Q}} \right) + \mathrm{Q} \cdot floor\left(\frac{-V_{in} \cdot \mathrm{g} \cdot C_2 + \mathrm{Q}}{\mathrm{Q}} \right) \tag{3}$$

In the formula, no threshold voltage is presented. This implies that the threshold levels will not give inaccuracies in addition and subtraction. Thresholds are still used in a control loop for closing switches S_1 and S_2, but the speed of the control loop and switch do not influence the accuracy of the system as was the case for the voltage-based additive companding. The accuracy is now determined by the accuracy of the charge source which can be made very accurately. The offsetting time has to be limited within 0.5 sample time. Because sampling of the subsequent sample and hold stage at the input of the ADC only occurs in between the offsetting steps and not during these steps, the added noise will ideally be zero. Because of this reason, this circuit is suitable for application in the readout of cochlear implants.

V. SIMULATION RESULTS

The charge domain based offsetting circuit is simulated using Cadence. The circuit is made using AMIS I3T25 (high voltage) CMOS technology.

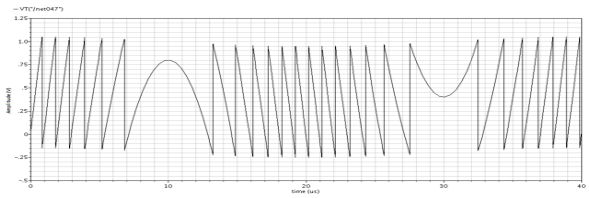

Figure 6. Compressed signal

Capacitor C_1 is realized with high voltage capacitor *mmchb* from the technology library having a finger length of 80µm and a number of fingers of 40. C_2 is realized with low voltage component *mimc* from the technology library having a width and a length of 20µm. Q and S_1 for this simulation are composed as a voltage source acting as a counter in series with a *mimc* capacitor having the same length and width as C_2. For $-Q$, the counter counts down instead of counting up. The simulation temperature is set at 37 ºC (body temperature). At the input of the circuit, a sine wave with an amplitude of 20V is applied. A gain of approximately ½ is achieved. The output of the attenuator is sensed and when a threshold of 1V is reached, the control loop will close switch S_2, thereby injecting a negative charge into C_2. When a threshold of -200mV is reached, the control loop will close S_1 injecting a positive charge into C_2. The resulting output signal (voltage) is depicted in Fig. 6. The signal is not offset at exactly the same voltage all the time. This is due to the different slope of the input signal and deviations in switching speed of the control loop. This does not affect the accuracy of the addition/subtraction step. The addition and subtraction steps are equal. By using a charge for offsetting, a high accuracy can be reached. Deviations of less than 1µV are reached.

A transient noise simulation is performed. The results are depicted in Fig. 7. Integrating the noise over the bandwidth gives a total noise of 1.1pV. This is far under the 10µV which is required.

Finally, an expansion of the compressed signal is performed by adding a fixed offset to the output signal. The compressed and expanded signals are depicted in Fig. 8. The reconstructed signal looks the same as the input signal. Only one difference can be seen. The reconstructed signal is approximately ½ of the input signal, which is the same as the gain of the circuit. Gain errors can be corrected by performing a calibration.

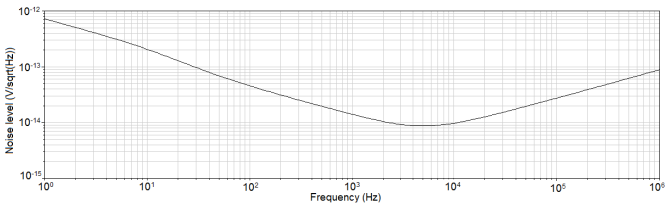

Figure 7. Noise simulation results

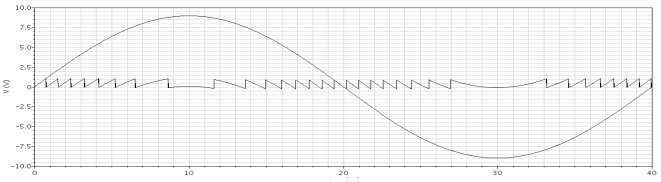

Figure 8. Reconstruction of the input signal

VI. CONCLUSION

A simulated circuit prototype based on additive instantaneous companding has been presented. The circuit is especially designed for application in cochlear implants read out systems. System level design and two circuit implementations have been discussed. Circuit simulations of the transient behavior, noise contribution and signal reconstruction are performed. The results verify that this method can be combined with an ADC to significantly reduce power consumption, chip area consumption and enable a very large dynamic range.

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