Dynamic Translinear Circuits

Wouter A. Serdijn, Jan Mulder,
Paul Poort, Michiel Kouwenhoven,
Arie van Staveren and Arthur H.M. van Roermund
Delft University of Technology,
Faculty of Information Technology and Systems/DIMES
Electronics Research Laboratory
Mekelweg 4, 2628 CD Delft, The Netherlands
phone: +31-15-2781715, fax: +31-15-2785922,
e-mail: W.A.Serdijn@its.tudelft.nl

Abstract

A promising new approach to shorten the design trajectory of analog integrated circuits without giving up functionality is formed by the class of dynamic translinear circuits. This paper presents a structured design method for this young, yet rapidly developing, circuit paradigm. As a design example, a 1-V 1.6-μA class-AB translinear sinh integrator for audio filter applications, is presented.

1 Introduction

Electronics design can be considered to be the mapping of a set of mathematical functions onto silicon. For discrete-time signal-processing systems, of which the digital signal processors (DSPs) today are by far the most popular, this comes down to the implementation of a number of difference equations, whereas for continuous-time signal-processing systems, often denoted by the term analog,

differential equations are the starting points. In mixed analog-digital systems, the analog parts, however, often occupy less than ten percent of the complete, i.e., the mixed analog-digital circuitry, whereas their design trajectory is often substantially longer and therefore more expensive than of their digital counterparts. Where does this discrepancy arise from? This can be partially explained by the fact that, at circuit level, for analog circuits far more components play an important role; various types of transistors, diodes, resistors and capacitors, to mention a few; sometimes also inductors, resonators, and others. Whereas for digital circuits, the complete functionality is covered by transistors only[1].

From the above, it automatically follows that, if we restrict ourselves to the use of as few different types of components as possible, without giving up functionality, we can shorten the analog design trajectory considerably, in the same way as this is done for digital circuits. One successful approach, as we will see in this paper, is given by the class of circuits called *dynamic translinear circuits.*

Dynamic translinear (DTL) circuits, of which recently an all-encompassing current-mode analysis and synthesis theory has been developed in Delft [1–3], are based on the DTL principle, which can be regarded as a generalization of the well-known 'static' translinear principle, formulated by Gilbert in 1975 [4]. The first DTL circuit was originally introduced by Adams in 1979 [5], being a first-order lowpass filter. Although not recognized then, this was actually the first time a first-order linear differential equation was implemented using translinear (TL) circuit techniques. In 1990, Seevinck introduced a 'companding current-mode integrator' [6] and since then the principle of TL filtering has been extensively studied by Frey [7–16], Punzenberger and Enz [17–31], Toumazou et al. [32–51], Roberts et al. [52–57], Tsividis [58–62], Mulder and Serdijn [63–84] and others [85, 86].

However, the DTL principle is not limited to filters, i.e. linear differential equations. By using the DTL principle, it is possible to

[1]It must be noted that, for higher frequencies or bit rates, also the interconnects come into play. However, their influence is considered to be equally important for analog as well as digital systems.

implement linear *and* nonlinear differential equations, using transistors and capacitors only. Hence, a high functional density can be obtained, and the absence of large resistors makes them especially interesting for ultra-low-power applications [76].

DTL circuits are inherently companding (the voltage swings are logarithmically related to the currents), which is beneficial with respect to the dynamic range in low-voltage environments [87,88]. In addition, DTL circuits are easily implemented in class AB, which entails a larger dynamic range and a reduced average current consumption. Further, owing to the small voltage swings, DTL circuits facilitate relatively wide bandwidth operation. At high frequencies though, considerable care has to be taken regarding the influence of parasitic capacitances and resistances, which affect the exponential behavior of the transistor.

DTL circuits are excellently tunable across a wide range of several parameters, such as cut-off frequency, quality factor and gain, which increases their designability and makes them attractive to be used as standard cells or programmable building blocks.

The DTL principle can be applied to the structured design of both linear differential equations, i.e. filters, and non-linear differential equations, e.g., RMS-DC converters [89–91], oscillators [92–103], phaselock loops (PLLs) [80–82] and even chaos. In fact, the DTL principle facilitates a direct mapping of any function, described by differential equations, onto silicon.

Application areas where DTL circuits can be successfully used include audio filters, high-frequency filters, high-frequency oscillators, demodulators, infra-red front-ends and low-voltage ultra-low-power applications.

This paper aims to present a structured design method for DTL circuits. The static and dynamic TL principles are reviewed in Section 2. The general class of DTL circuits contains several different types. In Section 3, the correspondences and differences of log-domain, tanh and sinh circuits are treated. Finally, Section 4 presents the design method, applied to the design of a DTL integrator, starting from a dimensionless differential equation that describes the integrator behavior in the time domain. After four

hierarchical design steps, being dimension transformation, the introduction of capacitance currents, TL decomposition and circuit implementation, a complete circuit diagram results. Measurement results of the thus obtained DTL integrator, are presented.

2 Design principles

TL circuits can be divided into two major groups: static and dynamic TL circuits. The first group can be applied to realize a wide variety of linear and non-linear static transfer functions. All kinds of frequency-dependent functions can be implemented by circuits of the second group. The underlying principles of static and dynamic TL circuits are reviewed in this section.

2.1 Static translinear principle

TL circuits are based on the exponential relation between voltage and current, characteristic for the bipolar transistor and the MOS transistor in the weak inversion region. In the following discussion, bipolar transistors are assumed. The collector current I_C of a bipolar transistor in the active region is given by:

$$I_C = I_S \mathrm{e}^{V_{BE}/V_T}, \tag{1}$$

where all symbols have their usual meaning.

The TL principle applies to loops of semiconductor junctions. A TL loop is characterized by an even number of junctions [4]. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Figure 1. It is assumed that the transistors are somehow biased at the collector currents I_1 through I_4. When all devices are equivalent and operate at the same temperature, this yields the familiar representation of TL loops in terms of products of currents:

$$I_1 I_3 = I_2 I_4. \tag{2}$$

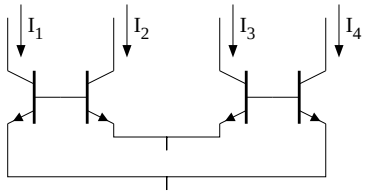

Figure 1: A four-transistor translinear loop.

This generic TL equation is the basis for a wide variety of static electronic functions, which are theoretically temperature and process independent.

2.2 Dynamic translinear principle

The static TL principle is limited to frequency-independent transfer functions. By admitting capacitors in the TL loops, the TL principle can be generalized to include frequency-dependent transfer functions. The term 'Dynamic Translinear' was coined in [89] to describe the resulting class of circuits. In contrast to other names proposed in literature, such as 'log-domain' [5], 'companding current-mode' [6], 'exponential state-space' [7], this term emphasizes the TL nature of these circuits, which is a distinct advantage with respect to structured analysis and synthesis.

The DTL principle can be explained with reference to the subcircuit shown in Figure 2. Using a current-mode approach, this circuit is described in terms of the collector current I_C and the capacitance I_{cap} flowing through the capacitance C. Note that the dc voltage source V_{const} does not affect I_{cap}. An expression for I_{cap} can be derived from the time derivative of (1) [6, 89]:

$$I_{\mathrm{cap}} = CV_T \frac{\dot{I}_C}{I_C}, \tag{3}$$

where the dot represents differentiation with respect to time.

Equation (3) shows that I_{cap} is a non-linear function of I_C and its time derivative $\dot{I}_C$. More insight in (3) is obtained by slightly

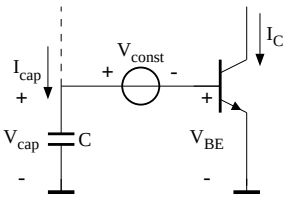

Figure 2: Principle of dynamic translinear circuits.

rewriting it:

$$CV_T\dot{I}_C = I_{\mathbf{cap}}I_C. \tag{4}$$

This equation directly states the DTL principle: *A time derivative of a current can be mapped onto a product of currents.* At this point, the conventional TL principle comes into play, since the product of currents on the right-hand side (RHS) of (4) can be realized very elegantly by means of this principle. Thus, the implementation of (part of) a differential equation (DE) becomes equivalent to the implementation of a product of currents.

The DTL principle can be used to implement a wide variety of DEs, describing signal processing functions. For example, filters are described by linear DEs. Examples of non-linear DEs are harmonic and chaotic oscillators, PLLs and RMS-DC converters.

3 Classes of dynamic translinear circuits

In all DTL circuits, the voltages are logarithmically related to the currents. Therefore, these circuits are in some way instantaneous companding. Figure 3 shows the general block schematic of an instantaneous companding integrator [6]. In DTL circuits, the internal integrator is a linear capacitance. The expander E expands the output voltage of this integrator into a current, exploiting the exponential V-I transistor transfer function. Several types of DTL circuits can be distinguished within the general class of DTL circuits based on the particular implementation of E. Next to the most prevalent class of log-domain circuits, the two classes of tanh

and sinh circuits have been proposed by Frey [12]. In this section, we describe their characteristics, which can be derived from the generic output structures, depicted in Figure 4.

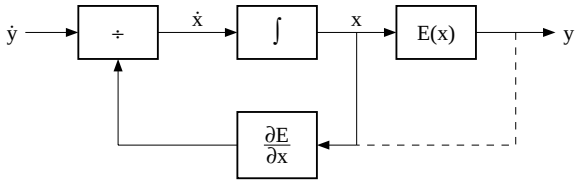

Figure 3: General block schematic of an instantaneous companding integrator.

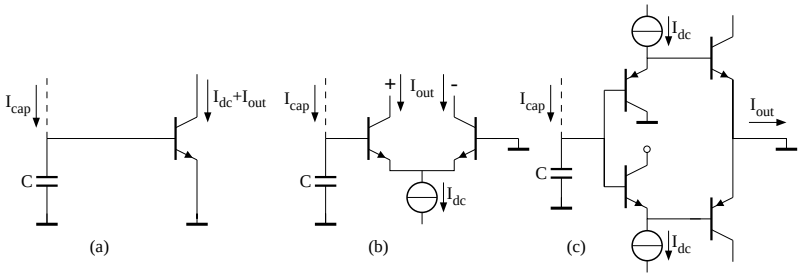

Figure 4: Generic output structures of (a) log-domain, (b) tanh, and (c) sinh circuits.

3.1 log-domain circuits

Most published DTL circuits are based on the common-emitter (CE) output stage shown in Figure 4(a), characteristic for the class of log-domain circuits. The transfer function from the capacitance voltage $V_{\mathbf{cap}}$ to the output current $I_{\mathbf{out}}$ is given by the well-known exponential law (1). In other words, E equals $\exp x$. The companding characteristics of a DTL circuit can be derived from the second order derivative of E with respect to x, denoted by E''. Without loss of generality, $x = 0$ is considered to be the quiescent point of the integrator shown in Figure 3. Figure 5 displays E'' for the output

stages shown in Figure 4. Applying a strict definition of companding, E'' should be strictly positive for $x > 0$ and strictly negative for $x < 0$. For log-domain circuits, a comparison of $E'' = \exp x$ with the strict definition of companding reveals that these circuits are indeed companding for $x > 0$; however, for $x < 0$ the exponential function constitutes a compression instead of an expansion. For a symmetrical output current, the overall behaviour of the CE output stage implies a compression rather than an expansion of the peak-to-peak signal swings [86].

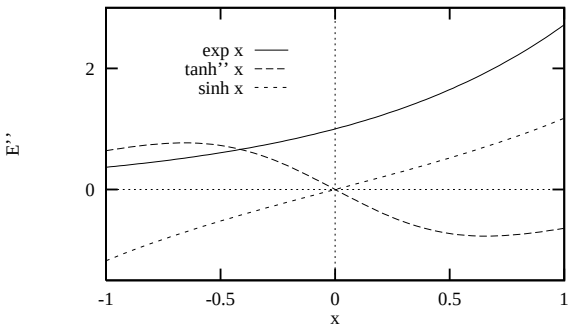

Figure 5: The second-order derivatives of the V-I transfer functions of the output stages shown in Figure 4.

From a current-mode point of view, the most important characteristic of a DTL output structure is the current-mode expression for the capacitance current I_{cap}. For log-domain filters, I_{cap} is given by Equation (3), where $I_C = I_{\mathrm{dc}} + I_{\mathrm{out}}$. As shown in Section 2, a linear derivative $\dot{I}_{\mathrm{out}}$ is obtained by multiplying I_{cap} by $I_{\mathrm{dc}} + I_{\mathrm{out}}$.

A favorable property of log-domain circuits is that a linear damping term can be implemented by the connection of a dc current source I_o in parallel to a capacitance. This can be explained from Equation (4). If instead of I_{cap}, $I_{\mathrm{cap}} + I_o$ is multiplied by $I_{\mathrm{dc}} + I_{\mathrm{out}}$, an additional term $I_o \cdot (I_{\mathrm{dc}} + I_{\mathrm{out}})$ is generated. The first term $I_o I_{\mathrm{dc}}$ represents a dc offset current. The second term $I_o I_{\mathrm{out}}$ results in a finite negative pole.

Typically, log-domain circuits operate in class A. The actual ac signal I_{out} is superposed on a dc bias current I_{dc}. As a consequence,

the output signal swing is limited to $I_{\rm out} > -I_{\rm dc}$. Note that this limitation is single sided, which is advantageous if a-symmetrical input wave-forms have to be processed. This characteristic can be exploited to enable class AB operation [6,9]. Using a class AB set-up, see Figure 6, the dynamic range can be enlarged without increasing the quiescent power consumption. Using a current splitter, the input current $I_{\rm in}$ is divided into two currents $I_{\rm in1}$ and $I_{\rm in2}$, which are both strictly positive, and related to $I_{\rm in}$ by: $I_{\rm in} = I_{\rm in1} - I_{\rm in2}$. The current splitter impresses a constant geometric or harmonic mean on $I_{\rm in1}$ and $I_{\rm in2}$. Next, $I_{\rm in1}$ and $I_{\rm in2}$ can be processed by two class A log-domain circuits. It is important to note that class AB operated log-domain circuits do satisfy the strict definition of companding due to the fact that only positive currents are processed, i.e., x is never negative.

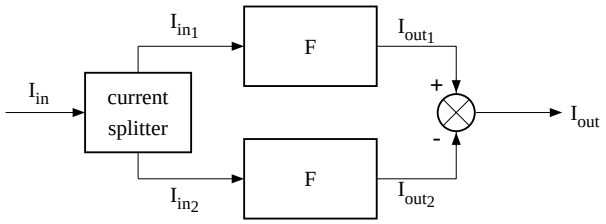

Figure 6: Set-up for class AB operation.

3.2 tanh circuits

Instead of a single transistor in CE configuration, the class of tanh circuits is characterized by a differential pair output structure [12], see Figure 4(b). The name of this class of circuits is derived from the well-known hyperbolic tangent V-I transfer function. The second-order derivative E'' is shown in Figure 5 and demonstrates that tanh circuits are not companding at all [48]. The differential pair implements a *compression* function.

The tail current of the differential pair is a dc current $I_{\rm dc}$, and therefore, tanh circuits also operate in class A. The output current $I_{\rm out}$ is the difference of the two collector currents. The output swing

is limited to $-I_{\rm dc} < I_{\rm out} < I_{\rm dc}$. Since this interval is symmetrical, the class AB set-up shown in Figure 6 cannot be applied to tanh circuits.

From Figure 4(b), the capacitance current $I_{\rm cap}$ is found to be:

$$I_{\rm cap} = CV_T \left(\frac{\dot{I}_{\rm out}}{I_{\rm dc} + I_{\rm out}} - \frac{-\dot{I}_{\rm out}}{I_{\rm dc} - I_{\rm out}} \right). \tag{5}$$

A linear derivative $\dot{I}_{\rm out}$ is obtained by multiplying this equation by $(I_{\rm dc} + I_{\rm out})(I_{\rm dc} - I_{\rm out})$:

$$2CV_T I_{\rm dc} \dot{I}_{\rm out} = I_{\rm cap}(I_{\rm dc} + I_{\rm out})(I_{\rm dc} - I_{\rm out}). \tag{6}$$

Comparing Equations (4) and (6), we can see that the RHS of (6) is third-order, whereas the RHS of (4) is only second-order. Consequently, in general, TL loops of a higher order are required to implement a tanh circuit, resulting in a more complex circuit. In addition, a linear loss cannot be implemented by a dc current source connected in parallel to a capacitance. This leads us to the conclusion that tanh circuits do not seem to have any advantages over log-domain circuits.

3.3 sinh circuits

The third class of DTL circuits proposed in literature is formed by the sinh circuits [12]. The output structure, shown in Figure 4(c), is a complete second-order TL loop. It implements the geometric mean function $I_{\rm dc}^2 = I_{\rm out1} I_{\rm out2}$. The actual output current $I_{\rm out}$ is the difference of $I_{\rm out1}$ and $I_{\rm out2}$. Since both $I_{\rm out1}$ and $I_{\rm out2}$ are always positive, the sinh output structure operates in class AB, which is beneficial with respect to the dynamic range. The V-I transfer function of the output structure is a hyperbolic sine function. Figure 5 displays $E'' = \sinh x$ and shows that the sinh output stage implements a genuine expansion function.

The current-mode expression for the capacitance current $I_{\rm cap}$ is

given by:

$$I_{\text{cap}} = CV_T \frac{\dot{I}_{\text{out}_1}}{I_{\text{out}_1}}, \tag{7}$$

$$= -CV_T \frac{\dot{I}_{\text{out}_2}}{I_{\text{out}_2}}, \tag{8}$$

$$= CV_T \frac{\dot{I}_{\text{out}}}{\sqrt{4I_{\text{dc}}^2 + I_{\text{out}}^2}}, \tag{9}$$

$$= CV_T \frac{\dot{I}_{\text{out}}}{I_{\text{out}_1} + I_{\text{out}_2}}. \tag{10}$$

A linear derivative $\dot{I}_{\text{out}}$ is obtained by multiplying I_{cap} by the sum $I_{\text{out1}} + I_{\text{out2}}$. It is interesting to note that the voltage V_{cap} and the current $I_{\text{out1}} + I_{\text{out2}}$ are related through a hyperbolic cosine function; the first-order derivative of E with respect to x.

4 Structured design of a class-AB dynamic translinear integrator

Synthesis of a dynamic circuit, be it linear or non-linear, starts with a DE or with a set of DEs describing its function. Often, it is more convenient to use a state-space description, which is mathematically equivalent. The structured synthesis method for DTL circuits is illustrated here by the design of a first-order integrator, described in the time domain by:

$$\frac{dy}{d\tau} - x = 0 \tag{11}$$

This equation describes the integrator output signal y as a function of the input signal x. τ is the dimensionless time of the integrator.

4.1 Transformations

In the pure mathematical domain, equations are dimensionless. However, as soon as we enter the electronics domain to find an

implementation of the equation, we are bound to quantities having dimensions. In the case of TL circuits, all time-varying signals in the DEs, i.e., the input signals, the output signals and the tunable parameters, have to be transformed into currents. For the above expression, x and y can be transformed into the currents $I_{\text{in}} = x \cdot I_o$ and $I_{\text{out}} = y \cdot I_o$, I_o being the DC bias current that determines the absolute current swings.

Subsequently, the dimensionless time τ, can be transformed into the time t with its usual dimension $[s]$, using the equivalence relation given by:

$$d/d\tau = CV_T/I_o \cdot d/dt. \tag{12}$$

From this expression it can be deduced that the integrator will be linearly frequency tunable by means of control current I_o.

Applying the mentioned transformations, the resulting differential equation becomes:

$$CV_T\dot{I}_{\text{out}} - I_o I_{\text{in}} = 0 \tag{13}$$

4.2 Definition of the capacitance current

Conventional TL circuits are described by multivariable polynomials, in which all variables are currents. The gap between these current-mode polynomials and the DEs can be bridged by the introduction of capacitance currents, since the DTL principle states that a derivative can be replaced by a product of currents.

The capacitance currents can be introduced simply by defining them. To this end, several equivalent expressions for the capacitance current I_{cap} associated with the generic output stage of (class-AB) sinh circuits, depicted in Figure 4(c), can were obtained in Section 3. These equations all have two important characteristics in common. First, the denominators on the RHS are collector currents. This implies that these currents have to be strictly positive. Second, the numerators on the RHS are the time derivatives of the denominators.

With these characteristics in mind, we can define the capacitance current for the sinh integrator. As the capacitance current

will be used to eliminate the derivative from the DE, in the definition of this current, the derivative present in the DE has to be used. Using (10), the differential equation transforms into:

$$I_{\rm cap}\,(I_{\rm out_1} + I_{\rm out_2}) = I_{\rm o} I_{\rm in}. \tag{14}$$

The current $I_{\rm cap}$ to be supplied to the capacitance C is thus given by:

$$I_{\rm cap} = \frac{I_{\rm o} I_{\rm in}}{I_{\rm out_1} + I_{\rm out_2}}. \tag{15}$$

From this point on, the synthesis theory for static TL circuits can be used [104], since both sides of the above DEs are now described by current-mode multivariable polynomials.

4.3 Translinear decomposition

The next synthesis step is translinear decomposition. That is, the current-mode polynomial has to be mapped onto one or more TL loop equations that are characterized by the general equation:

$$\prod_{\rm CW} J_{C,i} = \prod_{\rm CCW} J_{C,i} \tag{16}$$

$J_{C,i}$ being the transistor collector current densities in clockwise (CW) or counter-clockwise (CCW) direction.

A two-quadrant multiplier/divider is required to implement the Right-Hand Side (RHS) of Equation (15). Since a class-AB implementation is pursued, this two-quadrant multiplier/divider has to be realized by two one-quadrant multiplier/dividers. This is realized by splitting the input current into two strictly positive signals $I_{\rm in_1}$ and $I_{\rm in_2}$, the difference of which equals $I_{\rm in}$. Rewriting Equation (15) yields:

$$I_{\rm cap} = \frac{I_{\rm o} I_{\rm in_1}}{I_{\rm out_1} + I_{\rm out_2}} - \frac{I_{\rm o} I_{\rm in_2}}{I_{\rm out_1} + I_{\rm out_2}}. \tag{17}$$

Equation (17) is the basis for the block schematic of the sinh integrator depicted in Figure 7. At the input, a current splitter

generates I_{in_1} and I_{in_2} from I_{in}. Subsequently, the currents I_{in_1} and I_{in_2} are divided by $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ in two separate circuits. The current $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$ is obtained from the sinh output stage. The output currents of the two multiplier/dividers are denoted by $I_{\mathbf{cap1}}$ and $I_{\mathbf{cap2}}$ and are respectively equal to the first and the second term on the RHS of Equation (17). Hence, the current supplied to the capacitance equals $I_{\mathbf{cap1}} - I_{\mathbf{cap2}}$. The use of a single capacitor is an advantage over the class-AB integrator proposed in [6] as it eliminates the necessity of matched capacitors. Finally, the capacitance voltage $V_{\mathbf{cap}}$ is applied to the sinh output stage via a voltage buffer to prevent interaction between the capacitance and the output stage.

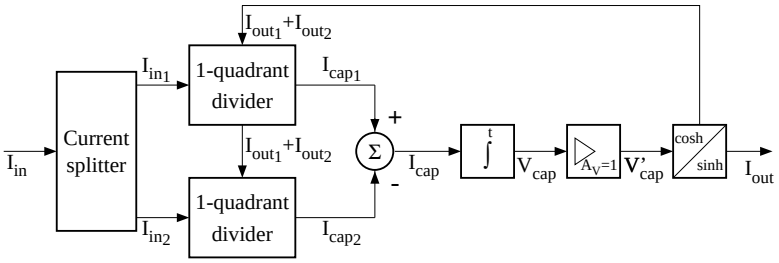

Figure 7: Block schematic of the class-AB translinear integrator.

4.4 Circuit implementation

The last synthesis step is the circuit implementation. The TL decomposition has to be mapped onto a TL circuit topology and the correct collector currents have to be forced through the transistors. Biasing methods for bipolar all-NPN TL topologies are presented in [104]. Additional implementation methods include the use of (vertical) PNPs, compound transistors or (simple) nullor implementations. If subthreshold MOSTs are used, some additional possibilities are the application of the back gate [105] and operation in the triode region [106].

The system blocks can be implemented by TL circuits, except of course the voltage buffer. To facilitate low-voltage operation, only

folded TL loop topologies are allowed. A bipolar IC technology is used to implement the individual blocks.

4.4.1 Design of the input current splitter

A current splitter generates the currents I_{in_1} and I_{in_2} at the input of the integrator. In principle, the type of current splitter to be used at the input is not dictated by Equation (17). As the output stage is a geometric mean current splitter, the same function was chosen for the input current splitter.

The TL loop equation to be implemented is $I_{\mathrm{dc}}^2 = I_{\mathrm{in}_1} I_{\mathrm{in}_2}$. Figure 8 depicts a 1 volt realization of this equation. The core of the circuit is the TL loop formed by Q_1 through Q_4. Transistors Q_1 and Q_3 are biased at a dc current I_{dc_1}. Transistor Q_2 conducts I_{in_2}. This current is inverted by a PNP current mirror and added to I_{in}. The resulting current I_{in_1} is conducted by Q_4, which is enforced by the Common-Collector (CC) stage Q_5. Biasing of Q_5 by means of a dc tail current source of the differential pair Q_2-Q_3 requires a relatively high dc current. This is disadvantageous with respect to the quiescent current consumption. A solution is dynamic biasing. The tail current of Q_2-Q_3 is generated by Q_6, Q_7 and Q_9, and equals $3I_{\mathrm{dc}_1} + I_{\mathrm{in}_2}$. Hence, Q_5 is biased at a dc current equal to only $2I_{\mathrm{dc}_1}$.

The voltage source V_{dc_1} is necessary to ensure that the Q_7 does not saturate. Note that this voltage source has no effect on the TL loop. A convenient value for V_{dc_1} is 200 mV.

4.4.2 Design of the multiplier/divider

Once the bipolar input current I_{in} is decomposed into two positive currents $I_{\mathrm{in}_{1,2}}$, such that the difference of these currents equals I_{in}, the two-quadrant multiplication of I_{in} can now be performed by the individual division of I_{in_1} and I_{in_2} by $I_{\mathrm{out}_1} + I_{\mathrm{out}_2}$, by means of two one-quadrant multiplier/dividers. The output currents of the one-quadrant multiplier/dividers satisfy:

$$I_{\mathrm{cap}_{1,2}} = \frac{I_o I_{\mathrm{in}_{1,2}}}{I_{\mathrm{out}_1} + I_{\mathrm{out}_2}}. \tag{18}$$

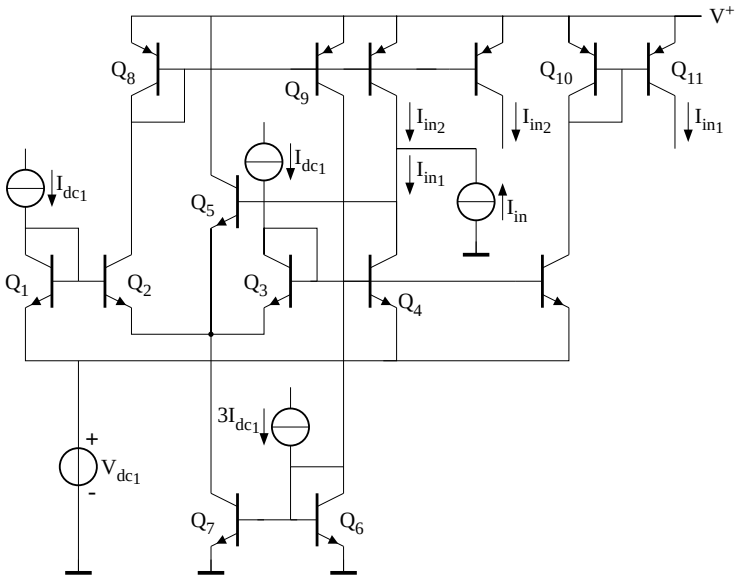

Figure 8: Implementation of the input current splitter.

As all linear factors in Equation (18) are strictly positive, it is a valid TL decomposition.

The 1 volt implementation of Equation (18) is shown in Figure 9. The second-order TL loop comprises Q_{12}–Q_{15}. Transistors Q_{13} and Q_{14} are biased by supplying respectively the currents $I_{\text{out}_1} + I_{\text{out}_2}$ and $I_{\text{in}_{1,2}}$ to the emitters of these devices. The collector current I_o of Q_{12} is enforced by the CC stage Q_{16}, which is biased by a dc current I_{bias1}.

A voltage source V_{dc_2} is necessary to ensure that the base voltages of Q_{13} and Q_{14} are always positive. Again, 200 mV is a convenient value.

The output of the multiplier/divider is the collector current of Q_{15}. Subtraction of I_{cap_1} and I_{cap_2} is performed by a PNP current mirror inverting I_{cap_2}.

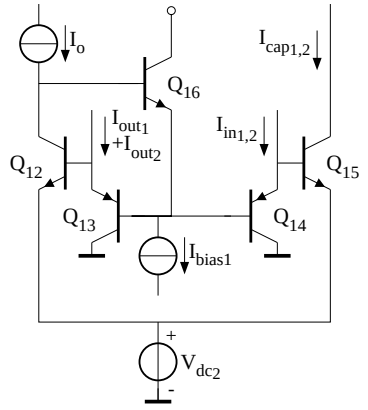

Figure 9: Implementation of the one-quadrant multiplier/divider.

4.4.3 Design of the voltage buffer

The current $I_{\mathbf{cap_1}} - I_{\mathbf{cap_2}}$ is supplied to the capacitor resulting in the voltage $V_{\mathbf{cap}}$. A voltage buffer is used to minimize the interaction between the capacitor and the sinh output stage. The principle of the buffer amplifier is depicted in Figure 10(a). Ideally, the buffering is performed by the nullor. A level-shift between the input and the output of the buffer, represented by the voltage source $V_{\mathbf{dc_3}}$, is necessary to avoid saturation of Q_{15} in the first multiplier/divider circuit. The output voltage is denoted by $V'_{\mathbf{cap}}$.

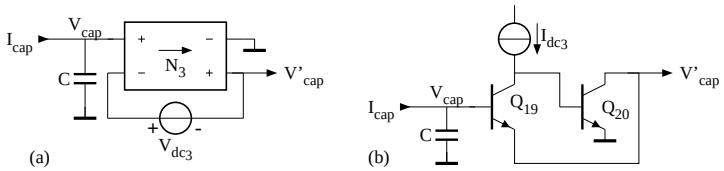

Figure 10: (**a**) Principle and (**b**) implementation of the voltage buffer.

The practical implementation of the nullor and the voltage source $V_{\mathbf{dc_3}}$ is shown in Figure 10(b). The nullor is implemented by two Common-Emitter (CE) stages, Q_{19} and Q_{20}. The level-shift is realized by the base-emitter voltage of Q_{19}. The output transistor Q_{20} must be able to sink the input current of the sinh output stage.

4.4.4 Design of the sinh output stage

The output stage has two functions. First, it enforces a geometric mean relation between the two output currents I_{out_1} and I_{out_2}. Secondly, it must provide the current $I_{\text{out}_1} + I_{\text{out}_2}$ to each of the multiplier/dividers, as shown in Figure 7.

The 1 volt realization of the output stage is depicted in Figure 11. The TL loop comprising Q_{21}–Q_{24} implements the sinh function given by:

$$I_{\text{out}} = 2I_{\text{dc}_2} \sinh \frac{V'_{\text{cap}} - V_{\text{dc}_4}}{V_T}, \tag{19}$$

where I_{dc_2} is a dc current. Note that Equation (19) is equivalent to the geometric mean function $I^2_{\text{dc}_2} = I_{\text{out}_1} I_{\text{out}_2}$.

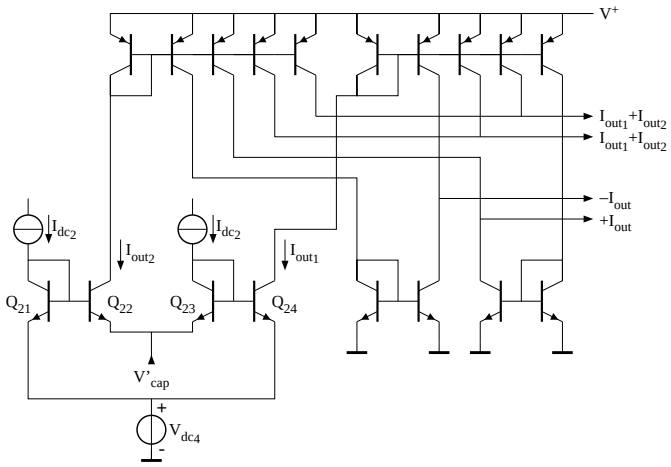

Figure 11: Implementation of the sinh output stage.

The current $I_{\text{out}_1} + I_{\text{out}_2}$ is supplied to the multiplier/dividers by means of PNP current mirrors. The output current I_{out} is generated by additional NPN current mirrors. The inverted output current $-I_{\text{out}}$ is added to easily enclose the integrator in a unity-feedback configuration by connecting $-I_{\text{out}}$ to the input of the integrator, which results in a first-order low-pass filter.

The voltage source V_{dc_4} is necessary to ensure that the emitter voltages of Q_{22} and Q_{23} are always positive. Once again, 200 mV is a convenient value.

4.5 Measurement results

Now that all the individual system blocks have been designed at circuit level, the sub-circuits can be linked together to form the integrator as depicted in Figure 7. For biasing purposes, the integrator is enclosed in a unity-feedback configuration, as discussed previously. This results in a first-order low-pass filter. Application of this filter in a hearing instrument was pursued. This leads to the required filter specifications shown in Table 1 [107]. For measurement purposes, the biasing current sources I_{dc_1}, I_{dc_2}, I_{dc_3} and I_{bias1} are realized by simple current mirrors and high-valued resistors. The frequency control current I_o is realized with a PTAT current source.

Table 1: Filter requirements.

Quantity	Value	Comment
Supply voltage	down to 1 V	
Current consumption	< 5 μA	$I_{\mathrm{in,max}} = 180$ nA$_{\mathrm{p}}$
Cut-off frequency (f_{c}) range	1.6–8 kHz	controllable
Dynamic range	68 dB	100 Hz–8 kHz
Total harmonic distortion	< 2 %	$f = 1$ kHz, $f_{\mathrm{c}} = 1.6$ kHz, $I_{\mathrm{in}} < 130$ nA$_{\mathrm{p}}$
	< 7 %	$f = 1$ kHz, $f_{\mathrm{c}} = 1.6$ kHz, $I_{\mathrm{in}} > 130$ nA$_{\mathrm{p}}$

To verify the integrator operation in practice, a semi-custom version of the active circuitry of the complete filter has been integrated in a standard 2-μm, 7-GHz process, fabricated at the Delft Institute of Microelectronics and Submicron Technology. Typical transistor parameters are: $h_{\mathrm{fe,NPN}} \approx 100$, $f_{T,\mathrm{NPN}} \approx 7$ GHz, $h_{\mathrm{fe,LPNP}} \approx 80$ and $f_{T,\mathrm{LPNP}} \approx 40$ MHz. The dc currents are set to $I_{\mathrm{dc}_1} = I_{\mathrm{dc}_2} = I_{\mathrm{dc}_3} = 45$ nA, and $I_{\mathrm{bias1}} = 135$ nA.

The capacitor has a value of 100 pF and is connected externally. The voltage sources $V_{\mathrm{dc}_{1,2,4}}$ equal 200 mV and are implemented by a resistive voltage divider.

The measurement results are summarized in Table 2 and are in good agreement with the expectations.

Table 2: Filter specifications.

Quantity	Value	Comment
Minimal supply voltage	0.95 V	
Supply current	1.9 μA	$I_{\mathrm{in}} = 180$ nA$_{\mathrm{p}}$
Quiescent supply current	1.6 μA	
Cut-off frequency range	1– $>$ 8 kHz	
Maximal signal-to-noise ratio	63 dB	100 Hz–8 kHz
Dynamic range	73 dB	100 Hz–8 kHz
Max. total harmonic distortion	2.7 %	$f_{\mathrm{in}} = 1$ kHz, $f_{\mathrm{c}} = 1.6$ kHz, $I_{\mathrm{in}} = 180$ nA$_{\mathrm{p}}$

5 Conclusions

In this paper, it was shown that dynamic translinear circuits constitute an exciting new approach to the structured design of analog signal processing functions, using transistors and capacitors only. The presented design methodology was elaborated into the design of a class-AB translinear sinh integrator for audio filter applications. Measurements on a semi-custom version of the integrator illustrate the attractive properties of dynamic translinear circuits for low-power and low-voltage applications.

Acknowledgments

This research was partially funded by the Dutch Technology Foundation (STW), project DEL33.3251.

References

[1] Mulder, J., van der Woerd, A.C., Serdijn, W.A., van Roermund, A.H.M., General current-mode analysis method for translinear filters, IEEE Transactions on Circuits & Systems I-Fundamental Theory & Applications, Vol. 44, No. 3, Mar. 1997, pp. 193-197.

[2] A.C. van der Woerd, J. Mulder, W.A. Serdijn and A.H.M. van Roermund, Recent trends in translinear integrated circuits, proc. Electronics - ET'96, Sozopol, Bulgaria, 1996.

[3] Mulder, J., Serdijn, W.A., van der Woerd, A.C., van Roermund, A.H.M., A current-mode synthesis method for translinear companding filters, proc. ICECS'97, Cairo, 15-18 December 1997, pp. 1419-1422.

[4] B. Gilbert, Translinear circuits: a proposed classification, Electronics Letters, Vol. 11, No. 1, January 1975, pp. 14-16.

[5] R.W. Adams, Filtering in the log domain, Preprint No. 1470, presented at the 63rd AES Conference, New York, May 1979.

[6] E. Seevinck, Companding current-mode integrator: a new circuit principle for continuous-time monolithic filters, Electronics Letters, 22nd November 1990, Vol. 26, No. 24, pp. 2046-2047

[7] Frey, D.R., General class of current mode filters, Proceedings - IEEE International Symposium on Circuits and Systems, Vol. 2, 1993, pp. 1435-1437.

[8] Frey, D.R., Log-domain filtering: an approach to current-mode filtering, IEE Proceedings, Part G, Circuits, Devices & Systems, Vol. 140, No. 6, Dec. 1993, pp. 406-416.

[9] Frey, D.R., Current mode class AB second order filter, Electronics Letters, Vol. 30, No. 3, Feb. 3, 1994, pp. 205-206.

[10] Frey, D.R., A 3.3 volt electronically tunable active filter usable to beyond 1 GHz, Proceedings - IEEE International Symposium on Circuits and Systems, Vol. 5, 1994, pp. 493-495.

[11] Frey, D.R., On log domain filtering for RF applications, Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting 1995, IEEE, Piscataway, NJ, USA, pp. 12-18.

[12] Frey, D.R., Exponential state space filters: A generic current mode design strategy, IEEE Transactions on Circuits & Systems I-Fundamental Theory & Applications, Vol. 43, No. 1, Jan. 1996, pp. 34-42.

[13] Frey, D.R., Log filtering using gyrators, Electronics Letters, Vol. 32, No. 1, Jan. 4, 1996, pp. 26-28.

[14] Frey, D.R. Steigerwald, L., Adaptive analog notch filter using log filtering, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 297-300.

[15] Frey, D.R., Log domain filtering for RF applications, IEEE Journal of Solid-State Circuits, Vol. 31, No. 10, Oct. 1996, pp. 1468-1475.

[16] Frey, D.R, State space synthesis of log domain filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 481-484.

[17] Enz, C., Low-power log-domain continuous-time filters: An introduction, Proc. Low-power low-voltage workshop at ESSCIRC'95, Lille, France.

[18] Punzenberger, M., Enz, C., Low-voltage companding current-mode integrators, Proceedings - IEEE International Symposium on Circuits and Systems, Vol. 3, 1995, pp. 2112-2115.

[19] Gilles van Ruymbeke, Filtres continus integres programmables, These no. 1397, EPFL, Lausanne, 1995.

[20] Fried, R., Python, D., Enz, C.C., Compact log-domain current mode integrator with high transconductance-to-bias current ratio, Electronics Letters, Vol. 32, No. 11, May 23, 1996, pp. 952-953.

[21] Punzenberger, Manfred., Enz, Christian., New 1.2-V BiCMOS log-domain integrator for companding current-mode filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 125-128.

[22] Manfred Punzenberger, Christian Enz, A 1.2-V BiCMOS companding current-mode integrator for Sigma-Delta-modulators, Proc. ICECS '96, Rhodos, Greece, Oct. 1996.

[23] Dominique Python, Rafael Fried, Christian Enz, A 1.2 volt companding current-mode integrator for standard digital CMOS processes, Proc. ICECS '96, Rhodos, Greece, Oct. 1996.

[24] van Ruymbeke, Gilles. Enz, Christian. Krummenacher, Francois. Declercq, Michel, BiCMOS programmable continuous-time filter using voltage-companding, Proceedings of the Custom Integrated Circuits Conference 1996, IEEE, Piscataway, NJ, USA, 96CH35886, pp. 93-96.

[25] Yang, Fuji. Enz, Christian. van Ruymbeke, Gilles., Design of low-power and low-voltage log-domain filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 117-120.

[26] Enz, C.C. Punzenberger, M. Python, D., Low-voltage log-domain signal processing in CMOS and BiCMOS, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 489-492.

[27] M. Punzenberger, C. Enz, A 1.2-V BiCMOS class AB log-domain filter, IEEE Proc. ISSCC, San Fransico, USA, Feb. 1997.

[28] Punzenberger, Manfred. Enz, Christian C., Noise in instantaneous companding filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 337-340.

[29] Punzenberger, Manfred. Enz, Christian C., A low-voltage power and area efficient BiCMOS log-domain filter, proc. ESSCIRC '97, pp. 256-259

[30] Punzenberger, Manfred. Enz, Christian C., A 1.2-V low-power BiCMOS class AB log-domain filter, IEEE JSSC, Vol. 32, No. 12, pp. 1968-1978, December 1997.

[31] Van Ruymbeke G., Enz C.C., Krummenacher F., Declercq M., A BiCMOS programmable continuous-time filter using image-parameter method synthesis and voltage-companding technique, IEEE Journal of Solid-State Circuits, Vol. 32, No. 3, Mar. 1997, pp. 377-387.

[32] Ngarmnil, J., Toumazou, C., Micropower analogue filter, IEE Colloquium (Digest), No. 185, 1994, IEE, Stevenage, Engl., pp. 6/1-6.

[33] Toumazou, C., Ngarmnil, J., Lande, T.S., Micropower log-domain filter for electronic cochlea, Electronics Letters, Vol. 30, No. 22, Oct. 27, 1994, pp. 1839-1841.

[34] Ngarmnil, Jitkasame. Toumazou, Chris, Fully tuneable micropower log-domain filter, IEE Colloquium (Digest), No. 122, 1995, IEE, Stevenage, Engl., pp. 9/1-9/4.

[35] Jitkasame Ngarmnil, Chris Toumazou, T.S. Lande, A fully tunable micropower log-domain filter, Proc. ESSCIRC Lille, France, 1995, pp. 86-89.

[36] Eskiyerli, M.H., Payne, A.J., Toumazou, C., State space synthesis of integrators based on the MOSFET square law, Electronics Letters, Vol. 32, No. 6, Mar. 14, 1996, pp. 505-506.

[37] Eskiyerli, M.H., Payne, A.J., Toumazou, C., State-space synthesis of biquads based on the MOSFET square law, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 321-324.

[38] J. Mahattanakul, C. Toumazou, Independent control of transconductance gain and input linear range in a MOS linear transconductance amplifier, Electronics Letters, Vol. 32, No. 18, Aug. 29, 1996, pp. 1629-1630.

[39] Mahattanakul J., Toumazou C., Pookaiyaudom S., Low-distortion current-mode companding integrator operating at f_T of BJT, Electronics Letters. Vol. 32, No. 21, Oct. 10, 1996, pp. 2019-2021.

[40] J. Mahattanakul, C. Toumazou, Instantaneous companding in ASP, Proc. IEE colloquium on Analog Signal Processing, Oxford, United Kingdom, 1996.

[41] Ngarmnil, J., Toumazou, C., Micropower log-domain active inductor, Electronics Letters. Vol. 32, No. 11, May 23, 1996, pp. 953-955.

[42] Payne, Alison. Toumazou, Chris., Linear transfer function synthesis using non-linear IC components, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 53-56.

[43] Toumazou, Payne, Pookaiyaudom, High frequency log & square-root domain analog circuits: from companding to state-space, Tutorial at ICECS '96, Rhodos, Greece, Oct. 1996.

[44] Toumazou C., Payne A., Analogue electronics - log domain processing and its applications, Electronic Engineering, Vol. 68, No. 840, Dec. 1996, pp. 45-46.

[45] Jitkasame Ngarmnil, Micropower log-domain circuits: theory and applications, Ph.D. thesis, Imperial College, London, December 1996.

[46] Drakakis, E.M., Payne, A.J., Toumazou, C., Log-domain filters, translinear circuits and the Bernoulli cell, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 501-504.

[47] Drakakis, E.M., Payne, A.J., Toumazou, C., Bernoulli operator: a low-level approach to log-domain processing, Electronics Letters, Vol. 33, No. 12, June 5, 1997, pp. 1008-1009.

[48] J. Mahattanakul, C. Toumazou, Instantaneous companding and expressing: A dual approach to linear integrator synthesis, Electronics Letters, Vol. 33, No. 1, Jan. 2 1997, pp. 4-5.

[49] Mahattanakul, Jirayuth. Toumazou, Chris., Non-linear design approach for high-frequency linear integrators, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 485-488.

[50] Mahattanakul, Jirayuth. Toumazou, Chris. Akbar, Atif Azim., DC stable CCII-based instantaneous companding integrator, IEEE International Symposium on Circuits and Systems, Vol. 2, 1997, pp. 821-824.

[51] Mahattanakul, J., Toumazou, C., Modular log-domain filters, Electronics Letters, Vol. 33, No. 13, June 19, 1997, pp. 1130-1131.

[52] D. Perry and G.W. Roberts, Log-domain filters based on LC ladder synthesis, Proc. IEEE ISCAS, Seattle, 1995, pp. 311-314.

[53] Perry, D., Roberts, G.W., The design of log-domain filters based on the operational simulation of LC ladders, IEEE Transactions on Circuits & Systems II-Analog & Digital Signal Processing, Vol. 43, No. 11, Nov. 1996, pp. 763-774.

[54] El-Gamal, Mourad. Roberts, Gordon W., LC ladder-based synthesis of log-domain bandpass filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 105-108.

[55] El-Gamal, Mourad. Leung, Vincent. Roberts, Gordon W., Balanced log-domain filters for VHF applications, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 493-496.

[56] Hematy, A. and Roberts, G.W., A fully-programmable analog log-domain filter circuit, proc. IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design, Baveno, Italy, 12-13 September 1997, pp. 91-96.

[57] Leung, Vincent W. El-Gamal, Mourad. Roberts, Gordon W., Effects of transistor nonidealities on log-domain filters, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 109-112.

[58] Tsividis, Yannis, On linear integrators and differentiators using instantaneous companding, IEEE Transactions on Circuits & Systems II-Analog & Digital Signal Processing, Vol. 42, No. 8, Aug. 1995, pp. 561-564.

[59] Tsividis, Y., General approach to signal processors employing companding, Electronics Letters, Vol. 31, No. 18, Aug. 31, 1995, pp. 1549-1550.

[60] Tsividis, Yannis. Li, Dandan., Current-mode filters using syllabic companding, IEEE International Symposium on Circuits and Systems, Vol. 1, 1996, pp. 121-124.

[61] Tsividis Y., Externally linear, time-invariant systems and their applications to companding signal processors, IEEE Transactions on Circuits & Systems II-Analog & Digital Signal Processing, Vol. 44, No. 2, Feb. 1997, pp. 65-85.

[62] Tsividis, Y., Instantaneously companding integrators, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 477-480.

[63] Mulder, J., van der Woerd, A.C., Serdijn, W.A., van Roermund, A.H.M., Current-mode companding square-root domain integrator, Electronics Letters, Vol. 32, No. 3, Feb. 1, 1996, pp. 198-199.

[64] J. Mulder, W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund, Design of current-mode companding square-root domain dynamic circuits, Proc. IEE colloquium on Analog Signal Processing, pp. 8/1-5, Oxford, United Kingdom, 1996.

[65] Mulder, J., Serdijn, W.A., van der Woerd, A.C., van Roermund, A.H.M., Syllabic companding translinear filter, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 101-104.

[66] Mulder, J., Kouwenhoven, M.H.L., van Roermund, A.H.M., Signal x noise intermodulation in translinear filters, Electronics Letters, Vol. 33, No. 14, July 3, 1997, pp. 1205-1207.

[67] Mulder, J., Serdijn, W.A., van der Woerd, A.C., van Roermund, A.H.M., Dynamic translinear circuits: an overview, proc. Symposium on IC Technology, Systems & Applications, Singapore, 10-12 September 1997, pp. 31-38.

[68] Mulder, J., Serdijn, W.A., van der Woerd, A.C., van Roermund, A.H.M., Dynamic translinear circuits: an overview, proc. IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design, Baveno, Italy, 12-13 September 1997, pp. 65-72.

[69] L.P.L. van Dijk, A.C. van der Woerd, J. Mulder and A.H.M. van Roermund, An ultra-low-power, low-voltage electronic audio delay line for use in hearing aids, IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998, pp. 291-294.

[70] M.H.L. Kouwenhoven, J. Mulder and A.H.M. van Roermund, Noise analysis of dynamically nonlinear translinear circuits, Electronics Letters, February 1998.

[71] J. Mulder, W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund: An instantaneous and syllabic companding translinear filter, IEEE Transactions on Circuits and Systems I, Vol. 45, No. 2, February 1998, pp. 150-154.

[72] J. Mulder, M.H.L. Kouwenhoven,W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund: Analysis of noise in translinear filters, IEEE International Symposium on Circuits and Systems, 1998.

[73] J. Mulder, M.H.L. Kouwenhoven,W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund: Non-linear analysis of noise in static and dynamic translinear circuits, accepted, IEEE Transactions on Circuits and Systems - II, 1998.

[74] J. Mulder, M.H.L. Kouwenhoven,W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund: Noise considerations for translinear filters, accepted, IEEE Transactions on Circuits and Systems - II, 1998.

[75] J. Mulder, Static and dynamic translinear circuits, Ph.D. thesis, Delft University of Technology, 1998.

[76] Serdijn, W.A., van der Woerd, A.C., van Roermund, A.H.M., Chain-rule resistance: a new circuit principle for inherently linear ultra-low-power on-chip transconductances or transresistances, Electronics Letters, Vol. 32, No. 4, Feb. 15, 1996, pp. 277-278.

[77] W.A. Serdijn, M. Broest, J. Mulder, A.C. van der Woerd and A.H.M. van Roermund, A low-voltage ultra-low-power current-companding integrator for audio filter applications, Proc. ESSCIRC'96, Neuchatel, Switzerland, 1996, pp. 404-407.

[78] W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund, Dynamic-range optimization in ultra-low-power fully integratable companding filters, proc. IEEE ProRISC, Mierlo, the Netherlands, 1996, pp. 299-302.

[79] W.A. Serdijn, M. Broest, J. Mulder, A.C. van der Woerd, A.H.M. van Roermund, A low-voltage ultra-low-power translinear integrator for audio filter applications, IEEE Journal of Solid-State Circuits, Vol. 32, No. 4, Apr. 1997, pp. 577-581.

[80] Serdijn, W.A. Mulder, J. van Roermund, A.H.M., Dynamic translinear circuits, proc. Low-Voltage Low-Power workshop, ESSCIRC'97, Southampton, United Kingdom, 19 September 1997.

[81] Serdijn, W.A., Mulder. J., van Roermund, A.H.M., Shortening the analog design trajectory by means of the dynamic translinear principle, proc. ProRISC CSSP'97, Mierlo, 27-28 November 1997, pp. 559-566.

[82] W.A. Serdijn, J. Mulder and A.H.M. van Roermund: Dynamic translinear circuits, proc. AACD'98, Copenhagen, 28-30 April 1998.

[83] W.A. Serdijn, M.H.L. Kouwenhoven, J. Mulder and A.H.M. van Roermund: The design of high-dynamic-range fully integratable translinear filters, accepted, Analog Integrated Circuits and Signal Processing (Kluwer), 1998.

[84] W.A. Serdijn and J. Mulder (guest editors): Special issue on dynamic translinear circuits, to appear, Analog Integrated Circuits and Signal Processing.

[85] Liu, Shen Iuan. Liao, Yu-Hung., Table-based log-domain linear transformation filter, Electronics Letters, Vol. 32, No. 19, Sep. 12, 1996, pp. 1771-1772.

[86] Fox, Robert. Nagarajan, Mahalingam. Harris, John., Practical design of single-ended log-domain filter circuits, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 341-344.

[87] W.A. Serdijn, A.C. van der Woerd, A.H.M. van Roermund and J. Davidse: "Design principles for low-voltage low-power analog integrated circuits," Analog Integrated Circuits and Signal Processing 8, July 1995, pp. 115-120.

[88] B. Gilbert: "Current-mode circuits from a translinear viewpoint: a tutorial," in: C. Toumazou, F.J. Lidgey and D.G. Haigh (editors): Analogue IC design: the current-mode approach, Peter Peregrinus, London, 1990.

[89] J. Mulder, A.C. van der Woerd, W.A. Serdijn and A.H.M. van Roermund, An RMS-DC converter based on the dynamical translinear principle, Proc. ESSCIRC'96, Neuchatel, Switzerland, 1996, pp. 312-315.

[90] Mulder J., Serdijn, W.A., van der Woerd, A.C. van Roermund, A.H.M., Dynamic translinear RMS-DC converter, Electronics Letters. Vol. 32, No. 22, Oct. 24, 1996, pp. 2067-2068.

[91] Mulder, J., van der Woerd, A.C., Serdijn, W.A., van Roermund, A.H.M., RMS-DC converter based on the dynamic translinear principle, IEEE Journal of Solid-State Circuits, Vol. 32, No. 7, July 1997, pp. 1146-1150.

[92] W.A. Serdijn, J. Mulder, A.C. van der Woerd and A.H.M. van Roermund, A wide-tunable translinear second-order oscillator, pp. 295-298, proc. IEEE ProRISC, Mierlo, the Netherlands, 1996.

[93] Serdijn, Wouter A., Mulder, Jan., van der Woerd, Albert C., van Roermund, Arthur H.M., Design of wide-tunable translinear second-order oscillators, IEEE International Symposium on Circuits and Systems, Vol. 2, 1997, pp. 829-832.

[94] Serdijn, W.A., Mulder, J., van der Woerd, A.C., van Roermund, A.H.M., A wide-tunable translinear second-order oscillator, proc. ESSCIRC'97, Southampton, United Kingdom, 16-18 September 1997, pp. 224-227.

[95] W.A. Serdijn, J. Mulder, A.C. van der Woerd and A.H.M. van Roermund: A wide-tunable translinear second-order oscillator, IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998, pp.195-201.

[96] J. Mulder, W.A. Serdijn, A.C. van der Woerd and A.H.M. van Roermund: A 3.3 V current-controlled square-root-domain oscillator, Analog Integrated Circuits and Signal Processing, Vol. 16, No. 1, April 1998, pp. 17-28.

[97] Pookaiyaudom, Sitthichai. Mahattanakul, Jirayuth., A 3.3 volt high-frequency capacitorless electronically-tunable log-domain oscillator, Proceedings - IEEE International Symposium on Circuits and Systems, Vol. 2, 1995, pp. 829-832.

[98] Sitthichai Pookaiyaudom, Jirayuth Mahattanakul, High-frequency low-distortion electronically-tunable log-domain oscillators, IEE Colloquium (Digest), 1995, England.

[99] Thanachayanont, A., Pookaiyaudom, S., Toumazou, C., State-space synthesis of log-domain oscillators, Electronics Letters, Vol. 31, No. 21, Oct. 12, 1995, pp. 1797-1799.

[100] J. Ngarmnil, A. Thanachayanont, C. Toumazou, On the design of micropower active resonators and oscillators using log-domain processing, Proc. ICECS '96, Greece, 1996.

[101] Thanachayanont, A., Payne, A.J., Pookaiyaudom, S., State-space synthesis of oscillators based on the MOSFET square law, Electronics Letters, Vol. 32, No. 18, Aug. 29, 1996, pp. 1638-1639.

[102] Pookaiyaudom, Sitthichai., Log domain oscillators, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 497-500.

[103] Thanachayanont, Apinunt. Payne, Alison. Pookaiyaudom, Sittichai., Current-mode phase-locked loop using a log-domain oscillator, IEEE International Symposium on Circuits and Systems, Vol. 1, 1997, pp. 277-280.

[104] E. Seevinck: "Analysis and synthesis of translinear integrated circuits," Elsevier, Amsterdam, 1988.

[105] J. Mulder, A.C. van der Woerd, W.A. Serdijn and A.H.M. van Roermund: "Application of the back gate in MOS weak inversion translinear circuits," IEEE Transactions on Circuits and Systems – I, Vol. 42, No. 11, 1995, pp. 958-962.

[106] A.G. Andreou and K.A. Boahen, Translinear circuits in subthreshold MOS, Analog Integrated Circuits and Signal Processing, Vol. 9, April 1996, pp. 141-166.

[107] W.A. Serdijn, A.C. van der Woerd, J. Davidse and A.H.M. van Roermund: "A low-voltage low-power fully-integratable front-end for hearing instruments," IEEE Transactions on Circuits and Systems – I, Vol. 42, No. 11, 1995, pp. 920-932.