A High Efficiency Orthogonally Switching Passive Charge Pump Rectifier for Energy Harvesters

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***Abstract*—The design and analytical modeling of a high efficiency energy harvester comprising a passive voltage-boosting network (VBN) and a switching charge pump rectifier (CPR) is presented in this paper. To improve the power conversion efficiency (PCE), the VBN increases the voltage at the input of the CPR and provides control signals for switching. Unlike traditional Schottky and diode-connected MOS transistor rectifiers, the proposed orthogonally switching CPR (OS-CPR) comprises MOS transistors as voltage-controlled switches. Analytical models for the OS-CPR are developed and presented. Circuit-level optimization techniques are employed to reduce conduction and switching losses. Simulated in a 90 nm standard CMOS technology (IBM 9RF), a 5-stage 915 MHz OS-CPR achieves a dc voltage of 1.35 V and a PCE of 11.9% with a 1 MΩ load at -18.2 dBm available input power ($P_{S,\mathrm{AV}}$). To show technology scalability of the design, the OS-CPR is also validated using AMS 0.18 μm high-voltage (HV) CMOS technology. When benchmarked with traditional rectifiers, the OS-CPR (under similar conditions) achieves a higher PCE and a higher output dc voltage. The OS-CPR is easily scalable to operate over multiple sub-GHz ISM frequency bands.**

***Index Terms*—Charge pump, energy harvesting, ISM, power conversion efficiency, radio frequency identification (RFID), rectifier.**

I. Introduction

RF ENERGY harvesting (or simply scavenging energy from radio frequency emissions) has been around for decades, yet only recently have designers begun to unravel its vastly untapped potential: a limitless power source. Broadcasting RF energy to power remote devices is suitable for wireless sensor networks (WSN), RF identification (RFID) and biomedical telemetry applications. In addition, it offers significant advantages over battery-powered solutions (e.g., low operational and assembly costs), amid negligible environmental effects [1]–[9].

Power originating from RF ambient sources may be unregulated, intermittent and/or small. Thus, in such circumstances it becomes paramount to maximize the power conversion efficiency (PCE) of the energy harvester (i.e., combined efficiency of a voltage-boosting/power matching network and the charge pump rectifier). As many RF systems are designed to operate across multiple ISM bands [10]–[13] (13.553–13.567, 300–348, 387–464 and 779–928 MHz bands), so should the power conversion circuits.

The energy harvester in this paper comprises a passive voltage-boosting network (VBN) and an orthogonally switching charge pump rectifier (OS-CPR). In turn, the VBN (a series resonant circuit) comprises a loop antenna (viewed as a single/multiple turn inductor) tuned to a carrier frequency, f_c, with a tuning capacitor, C_T [14], [15].

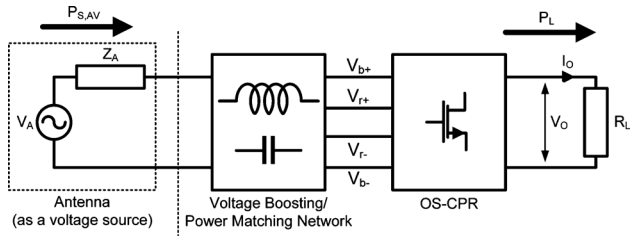

Fig. 1. Block diagram of the proposed RF energy harvester.

The threshold voltage of diodes and diode-connected MOS transistors limits the maximum PCE of a charge-pump rectifier [16], [17], thereby limiting the maximum power delivered to the load, which in turn determines the maximum operational distance of the device. Floating-gate techniques, often used to reduce/cancel the threshold voltage of MOS transistors, require a pre-charge/calibration phase, thus making them unattractive [18]. Designs employing threshold voltage cancelation techniques often present low PCE for high input power levels. In comparison, Schottky diodes (with reduced forward voltage drop) significantly increase the efficiency of the rectifier. However, the high fabrication cost (due to extra masks) associated with Schottky diodes, makes them unaffordable for low-cost solutions [19], [20].

We propose an orthogonally switching charge pump rectifier comprising MOS transistors as voltage-controlled switches. The paper is organized as follows. In Section II the circuit design of the OS-CPR is presented. Section III presents two analytical models (for near and far field conditions). In Section IV, we show that the OS-CPR achieves high PCE with an output dc voltage of 1.35 V and is easily scalable to operate across multiple ISM frequency bands. Conclusions are drawn in Section V.

II. Orthogonally Switching Charge Pump Rectifier

A. System Architecture and Circuit Topology

As in [9], [18], [21], the proposed RF energy harvester comprises a receiving antenna, a voltage boosting/power matching network and a rectifying circuit as shown in Fig. 1.

The PCE of the system is defined as

$$\mathrm{PCE} = \frac{P_L}{P_{S,\mathrm{AV}}} \tag{1}$$

where P_L is the power delivered to the resistive load R_L and $P_{S,\mathrm{AV}} = V_A^2/\mathrm{Re}\{Z_A\}$ represents the maximum signal power that can be delivered by the antenna to the VBN/OS-CPR.

To adequately drive the OS-CPR, the VBN offers large-swing signals, V_{b+} and V_{b-}, which in turn control the *orthogonal* switching behavior of the rectifier. The resonant circuit of the

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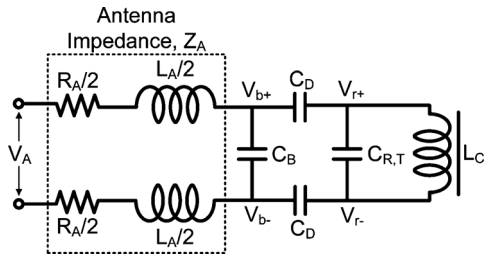

Fig. 2. Circuit diagram of the voltage boosting network.

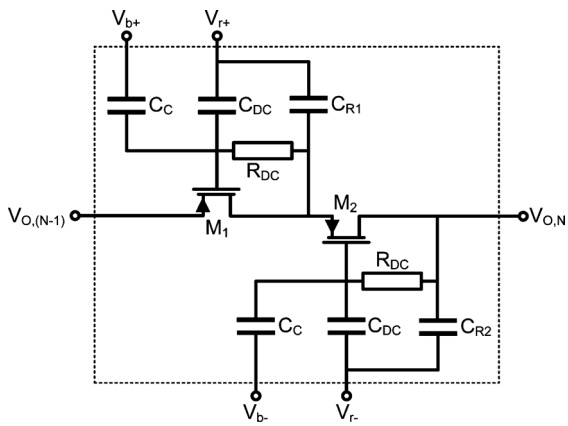

Fig. 3. Schematic of the orthogonally switching CPR (Nth-stage).

VBN is modeled by the self-inductance of the antenna, L_A, its series resistance, R_A and capacitance C_T (comprising the sum of the tuning and parasitic capacitances).

As with most charge pump rectifiers [9], [18], flow-back current reduces the PCE. To mitigate this unwanted effect, a capacitive voltage divider limits the maximum input voltage swing (V_{r+} and V_{r-}) applied to the rectifier. The tuning capacitance C_T is

$$C_T = C_B + \frac{C_D C_{R,T}}{C_D + 2C_{R,T}}$$

where C_B denotes the boost capacitance, C_D is the capacitance of the capacitive voltage divider and $C_{R,T}$ is the input capacitance of the rectifier as shown in Fig. 2. An inductive choke L_C provides a dc short at the input terminals of the rectifier. This is to ensure a zero dc offset error at the input of the OS-CPR.

Fig. 3 presents the rectifier circuitry made up of PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and for energy storage (C_{R1} and C_{R2}). To further mitigate flow-back current, parasitic capacitances C_{DC} and resistors R_{DC} set the optimum dc gate potentials of M_1 and M_2. The salient feature of the OS-CPR is its capacity to operate in both weak and strong inversion regions. Further details will be discussed in Section III.

The PCE of an N-stage OS-CPR in terms of its output voltage ($V_{O,N}$) is

$$\mathrm{PCE} = \frac{(V_{O,N})^2}{P_{S,\mathrm{AV}} R_L} = \frac{(NV_O)^2}{P_{S,\mathrm{AV}} R_L} \tag{2}$$

where the output voltage (V_O) of a single stage is

$$V_O = 2(V_r - V_{\mathrm{DS,max}}) \tag{3}$$

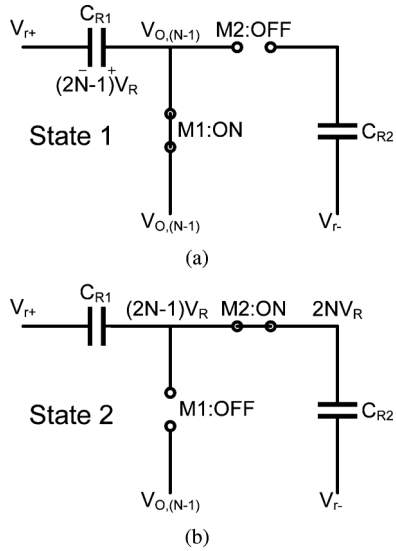

Fig. 4. State 1 (a) and State 2 (b) of the OS-CPR (Nth-stage).

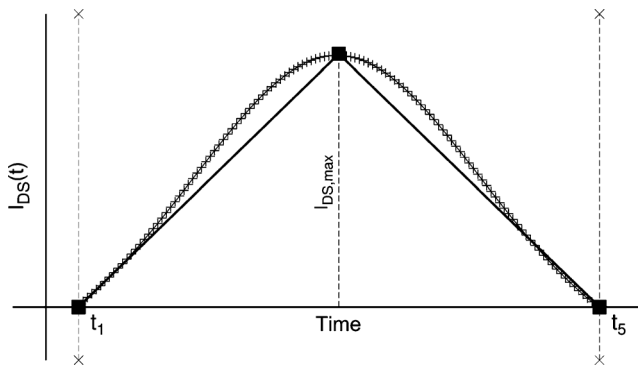

Fig. 5. The $I_{\mathrm{DS}}(t)$ curve and its triangular approximation for the PMOS transistors of the OS-CPR operating in the far field.

and V_r is the input voltage of the OS-CPR, which is defined as

$$V_r = (V_{r+} - V_{r-}). \tag{4}$$

In Section III we will derive the equation for the maximum drain-source voltage ($V_{\mathrm{DS,max}}$) of the PMOS transistors (M_1, M_2), thus arriving at the expression for the output voltage of an N-stage OS-CPR.

B. Mode of Operation

In Fig. 3, the differential signal (V_r) applied to the input of the OS-CPR is

$$V_r \approx \left(\frac{C_D}{2C_{R,T} + C_D}\right) V_b \tag{5}$$

The differential control signal (V_b) is

$$V_b = (V_{b+} - V_{b-}) \approx QV_A \tag{6}$$

where Q is the quality factor of the VBN and V_A is the voltage across the terminals of the antenna. Assuming that $V_{O,(N-1)}, V_{O,N}$ and V_{r-} are synchronized, signals V_b and V_r control the switching action of the rectifier as follows.

State 1: When M_1 is ON, M_2 is OFF, $V_{O,(N-1)} > V_{r+}$ and $V_{b+} < V_{b-}$, then C_{R1} is charged to approximately $(2N-1)V_R$. See Fig. 4(a)

State 2: When M_1 is OFF, M_2 is ON, $V_{r+} > V_{r-}$ and $V_{b+} > V_{b-}$, then C_{R2} is charged to approximately $2NV_R$, where $2NV_R$ is the output voltage of the N-stage rectifier. See Fig. 4(b).

In States 1 and 2, we assume that a large signal is present at the gate-source potentials of M_1 and M_2. This implies that charge is constantly being transferred to C_{R1} (in **State 1**) and C_{R2} (in **State 2**). When operating in the triode (linear) region, M_1 and M_2 experience a lower voltage drop across their drain-source terminals. This minimizes the power dissipation in M_1 and M_2. Compared to the state of the art, the OS-CPR presents higher PCE, especially for lower resistive loads (e.g., <300 kΩ).

III. Modeling and Approximations

In this section, we use different approximation techniques to derive the expression for the maximum drain-source voltage $V_{\mathrm{DS,max}}$ and output voltage $V_{O,N}$ of the OS-CPR in both near and far-field regions.

A. Far-Field Analysis

In the far field, the PMOS transistors of the OS-CPR operate in the weak-inversion region [22]. In this region, the drain-source current $I_{\mathrm{DS}}(t)$ is defined as

$$I_{\mathrm{DS}}(t) = I_s \exp\left[\frac{V_{\mathrm{GS}}(t) - V_{\mathrm{th}}}{nV_T}\right]\left[1 - \exp\left(\frac{-V_{\mathrm{DS}}(t)}{V_T}\right)\right] \tag{7}$$

where I_s is the product of the aspect-ratio W/L and the weak-inversion saturation current I_{DO}. From (7), $V_{\mathrm{DS,max}}$ is derived and equals

$$V_{\mathrm{DS,max}} = -V_T \ln\left[1 - \frac{I_{\mathrm{DS,max}}}{I_s \exp\left(\frac{V_{\mathrm{GS,max}} - V_{\mathrm{th}}}{nV_T}\right)}\right] \tag{8}$$

Note that $V_{\mathrm{DS,max}}$ is a function of the maximum gate-source voltage $V_{\mathrm{GS,max}}$ and the maximum drain-source current $I_{\mathrm{DS,max}}$. $V_{\mathrm{GS,max}}$ can be calculated from $V_{\mathrm{GS}}(t)$.

$$V_{\mathrm{GS}}(t) = \frac{1}{2}[V_O + V_b\cos(\omega t) - V_r\cos(\omega t + \pi)] \tag{9}$$

where $\omega = 2\pi/T$ and $T = 1/f_c$. From (9), $V_{\mathrm{GS,max}}$ becomes

$$V_{\mathrm{GS,max}} = \frac{1}{2}(V_O - V_b - V_r) \tag{10}$$

To derive the expression for $I_{\mathrm{DS,max}}$, we assume that the average voltage across C_{R2} is constant and that the charge Q_D delivered by the PMOS transistor is

$$Q_D = Q_L + \Delta Q_{C_{R2}} \tag{11}$$

where $(Q_L + \Delta Q_{C_{R2}})$ is the charge drawn by the load and is equal to $V_{O,N}T/R_L$. Thus, charge Q_D is

$$Q_D = \int_{t1}^{t5} I_{\mathrm{DS}}(t)\,\mathrm{d}t = \frac{V_{O,N}T}{R_L} \tag{12}$$

The interval $(t_5 - t_1)$ is the period of conduction of the PMOS transistors and is denoted as Δt. During the period of conduction, the function $I_{\mathrm{DS}}(t)$ resembles a triangle with base Δt and height $I_{\mathrm{DS,max}}$, as presented in Fig. 5. To simplify the analysis, we assume that the integral of $I_{\mathrm{DS}}(t)$ over Δt can be approximated by the area under the triangle. In the following subsections, we derive expressions for $I_{\mathrm{DS,max}}$ for low and high-ohmic load conditions.

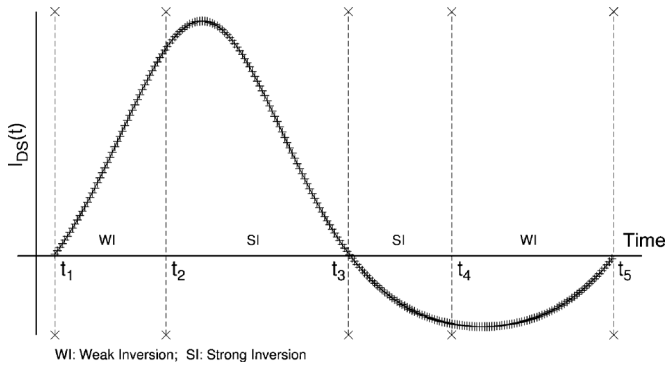

Fig. 6. The $I_{\mathrm{DS}}(t)$ curve of the PMOS transistors of the orthogonally switching CPR operating in the near-field.

1) $I_{\mathrm{DS,max}}$ for Low-Ohmic Loads: At instances t_1 and t_5, $I_{\mathrm{DS}}(t) = 0$. From (12), we can approximate $I_{\mathrm{DS,max}}$ by

$$I_{\mathrm{DS,max}} = \frac{2V_{O,N}T}{R_L(\Delta t)} \tag{13}$$

Instances t_1 and t_5 are derived from (9) when $V_{\mathrm{GS}}(t) = 0$.

$$t_1 = \frac{T}{2\pi}\left[\arccos\left(\frac{-V_O}{V_b + V_r}\right)\right] \tag{14}$$

$$t_5 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{-V_O}{V_b + V_r}\right)\right] \tag{15}$$

To derive the expression for $V_{O,N} = NV_O$, we substitute (10) and (13) in (8) and then (8) in (3) and solve for V_O. This yields

$$V_O = 2[Vr + V_T\ln(1 - K_1)] \tag{16}$$

where

$$K_1 = \frac{2V_{O,N}}{R_L(\Delta t/T)I_s\exp\left[\frac{1}{nV_T}\left(\left|\frac{V_O - V_b - V_r}{2}\right| - |V_{\mathrm{th}}|\right)\right]}$$

Note that the expression for V_O in (16) is derived for low-ohmic loads. Now we derive the expression for V_O for high-ohmic loads.

2) $I_{\mathrm{DS,max}}$ for High-Ohmic Loads: In this analysis we use a Taylor series approximation to solve for $I_{\mathrm{DS}}(t)$ and derive the expression for $I_{\mathrm{DS,max}}$. The 1st-order Taylor series expansion of Q_D in (12) is

$$Q_D = \int_{t1}^{t5}[I_1 + I_2\cos(\omega t)]\,\mathrm{d}t = \frac{\mathrm{V_{O,N}T}}{R_L} \tag{17}$$

where

$$I_1 = \frac{I_sV_O}{2nV_T\exp\left(\frac{V_{\mathrm{th}}}{nV_T}\right)} \quad I_2 = \frac{I_s(V_b + V_r)}{2nV_T\exp\left(\frac{V_{\mathrm{th}}}{nV_T}\right)}$$

From (17) we derive the expression for $I_{\mathrm{DS,max}}$.

$$I_{\mathrm{DS,max}} = I_2 + \frac{T}{\Delta t}\left(I_3 + \frac{V_{O,N}}{R_L}\right) \tag{18}$$

TABLE I
DEVICE PARAMETERS FOR AMS HV AND IBM 9RF

Process	BEOL	Oxide	FET	V_{th}	Capacitor
IBM 9RF	8-Metal	Thin	PFET	-0.22 V	HT-MiM
AMS HV	4-Metal	Thick	PFET	-0.45 V	DM-MiM

where

$$I_3 = \frac{I_2}{\pi} \sin\left[\arccos\left(\frac{-V_O}{V_b + V_r}\right)\right]$$

To find $V_{O,N} = NV_O$, we substitute (10) and (18) in (8) and then (8) in (3) and solve for V_O. This yields

$$V_O = 2(V_r + V_T \ln(1 - K_2)) \tag{19}$$

where

$$K_2 = \frac{I_2 + \frac{T}{\Delta t}\left(I_3 + \frac{V_{O,N}}{R_L}\right)}{I_s \exp\left[\frac{1}{nV_T}\left(\left|\frac{V_O - V_b - V_r}{2}\right| - |V_{\rm th}|\right)\right]}$$

There are more sophisticated approximants that require more mathematical computations to provide a higher degree of accuracy. These are beyond the scope of this paper.

B. Near-Field Analysis

The orthogonally switching CPR also operates under near-field conditions, where the transistors operate in both the weak-inversion and the strong-inversion region. Fig. 6 shows the $I_{\rm DS}(t)$ curve of the PMOS transistors in this case.

Assuming the average voltage across C_{R2} is constant,

$$Q_D = Q_L + \Delta Q_{C_{R2}} + Q_{FB} \tag{20}$$

where Q_D is the charge delivered by the PMOS transistors, $(Q_L + \Delta Q_{C_{R2}})$ is the charge $(V_{O,N}T/R_L)$ drawn by the load and Q_{FB} denotes the flow-back current through the PMOS channel. From Fig. 6, we can now rewrite (20) as,

$$\begin{aligned} Q_D &= \int_{t_1}^{t_2} I_{{\rm DS},wi}(t)\,{\rm d}t + \int_{t_2}^{t_3} I_{{\rm DS},si}(t)\,{\rm d}t \\ &= \int_{t_3}^{t_4} I_{{\rm DS},si}(t)\,{\rm d}t + \int_{t_4}^{t_5} I_{{\rm DS},wi}(t)\,{\rm d}t + \frac{V_{(O,N)}T}{R_L} \end{aligned} \tag{21}$$

where $I_{{\rm DS},wi}(t)$ (as stated in (7)) and $I_{{\rm DS},si}(t)$ are the drain-source currents of the PMOS transistors in the weak and strong inversion regions, respectively. $I_{{\rm DS},si}(t)$ equals

$$I_{{\rm DS},si}(t) = \beta_{si}[(V_{\rm GS}(t) - V_{\rm th})V_{\rm DS}(t)] \tag{22}$$

where β_{si} is the beta parameter of the PMOS transistors in strong inversion. The drain-source voltage $V_{\rm DS}(t)$ is

$$V_{\rm DS}(t) = V_r \cos(\omega t) + V_O/2 \tag{23}$$

We now derive the equations for the charge delivered to the storage capacitors in each interval. In interval (t_1, t_2), charge $Q_{(t_1,t_2)}$ is given by (24).

$$\begin{aligned} Q_{(t_1,t_2)} = \beta_{si}\frac{(t_2 - t_1)}{2}[&V_A \cos^2(\omega t_2) \\ &+ V_B \cos(\omega t_2) + V_C] \end{aligned} \tag{24}$$

Variables V_A, V_B and V_C are given by

$$\begin{aligned} V_A &= 1/2V_r(V_b + V_r) \\ V_B &= 1/4(3V_O V_r + V_O V_b - 4V_r V_{\rm th}) \\ V_C &= 1/4\left(V_O^2 - 2V_O V_{\rm th}\right) \end{aligned}$$

Similarly, the charge delivered to the storage capacitors in intervals (t_2, t_3) and (t_3, t_4) are given by (25) and (26),

$$\begin{aligned} Q_{(t_2,t_3)} = \beta_{si}\Bigg[&(t_3 - t_2)(V_A/2 + V_C) \\ &+ \frac{V_A}{4\omega}\sin(2\omega t_3) - \frac{V_A}{4\omega}\sin(2\omega t_2) \\ &+ \frac{V_B}{\omega}\sin(\omega t_3) - \frac{V_B}{\omega}\sin(\omega t_2)\Bigg] \end{aligned} \tag{25}$$

$$\begin{aligned} Q_{(t_3,t_4)} = \beta_{si}\Bigg[&(t_4 - t_3)(V_A/2 + V_C) \\ &+ \frac{V_A}{4\omega}\sin(2\omega t_4) - \frac{V_A}{4\omega}\sin(2\omega t_3) \\ &+ \frac{V_B}{\omega}\sin(\omega t_4) - \frac{V_B}{\omega}\sin(\omega t_3)\Bigg] \end{aligned} \tag{26}$$

respectively. A strong to weak inversion transition occurs at instance t_4. A 2nd-order Taylor series is used to improve the accuracy of the approximation to the charge $Q_{(t_4,t_5)}$ in interval (t_4, t_5) (27).

$$\begin{aligned} Q_{(t_4,t_5)} = \frac{I_s}{8(nV_T)^2}\Bigg[&t_5\left(V_D + \frac{(V_b + V_r)^2}{2}\right) \\ &+ \frac{V_E}{\omega}\sin(\omega t_5) + \frac{(V_b + V_r)^2}{4\omega}\sin(2\omega t_5) \\ &- t_4\left(V_D + \frac{(V_b + V_r)^2}{2}\right) - \frac{V_E}{\omega}\sin(\omega t_4) \\ &- \frac{(V_b + V_r)^2}{4\omega}\sin(2\omega t_4)\Bigg] \end{aligned} \tag{27}$$

Variables V_D and V_E are defined as

$$V_D = 8(nV_T)^2 + 4nV_T(V_O - 2V_{\rm th}) + V_O^2 - 4V_O V_{\rm th} + 4V_{\rm th}^2$$

and

$$V_E = 2(V_b + V_r)(2nV_T + V_O - 2V_{\rm th}).$$

In period (t_2, t_4) the PMOS transistors are in the strong-inversion region. The equations for t_2 and t_4 are given as

$$t_2 = \frac{T}{2\pi}\left[\arccos\left(\frac{2V_{\rm th} - V_O}{V_b + V_r}\right)\right] \tag{28}$$

$$t_4 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{2V_{\rm th} - V_O}{V_b + V_r}\right)\right] \tag{29}$$

TABLE II
PARAMETERS OF THE VOLTAGE BOOSTING NETWORK

Process	f_c (MHz)	L_A (nH)	R_A (Ω)	C_T (pF)	Q
IBM 9RF	13.56	3000	16	85	16
AMS HV	13.56	8000	16	17	42
IBM 9RF	433.92	165	16	0.8	28
IBM 9RF	915.00	108	16	0.29	38

TABLE III
TRANSISTOR ASPECT RATIOS (W/L)

Process	f_c (MHz)	W/L
IBM 9RF	13.56	250/0.4
AMS HV	13.56	700/0.2
IBM 9RF	433.92	95/0.5
IBM 9RF	915.00	47/0.5

TABLE IV
ORTHOGONALLY SWITCHING CPR COMPONENT VALUES

Process	f_c (MHz)	R_{DC} (kΩ)	C_C (pF)	C_R (pF)
IBM 9RF	13.56	200	5.5	6
AMS HV	13.56	350	8.5	9
IBM 9RF	433.92	200	1	1.2
IBM 9RF	915.00	200	1	0.65

At instance $t_3, V_{\rm DS}(t)$ is equal to 0 V. Hence, t_3 can be expressed as

$$t_3 = \frac{T}{2\pi}\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right] \tag{30}$$

We once again substitute the parameters for charge and time instances t_1 through t_5 in (21) and collect terms for the output voltage of the Nth-stage $(V_{O,N})$ of the OS-CPR operating in the near-field region, producing (31).

$$\begin{aligned} V_{O,N} &= R_L\left[\left(\frac{\beta_{si}}{\pi}\right)\alpha_1 - \left(\frac{I_s}{16\pi(nV_T)^2}\right)\alpha_2\right] \\ \alpha_1 &= \left\{\frac{1}{4}\left[\arccos\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right)\right.\right. \\ &\quad \left.\left. - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right]\left[V_A\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right)^2\right. \\ &\quad \left. + V_B\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right) + V_C\right] \\ &\quad + \left(\frac{V_A+2V_C}{2}\right)\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right] \\ &\quad - \left(\frac{V_A/2+V_C}{2}\right)\left[\arccos\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right)\right] \\ &\quad + \left(\frac{V_A}{4}\right)\sin\left[4\pi - 2\arccos\left(\frac{-V_O}{2V_r}\right)\right] \\ &\quad \left. + V_B\sin\left[2\pi - \arccos\left(\frac{-V_O}{2V_r}\right)\right]\right\} \\ \alpha_2 &= \left\{\left[V_D + \frac{(V_b+V_r)^2}{2}\right]\left[2\pi - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right]\right. \\ &\quad + \frac{(V_b+V_r)^2}{4}\sin\left[4\pi - 2\arccos\left(\frac{-V_O}{V_b+V_r}\right)\right] \\ &\quad + V_E\sin\left[2\pi - \arccos\left(\frac{-V_O}{V_b+V_r}\right)\right] \\ &\quad - \frac{(V_b+V_r)^2}{4}\sin\left[4\pi - 2\arccos\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right)\right] \\ &\quad \left. - V_E\sin\left[2\pi - \arccos\left(\frac{2V_{\rm th}-V_O}{V_b+V_r}\right)\right]\right\} \end{aligned} \tag{31}$$

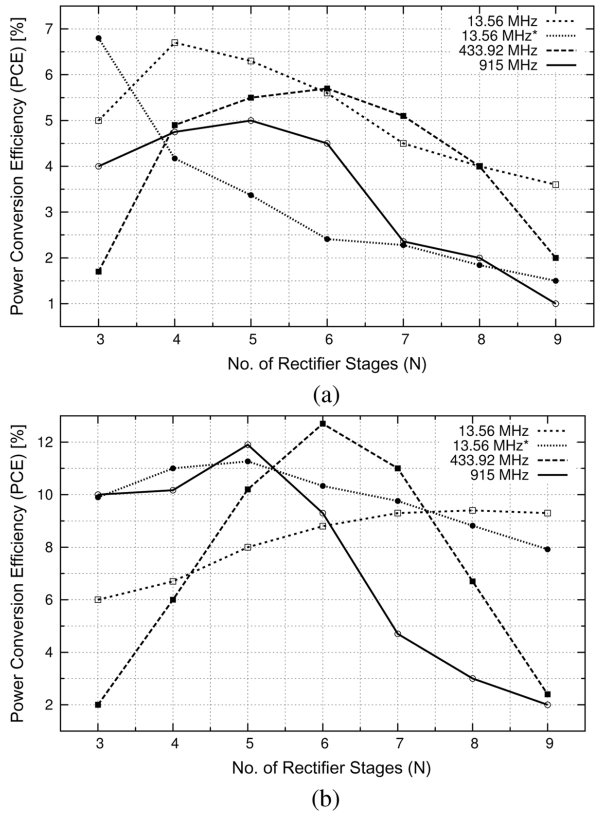

Fig. 7. Simulated PCE of the OS-CPR as a function of number of rectifier stages: (a) for 100 kΩ R_L and (b) for 1 MΩ R_L at f_c 13.56, 433.92 and 915 MHz, for $P_{S,\rm AV} = -18.2$ dBm.

TABLE V
PCE AND OPTIMUM N FOR $P_{S,\rm AV} = -18.2$ dBm

Process	f_c (MHz)	R_L (MΩ)	N	PCE (%)
IBM 9RF	13.56	0.1/1	4/8	6.7/9.4
AMS HV	13.56	0.1/1	5/5	3.5/11.3
IBM 9RF	433.92	0.1/1	6/6	5/12.7
IBM 9RF	915.00	0.1/1	5/5	5/11.9

In the following section, the analytical models of the OS-CPR are verified through simulations using two different submicron CMOS processes.

IV. SIMULATION RESULTS

The OS-CPR and the VBN are simulated in 0.18 μm (HV) and 90 nm (RF) CMOS processes (see Table I for technology characteristics).

We assume an antenna resistance (R_A) of 16 Ω (i.e., this value is estimated from the trade-off between the size, quality factor and efficiency of the antenna). Equations for the VBN

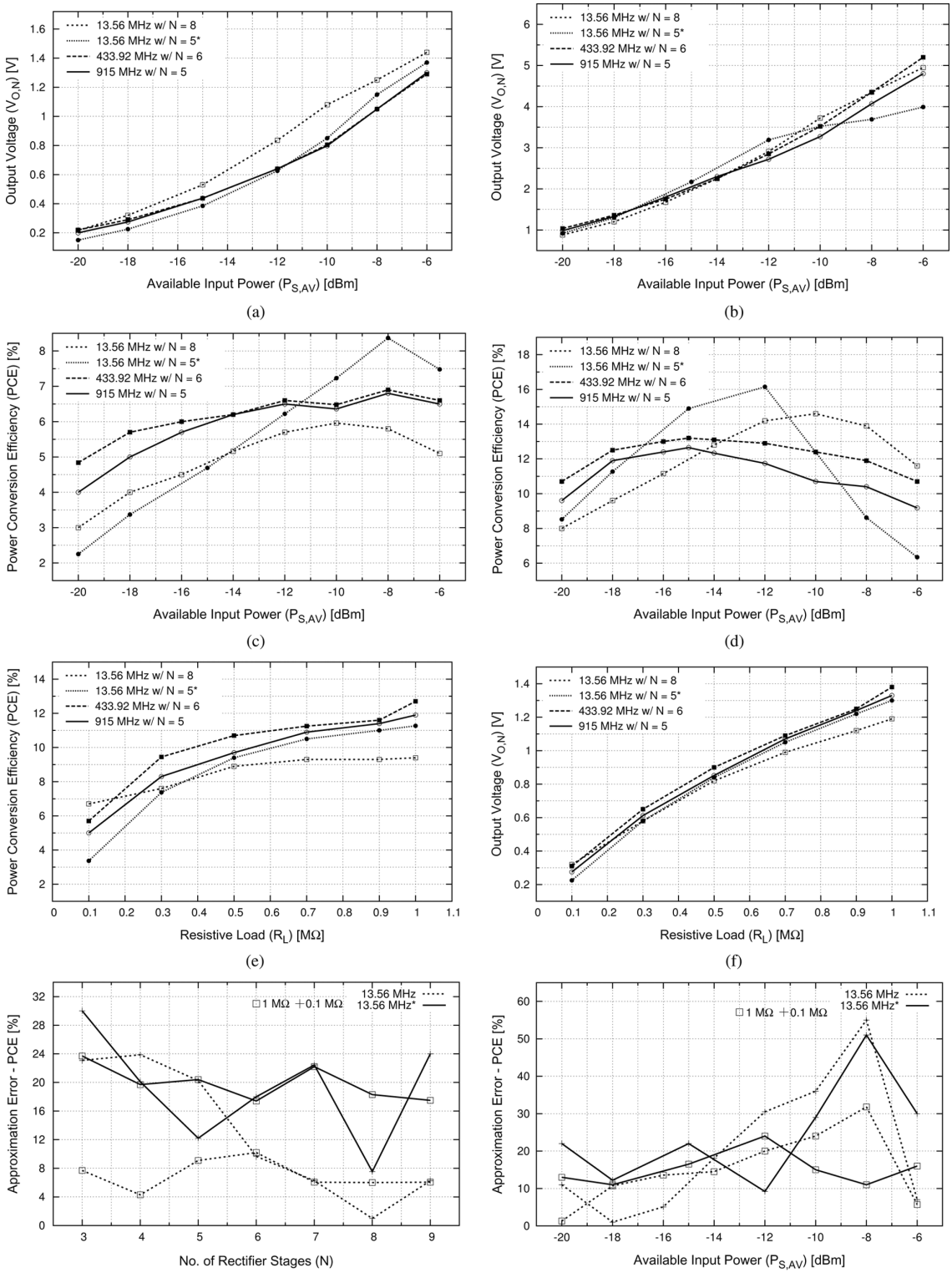

Fig. 8. Simulated output dc voltage as a function of $P_{S,\mathrm{AV}}$, (a) for 100 kΩ R_L and (b) for 1 MΩ R_L. Simulated PCE as a function of $P_{S,\mathrm{AV}}$, (c) for 100 kΩ R_L and (d) for 1 MΩ R_L at f_c 13.56 MHz, 433.92 MHz and 915 MHz. (e) PCE as a function of resistive load and (f) output dc voltage as a function of resistive load for $P_{S,\mathrm{AV}} = -18.2$ dBm at f_c 13.56, 433.92 and 915 MHz. (g) Approximation error (PCE) as a function of number of rectifier stages for $P_{S,\mathrm{AV}} = -18.2$ dBm. (h) Approximation error (PCE) as a function of $P_{S,\mathrm{AV}}$ for 100 kΩ and 1 MΩ R_L at f_c 13.56 MHz.

and the models derived in Section III facilitate the design and optimization of the OS-CPR. The algorithm used for the optimization is described as follows.

Design and Optimization Algorithm of the OS-CPR

1) Calculate the self-inductance $(L_A = R_A Q \omega^{-1})$ and tuning capacitance $(C_T = (\omega^2 L_A)^{-1})$ of VBN.
2) Calculate the voltage swings of the rectifier (V_r) and control signals (V_b) from (5) and (6), respectively.
3) Estimate the number of stages (N) from (2).
4) Estimate the aspect ratios (W/L) of transistors M_1 and M_2 from the model. Estimate C_C capacitance to be bigger than the gate-source capacitance of M_1 and M_2.

TABLE VI
SUMMARY OF THE ORTHOGONALLY SWITCHING-CPR AND COMPARISON WITH PREVIOUSLY PUBLISHED DESIGNS

Specifications	This work	Papotto [9]	Le [18]	Karthaus [19]	Kocer [21]
Frequency (MHz)	915	915	906	869	450
Conditions	Standard CMOS	Deep N-Well	Pre-charge Phase	Schottky Diodes	Low-V_{TH}
Number of stages	5	17	36	n.a.	16
V_{OUT}[§] (V) (at R_L = 1 MΩ)	1.35	0.9	1.3	n.a.	1.3
PCE[§] (%) (at R_L = 1 MΩ)	11.9	5/12[‡]	8.5	14.5 (at -20.1dBm)	11.2
PCE[§] (%) (at R_L = 0.5 MΩ)	9.7	2.8	n.a.	n.a.	n.a.
PCE[§] (%) (at R_L = 0.33 MΩ)	8.3	n.a.	1.3	n.a.	n.a.
PCE[§] (%) (at R_L = 0.1 MΩ)	5	n.a.	n.a.	n.a.	n.a.
PCE[†] (%) (at R_L = 1 MΩ)	9.2	2.25	9.1	n.a.	n.a.
	Simulated	Measured	Measured	Measured	Measured
Technology (nm)	CMOS (90)	CMOS (90)	CMOS (250)	CMOS (500)	CMOS (250)

[§] at $P_{S,AV}$ = -18.2 dBm (far-field region).
[†] at $P_{S,AV}$ = -6 dBm (near-field region).
[‡] Before/after de-embedding matching network losses.

5) For minimum ripple, calculate C_{R1} and C_{R2}.
6) Run PSS and PAC simulations.
7) Fine tune C_T and/or the OS-CPR component values for frequency optimization.
8) Repeat steps 3)–7) for system optimization.

The resulting electrical parameters of the VBN are given in Table II.

Tables III and IV show the transistor aspect ratios and the component values of the OS-CPR.

The PCE of the OS-CPR at 13.56 MHz, 433.92 MHz and 915 MHz as a function of the number of rectifier stages for R_L equal to 100 kΩ and 1 MΩ is shown in Fig. 7(a) and (b), respectively. Beyond a certain number of stages, the PCE decreases because the total voltage drop and the total capacitance (as seen from the input) increase with each additional rectifier stage. Table V presents the PCE for the optimum number of rectifier stages. Note that all curves with an asterisk are for AMS HV 0.18 μm CMOS.

Fig. 8(a) and (b) show the output dc voltage as a function of the available RF input power, $P_{S,\mathrm{AV}}$, for an R_L of 100 kΩ and 1 MΩ, respectively. As modeled, the output dc voltage increases with $P_{S,\mathrm{AV}}$. Similarly, the PCE as a function of $P_{S,\mathrm{AV}}$ for R_L equal to 100 kΩ and 1 MΩ is shown in Fig. 8(c) and (d), respectively. At high RF input power levels, the PCE decreases because of current flow-back.

The PCE as a function of the resistive load is shown in 8(e). Unlike traditional rectifiers, the OS-CPR can operate over a large range (300 kΩ to 1 MΩ) of resistive loads. Fig. 8(f) presents the output dc voltage as a function of the resistive load. As modeled in the far-field analysis, the output dc voltage increases logarithmically with the load resistance.

Fig. 8(g) presents the approximation error in PCE (i.e., modeled vs. simulated) as a function of the number of rectifier stages for $P_{S,\mathrm{AV}} = -18.2$ dBm at 13.56 MHz. The peak error in PCE is 29% for a load resistance of 100 kΩ. This discrepancy of 29% will reduce with higher-order Taylor series expansions. The approximation error in PCE as function of $P_{S,\mathrm{AV}}$ for resistive loads of 100 kΩ and 1 MΩ is shown in Fig. 8(h). Note that the peak error in PCE is seen at the transition point from weak to strong inversion mode of operation. Instead of using the weak-inversion model until transition, an analytical model for the moderate inversion regime must be developed. From simulations, we see that the approximation error in PCE as a function of the resistive load (0.1 to 1 MΩ) for $P_{S,\mathrm{AV}} = -18.2$ dBm is $16 \pm 4\%$.

Table VI compares the OS-CPR to recently published rectifiers in CMOS technologies. Power conversion efficiency is an appropriate figure-of-merit (FOM) for energy conversion circuits. The results from our analytical models closely match simulation results and thus we can say that this design demonstrates superior PCE over a wide range of resistive loads and frequency bands. Moreover, to achieve an output dc voltage of 1.35 V at R_L of 1 MΩ only a 5-stage rectifier is required. This rectifier is technology scalable and operates under both near-field and far-field conditions.

V. CONCLUSION

The design of an orthogonally switching charge-pump rectifier with high PCE is presented. The OS-CPR comprises MOS transistors as voltage-controlled switches. Analytical models and simulation results in 90 nm show that a 5-stage 915 MHz OS-CPR with a 1 MΩ load achieves a dc voltage of 1.35 V and a PCE of 11.9% at -18.2 dBm available input power. When compared to traditional rectifiers, the OS-CPR (under similar conditions) achieves a higher PCE and a larger output dc voltage. Simulations show that the OS-CPR is both technology and frequency scalable.

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REFERENCES

[1] J. Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2193–2202, Nov. 2005.
[2] W. G. Yeoh, Y. B. Choi, K. Y. Tham, S. X. Diao, and Y. S. Li, "A CMOS 2.45-GHz radio frequency identification tag IC with read/write memory," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2005, pp. 365–368.
[3] R. Barnett, J. Liu, and S. Lazar, "A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 354–370, Feb. 2009.
[4] S. Pellerano, J. Alvarado, Jr., and Y. Palaskas, "A mm-wave power harvesting RFID tag in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1627–1637, Aug. 2010.
[5] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10 m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.
[6] H. Nakamoto *et al.*, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35 μm technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101–110, Jan. 2007.

[7] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.
[8] J. P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for micro-power rectifier analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2771–2779, Dec. 2005.
[9] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011.
[10] A. Missoni, C. Klapf, W. Pribyl, H. Guenter, and G. Holweg, "A triple-band passive RFID tag," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 288–614.
[11] J. Bouvier, T. Thorigne, S. Hassan, M. Revillet, and P. Senn, "A smart card CMOS circuit with magnetic power and communications interface," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1997, pp. 296–297.
[12] G. de Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2978–2990, Sep. 2005.
[13] M. Baghaei-Nejad, D. S. Mendoza, Z. Zou, S. Radiom, G. Gielen, L. Zheng, and H. Tenhunen, "A remote-powered RFID tag with 10 Mb/s UWB uplink and 18.5 dBm sensitivity UHF downlink in 0.18 m CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2009, pp. 198–199.
[14] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. de Flaviis, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 6, pp. 1089–1097, Jun. 2007.
[15] N. Soltani and F. Yuan, "A high-gain power-matching technique for efficient radio-frequency power harvest of passive wireless microsystems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2685–2695, Oct. 2010.
[16] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.
[17] H. Xu and M. Ortmanns, "A temperature and process compensated ultra low-voltage rectifier in standard threshold CMOS for energy-harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 12, pp. 812–816, Dec. 2011.
[18] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.
[19] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7 μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.
[20] R. Barnett, G. Balachandran, S. Lazar, B. Kramer, G. Konnail, S. Rajasekhar, and V. Drobny, "A passive UHF RFID transponder for EPC gen 2 with -14 dBm sensitivity in 0.13 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2007, pp. 582–623.
[21] F. Kocer and M. P. Flynn, "A new transponder architecture with on-chip ADC for long-range telemetry applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1142–1148, May 2006.
[22] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. Hoboken, NJ, USA: Wiley, 2001.

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