An Implementation of Least-Voltage Drop Stimulator Circuit for Cochlear Implants

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Abstract : Implantable neural stimulators can be effective for the treatment of many pathologies. Examples include cochlear implants [1] and deep brain stimulators [2]. From an electrical point of view neural stimulation essentially means conveying a particular amount of charge into the tissue.

A novel method to maximize charge transfer was proposed by maximizing the output impedance of the current source using a double loop feedback topology [3]. The output resistance of a MOS current mirror circuit requires only one effective drain-source voltage drop.

In this work we aim to implement the proposed stimulator circuit for use in cochlear implants (R_{tissue}≈1~10kΩ, C_{tissue}≈1~10nF) using the 0.18µm AMS HV technology. To minimize the area occupied by the circuit, the number of HV transistors applied should be as small as possible. The stimulation current is set by scaling a reference current using a DAC configuration. To minimize the number of HV transistors, the DAC is implemented in two stages: one using LV transistors and one using HV transistors. A minimum number of 3 bits for the HV DAC (an effective transistor width of $(2^3-1)*5u$) is required to support the maximum stimulation current (1.05mA). The remaining 4 bits are handled by the low voltage DAC.

The circuit uses a single supply voltage only and therefore a switch array is incorporated to inverse the stimulation current direction to achieve charge balanced stimulation. Because of the inversion of the tissue polarity, the potential at a tissue node can become negative. In order to prevent substrate leakage current, a Shottkey diode is added in series with the switch.

Simulation results, using the AMS 0.18µm high-voltage CMOS process, show that the charge error within a cycle (600µs) is only 0.02%, equivalent to a DC current error of 3nA at the maximum stimulation current with a load of 10kΩ+10nF.

Reference :

[1] J. Georgiou and C. Toumazou, "A 126 µW cochlear chip for totally implantable system," *IEEE J. Solid- State Circuits*, vol. 40, no. 2, pp. 430-443, 2005.

[2] M. N. van Dongen and W. A. Serdijn, "Design of a low power 100 dB dynamic range integrator for an implantable neural stimulator", IEEE BioCAS, Paphos, Cyprus, Nov. 3-5, 2010.

[3] C. Sawigun, W. Ngamkham, M. van Dongen and W. A. Serdijn,"A Least-Voltage Drop High Output Resistance Current Source for Neural Stimulation," Proc. IEEE BioCAS, Paphos, Cyprus, Nov. 3-5, 2010.

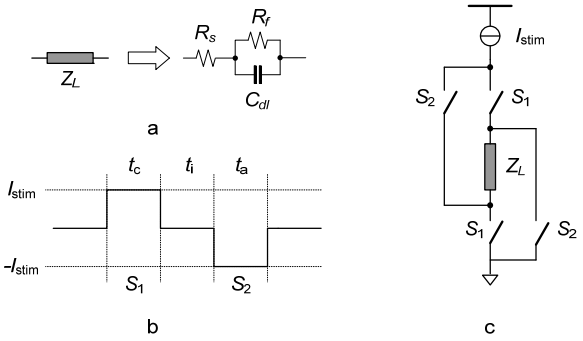

Figure 1. Biphasic current stimulation concept

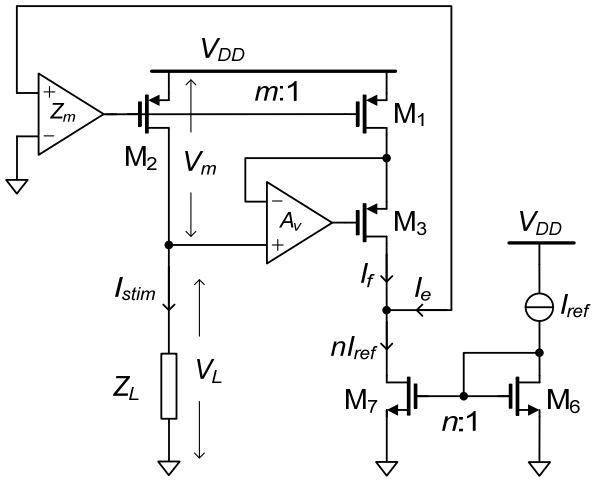

Figure 2. A concept of current stimulator

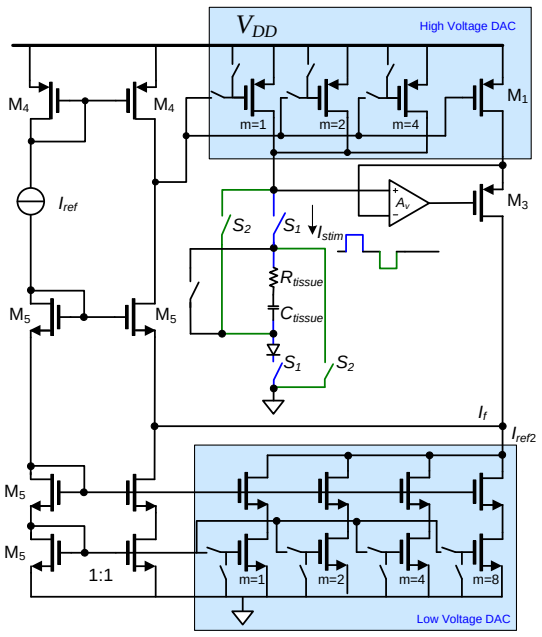

Figure 3. The implemented current stimulator

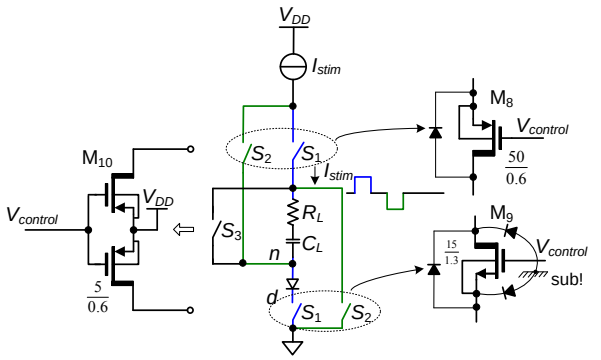

Figure 4. Switch array

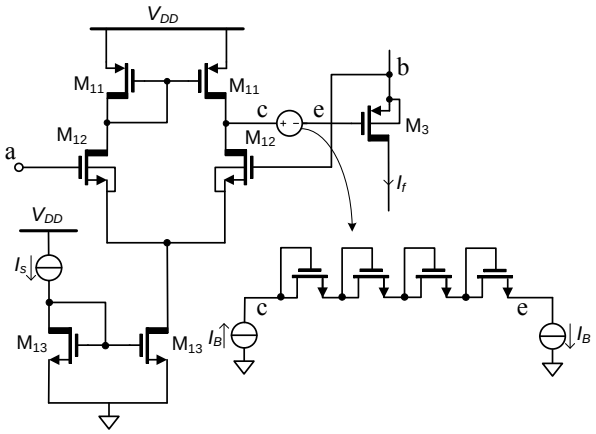

Figure 5. Differential amplifire, A_v

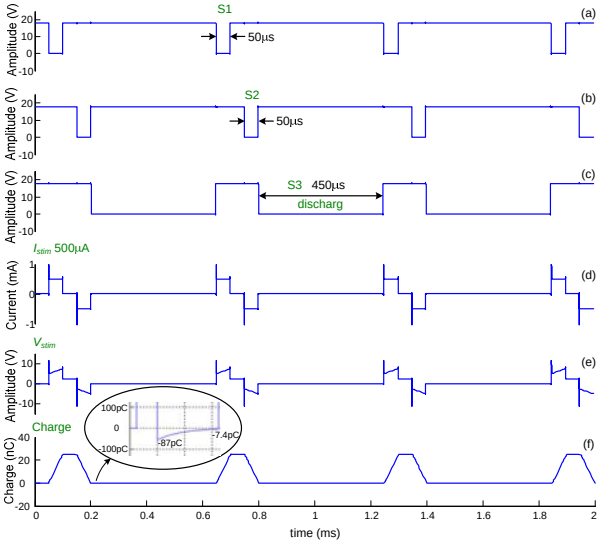

Figure 6. Transient simulation waveform of a stimulation current of 500µA with a load of 10kΩ+10nF. (a) Switch control signal S1, (b) Switch control signal S2, (c) Switch control signal S3, (d) stimulation current, (e) electrode potential and (f) total charge at the load.